ENG - 472

0.35µm CMOS C35 SPICE Models

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Contents

1 Introduction 3
1.1 Revision 3
1.2 Related Documents 3
2 Simulation Models 4
2.1 Introduction 4
2.2 Parameter Extraction 4
2.3 MOS Transistor Model 5
2.4 Waffle Transistor Model 7
2.5 HV MOS Transistor Model 9
2.6 Bipolar Transistor Model 9
2.7 Well Resistor Model 12
2.8 Diffusion Resistor Model 12
2.9 Poly2 and High Resistive Poly Resistor Model 13
2.10 Low TC Poly Resistor Model 14
2.11 Poly and MIM Capacitor Model 15
2.12 MOS Capacitor Model 16
2.13 Diode Model 17
2.14 Zener Diode Model 17
2.15 Schottky Barrier Diode Model 18
2.16 Model Feature Overview Table 19
2.17 Summary of Simulation Models 21
2.18 Circuit Simulators and Models 24
3 Characteristic Curves 25
3.1 Introduction 25
3.2 MOS Transistor Characteristics 26
3.3 Bipolar Transistor Characteristics 70
3.4 Well Resistor Characteristics 71
3.5 Poly Resistor Temperature Characteristics 72
3.6 Capacitor Characteristics 73
3.7 Schottky Barrier Diode Characteristics 74
4 Support 75

1 Introduction

1.1 Revision

Change Status of Pages (including short description of change)

Revision	Date	Changes	Affected pages
1.0	March 2013	First version of document specification **New:** HiSIM2.5.1 is supported for MOSFETs, Waffle transistor model, CPMIM model. **Changed:** CMIM model.	1-73
2.0	March 2014	**Changed:** improved models for the Schottky barrier diode	18,20,23,25,74

1.2 Related Documents

Description	Document Number
0.35µm CMOS C35 Process Parameters	ENG - 182
0.35µm CMOS C35 Design Rules	ENG - 183
0.35µm CMOS C35 Noise Parameters	ENG - 189
0.35µm CMOS Matching Parameters	ENG - 228
C35 ESD Design Rules	ENG-236
Standard Family Cells	ENG-42
Assembly Related Design Rules	ASSY-15

2 Simulation Models

2.1 Introduction

This section presents a summary of circuit simulation models for MOS transistors, CMOS compatible bipolar transistors, resistors and capacitors.

The characterization temperature range is -40°C <=T<=180°C.

The simulation parameters are intended for use with the analog circuit simulator SPICE or one of the improved simulators derived from SPICE (e.g. ELDO, SPECTRE, HSPICE) or any other simulation program which contains SPICE compatible models. Technology files for other circuit simulation tools are available on request. All parameters and technology files are available via internet, by email or with the HitKit.

The information in this document is not exhaustive and does not intend to cover all possible limitations.

2.2 Parameter Extraction

High precision mixed analog and digital circuit simulation requires good parameter extraction strategies and accurate models. In general, the quality of a parameter extraction procedure depends on the selection of measured data (1), on the parameter extraction program (2) and on the simulation model (3).

The Input Data

We use measured current-voltage and conductance-voltage characteristics of a matrix of element geometry under all operating conditions. The geometry and the operating points are carefully selected in order to fulfill the requirements of typical mixed analog-digital design applications.

The Parameter Extraction Program

This program contains tools for extracting and optimizing the SPICE model parameters. The non-linear least-square-fit routine can optimize multiple devices with respect to multiple bias conditions in order to reduce the error between the simulated data and the measured data.

2.3 MOS Transistor Model

We supply SPICE parameters for the BSIM3v3.24 and for the HiSIM2.5.1 model.

2.3.1 BSIM3v3.24 MOS Transistor Model Features

- Modeling for ids, gm and gds for all MOS transistor operation regions up to the maximum operating conditions.
- Modeling of impact ionization including body current and the resulting additional drain current.
- Modeling of the bias dependent and bias independent overlap capacitances.
- Use of the BSIM3v3 1/f and thermal noise equation.
- Device mismatch modeling for threshold voltage and mobility.
- Modeling temperature range validity -40°C up to 180°C

2.3.2 BSIM3v3.24 MOS Transistor Model Limitations and Restrictions

- The MOS transistor model is valid within the specified operation conditions only.
- The SPICE models for the devices listed in this document are intended for analog/mixed signal applications only.
- MOS transistor models are valid only up to a frequency of 1GHz for minimum channel length.
- The model does not include poly depletion effects or finite thickness charge layer effects.

2.3.3 BSIM3v3.24 MOS Transistor Worst Case Corner Model

We supply typical mean (TM) parameters, which have been extracted from typical wafers. Additionally, the worst case tolerances of the main parameters are given. They can be used to establish worst case parameter sets. Four predefined worst case parameter sets are available: WP=worst case power=fast NMOS & fast PMOS, WS=worst case speed=slow NMOS & slow PMOS, WO=worst case one=fast NMOS & slow PMOS, WZ=worst case zero=slow NMOS & fast PMOS. Statistical parameter sets for Monte Carlo simulations (MC) are available on request.

Please note that parameters do not vary independently:

NMOS and PMOS transistors of the same wafer should have the same TOX, XW, etc.

Even for one type of transistor, most parameters are correlated. In principle only the four parameters TOX, XL, XW and VTH0 are linearly independent and their tolerances are related to process variations. We have additionally specified the tolerances of the first-order parameters NSUB, NCH and UO although they are correlated with VTH0. On the other hand we have neglected all variations of parameters describing second order effects.

The worst case tolerances of K1 and K2 are calculated from the worst case tolerances of TOX, NSUB, and NCH.

Note: The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control

parameters are extracted from simplified model equations. Hence, circuit simulation parameters may differ from their corresponding process control transistor parameters.

Following BSIM3v3.24 SPICE parameters are varied within the worst case parameter sets

tox	gate oxide thickness (related to TGOX)
vth0	threshold voltage large transistor (related to VTO10X10)
u0	carrier mobility (related to KP)
xl	channel length offset parameter (related to LEFF)
xw	channel width offset parameter (related to WEFF)
nsub, nch	Substrate and channel doping concentration (related to GAMMA and TGOX)
cgsl, cgdl	light doped source/drain–gate overlap capacitance (related to TOX)
cgbo	gate-bulk overlap capacitance (related to TOX)
rsh	drain-source diffusion resistance (related to RDIFF)
cj, cjsw	area and sidewall junction capacitance (related to CJ, CJSW)

2.3.4 HiSIM2.5.1 Transistor Model Features

- Surface potential based model.
- Quantum-Mechanical Effects.
- Channel-Length Modulation.
- Narrow-Channel Effects.
- Source/Bulk and Drain/Bulk Diode Models.
- Non-Quasi-Static (NQS) Model.
- HiSIM2 uses advanced 1/f noise model describing carrier and mobility fluctuations. For thermal noise modeling no additional model parameters are required as being a function of the surface potential and its derivatives.
- Modeling for ids, gm and gds for all HV MOS transistor operation regions up to the maximum operating conditions for the specified layout.
- Device mismatch modeling.
- Sub-threshold current and leakage modeling.
- Modeling temperature range validity -40°C up to 180°C.
- Parasitic Models:
  We supply extended transistor models including additional drain-well diodes and substrate diodes for a more realistic simulation of diode-leakage and parasitic capacitance.
- SOAC Models:
  Models including Safe Operating Area Check (SOAC) are provided for simulators SPECTRE and Eldo. The models enable the interactive checking of operating conditions during circuit simulation. It is highly recommended to use those models for high voltage design application.

2.3.5 HiSIM2.5.1 Transistor Model Limitations and Restrictions

- The MOS transistor model is valid within the specified operation conditions only.

- The SPICE models for the devices listed in this document are intended for analog/mixed signal applications only.
- RF modeling is not supported.
- The model does not include poly depletion effects or finite thickness charge layer effects.
- The model does not include gate current model effects.

2.3.6 HiSIM2.5.1 Worst Case model

Following HiSIM_HV SPICE parameters are varied within the worst case corner parameter sets:

tox	gate oxide thickness (related to TGOX)
vfbc	flat-band voltage (related to VTO10X10)
mueph1,muephl	phonon scattering (related to KP and IDSAT)
xl	channel length offset parameter (related to LEFF)
xw	channel width offset parameter (related to WEFF)
nsubc, nsubp	Substrate doping and maximum pocket concentration (related to GAMMA and TGOX)
clm6	channel-length-modulation parameter (related to GDS)
vmax	saturation velocity (related to IDSAT)
lover	lightly doped source/drain–gate overlap length (related to TOX)
cgso, cgdo	source/drain–gate overlap capacitance (related to TOX)
cgbo	gate-bulk overlap capacitance (related to TOX)
rsh	source/drain sheet resistance of diffusion region (related to RDIFF)
cj, cjsw	area and sidewall junction capacitance at zero bias (related to CJ, CJSW)

2.4 Waffle Transistor Model

The waffle structure is a transistor array where a specific S/D diffusion is shared by four transistors (in a center device), by two transistors (in an edge device) or by one transistor only (corner device). Alternating metal stripes for source and drain connect all transistors of the array in parallel. 3.3V and 5V waffle transistors are provided: NMOSW, PMOSW, NMOSMW and PMOSMW. We supply SPICE parameters for a BSIM3v3.24 based sub-circuit model shown in Fig.2.1, which is a parallel connection of three components: center, edge and corner transistors.

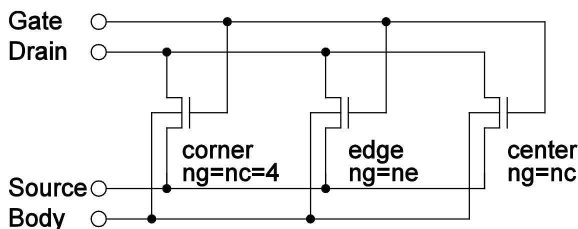

Fig.2.1 The waffle transistor sub-circuit model.

2.4.1 Device Restrictions

The following parameters can be set in the simulation environment:

- Number of rows and columns

- Channel length L=0.5 um to L=3 um continuous scalable.

Constant parameters are:

- Gate to S/D diffusion contact distance = 1.2 um = const.
- Width of a transistor: W = 4 um = constant.

The simulation sub-circuit and the PCELL are generated according to the chosen number of columns and rows.

2.4.2 Waffle MOS Transistor Model Features

- Modeling for ids, gm and gds for all MOS transistor operation regions up to the maximum operating conditions for the specified layout.
- Use of the SPICE 1/f and thermal noise equation.
- Modeling temperature range validity -40°C up to 180°C

2.4.3 Waffle MOS Transistor Model Limitations and Restrictions

- The MOS transistor model is valid within the specified operating conditions only.
- The SPICE models for the devices listed in this document are intended for analog/mixed signal applications only. RF modeling is not supported.
- The model does not include poly depletion effects or finite thickness charge layer effects.
- The impact ionization and the resulting body and drain current are not modeled.
- Self-heating is not modeled.
- The compact waffle structure must not be used for current mirror applications. Current mirrors can be realized by isolating the mirror diode. This can be achieved by splitting the shared diffusions.

2.4.4 Waffle Transistor Worst Case Corner Model

Following BSIM3v3 SPICE parameters are varied within the worst case corner parameter sets

tox	gate oxide thickness (related to TGOX)
vth0	threshold voltage large transistor (related to VTO3N)
u0	carrier mobility (related to KP)
xl	channel length offset parameter (related to LEFF)
xw	channel width offset parameter (related to WEFF)
nsub, nch	Substrate and channel doping concentration (related to GAMMA and TGOX)
cgsl, cgdl	light doped source/drain–gate overlap capacitance(related to TOX)
cgbo	gate-bulk overlap capacitance (related to TOX)
cj, cjsw	area and sidewall junction capacitance (related to CJ, CJSW)

2.5 HV MOS Transistor Model

We supply SPICE parameters for the BSIM3v3.24 sub-circuit model.

2.5.1 HV MOS Transistor Model Features

- Modeling for ids, gm and gds for all HV MOS transistor operation regions up to the maximum operating conditions for the specified layout.
- Use of the SPICE 1/f and thermal noise equation.
- Modeling temperature range validity -40°C up to 180°C

2.5.2 HV MOS Transistor Model Limitations and Restrictions

- The MOS transistor model is valid within the specified operating conditions only.
- The SPICE models for the devices listed in this document are intended for analog/mixed signal applications only. RF modeling is not supported.
- The model does not include poly depletion effects or finite thickness charge layer effects.
- The impact ionization and the resulting body and drain current is not modeled.
- Self heating is not modeled.

2.5.3 HVMOS Transistor Worst Case Corner Model

Following HV MOS BSIM3v3 SPICE parameters are varied within the worst case corner parameter sets

tox	gate oxide thickness (related to TGOX)
vth0	threshold voltage large transistor (related to VTO10X10)
u0	carrier mobility (related to KP)
xl	channel length offset parameter (related to LEFF)
xw	channel width offset parameter (related to WEFF)
nsub, nch	Substrate and channel doping concentration (related to GAMMA and TGOX)
cgsl, cgdl	light doped source/drain–gate overlap capacitance(related to TOX)
cgbo	gate-bulk overlap capacitance (related to TOX)
rhv	drain-source diffusion resistance (related to ron)
cj, cjsw	area and sidewall junction capacitance (related to CJ, CJSW)

2.6 Bipolar Transistor Model

Two parasitic bipolar devices are inherently available for design in any CMOS technology: VERT10 and LAT2

The **vertical bipolar transistor** (VERT10) uses the substrate as the (common) collector, the well as the base and diffusion as the emitter. We supply SPICE parameters for the standard SPICE Gummel-Poon model for VERT10 for the fixed layout.

The CMOS-compatible **lateral bipolar transistor** (LAT2) consists of a diffusion square as the emitter, a diffusion ring around it as the collector and a well as the base. Emitter and collector are separated by gate area. We supply SPICE parameters for a special sub-circuit model based on the standard SPICE Gummel-Poon for LAT2 (Fig. 2.2) for the fixed layout.

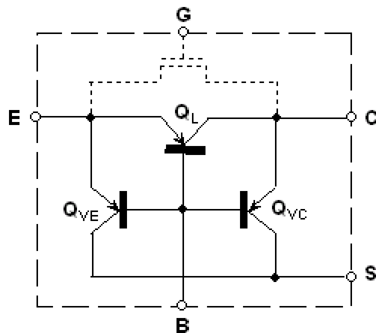

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Fig.2.2 Equivalent circuit of the lateral bipolar transistor (LAT2).

The complete LAT2 transistor is modeled with main bipolar transistor (QL) and additional two vertical parasitic transistors under the emitter (QVE) and the collector (QVC). Both the vertical collector current as well as the parasitic substrate current is modeled. Though the PMOS transistor between the E and C region of the LAT device is indicated, it is not modeled. The gate (G) voltage VGB=2V was applied during the measurements for the model.

Note: The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations. Hence, the circuit simulation parameters BF, IKF and VAF may differ from their corresponding process control transistor parameters BETA, ICHB and VAF.

2.6.1 Bipolar Transistor Model Features

- Modeling temperature range validity -40°C up to 180°C
- 1/f noise modeling for VERT10
- VERT10 mismatch modeling for forward gain current beta and saturation current IS.

2.6.2 Bipolar Transistor Model Limitations and Restrictions

- The collector current of LAT2 (lateral PNP bipolar transistor) is a function of the gate voltage. The circuit simulation parameters are valid for a positive gate-emitter voltage VGE of about 1 V. For zero or negative gate-emitter voltages, the collector current is increased considerably by the parasitic MOS current. This effect is not included in the circuit simulation model.
- Lateral and vertical PNP transistor models are valid only up to a frequency of 800MHz.
- 1/f noise and mismatch parameters are not available for LAT2

2.6.3 Bipolar Transistor Worst Case Corner Model

We supply parameters, which represent the typical mean (TM) process condition. Additionally, the worst case tolerances of the main parameters are available. They can be used to establish worst case parameter sets. Three predefined worst case parameter sets are available: HS = high speed & high beta, LB = low speed & low beta, HB = low speed & high beta. Statistical parameter sets for Monte Carlo simulations (MC) are also available on request.

VERT10: Following Gummel - Poon SPICE parameters are varied within the worst case corner parameter sets

is	saturation current (related to VBE)
bf	current gain (related to BETA)
vaf	Early voltage (related to VAF)
cje	e-b junction capacitance (related to CJP)
cjc	b-c junction capacitance (related to CJN)
ikf	forward beta high current roll off
rb	base resistor (related to RPWELLS and RPWELLR)
rbm	minimum base resistor at high currents
re	emitter resistor (related to RDIFF)
rc	collector resistor (related to RPWELLS and RPWELLR)
tf	ideal forward transit time

Lat2: Following Gummel - Poon SPICE parameters are varied within the worst case corner parameter sets

is	saturation current (related to VBE)
bf	forward current gain (related to BETA)
bfv	forward current gain for vertical pnp at emitter side (related to BETA)
vaf	Early voltage (related to VAF)
cje	e-b junction capacitance (related to CJP)
cjc	b-c junction capacitance (related to CJN)
ikf	forward beta high current roll off
rb	base resistor (related to RPWELLS and RPWELLR)
rbm	minimum base resistor at high currents
re	emitter resistor (related to RDIFF)
rc	collector resistor (related to RPWELLS and RPWELLR)
tf	ideal forward transit time

2.7 Well Resistor Model

The following non-linear resistor is available for design: RNWELL

Field well resistors (covered by field oxide) are available for design. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence of their resistance due to the resistor-to-bulk diodes, which cannot be described by the 2-terminal resistor model in SPICE.

2.7.1 Well Resistor Model Features

- We supply model parameters for the 3-terminal SPICE JFET model. The substrate is the gate of the JFET.
- Modeling temperature range validity -40°C up to 180°C

2.7.2 Well Resistor Model Limitations and Restrictions

- RNWELL is a field n-well resistor (covered by field oxide). Device n-well resistors (covered by gate oxide) are not supported.
- The JFET noise model in SPICE is only valid in saturation. Therefore, it is recommended to replace n-well resistors by standard resistors for correct simulation of the thermal noise.
- The model is only valid up to |5V|.
- The model is valid for L/W > 5 only
- 1/f noise and mismatch modeling is not included

2.7.3 Well Resistor Worst Case Model

Following SPICE parameters are varied within the worst case corner parameter sets:

beta	sheet resistance (related to RNWELL)
wd	width reduction (related to WNWELL)
cj, cjsw	area and sidewall junction capacitance

2.8 Diffusion Resistor Model

Model parameters for the diffusion resistors RDIFFN3 and RDIFFP3 are available. These resistors are only intended for use in periphery cells.

2.8.1 Diffusion Resistor Model Features

- We supply model parameters for the 3-terminal SPICE JFET model. The model includes the parasitic temperature dependent leakage current and the junction capacitances. The substrate is the gate of the JFET.
- Modeling temperature range validity -40°C up to 180°C

2.8.2 Diffusion Resistor Model Limitations and Restrictions

- The model is valid for L/W > 5 only
- 1/f noise and mismatch modeling is not included

2.8.3 Diffusion Resistor Worst Case Model

Following resistor SPICE parameters are varied within the worst case corner parameter sets:

rsh	sheet resistance (related to RDIFFN/RDIFFP)
wd	width reduction (related to WDIFFN/WDIFFP)
cj, cjsw	area and sidewall junction capacitance

2.9 Poly2 and High Resistive Poly Resistor Model

The voltage and temperature modeling of RPOLY2, RPOLY2P, RPOLY2PH and RPOLYH is taken into account by the following equations:

Temperature modeling:

$$\frac{R(T)}{R(T0)} = 1 + TCR1 \cdot (T - T0) + TCR2 \cdot (T - T0)^2$$

Voltage dependent modeling:

$$R_{T_0}(W, L, V) = RSH \cdot \frac{L - LD}{W - WD} \cdot \left[1 + RV(W) \cdot \left(\frac{V}{L}\right)^2\right]$$

$$RV(W) = TCR1 \cdot RTH \cdot W^{WEX}$$

L	drawn resistor length
W	drawn resistor width
WD	width reduction parameter
R(T)	temperature dependent resistor
R(T0)	resistor at 27°C
TCR1	linear temperature coeff.
TCR2	quadratic temperature coeff.
WEX	width exponent
RV	width dependent voltage coeff.

2.9.1 Poly2 and high resistive poly Resistor Model Features

- Modeling temperature range validity -40°C up to 180°C
- Voltage and temperature dependency in first and second order
- Width dependency model
- Device mismatch modeling
- Special RF-models are available and documented in the RF SPICE Models document.

2.9.2 Poly2 and high resistive poly Resistor Model Limitations and Restrictions

- The model is valid for L/W > 5 only
- Parasitic capacitances are included in the RPOLYXC models only.
- The extended voltage and temperature model is not supported for poly1
- Self- heating is not modeled

2.9.3 Poly2 and high resistive poly Resistor Worst Case Model

Following resistor SPICE parameters are varied within the worst case corner parameter sets:

rsh	sheet resistance (related to RPOLYX)
wd	width reduction (related to WPOLYX)

2.10 Low TC Poly Resistor Model

The voltage and temperature modeling of RPOLYZ is taken into account wih following equations:

$$RT = RnV\left[1 + TCR1\cdot(T - T_0) + TCR2\cdot(T - T_0)^2\right]$$

$$RnV = R_0\left[1 + RVL\left(\frac{V}{l}\right) + RVQ\left(\frac{V}{l}\right)^2\right]$$

$$R_0 = RSH\cdot\frac{l - LD}{w - WD} \qquad RVL = \frac{l}{w}\cdot RVLN$$

$$RVQ = \frac{1}{R_0}\cdot\left[RTH\cdot TCR1\cdot\left(\frac{l}{w}\right)^{WEX}\cdot(T - T_0) + RT0W\right]$$

RT	temperature dependent resistor
L	drawn resistor length
W	drawn resistor width
WD	width reduction parameter
LD	length reduction parameter
TCR1	linear temperature coefficient
TCR2	quadratic temperature coeff.
WEX	width exponent
RV	width dependent voltage coeff.

2.10.1 Low TC Poly Resistor Model Features

- Modeling temperature range validity -40°C up to 180°C
- Voltage and temperature dependency in first and second order
- Width dependency model
- Device mismatch modeling

2.10.2 Low TC Poly Resistor Model Limitations and Restrictions

- The model is valid for L > 3um and 0.8µm < W < 48um only
- 1/f noise modeling is not included
- Parasitic capacitances are not included in the model.
- The extended voltage and temperature model is applied for the following circuit simulators: Spectre, ELDO, HSPICE and SMARTSPICE.
- Self-heating is not modeled
- RF model is not supported.

2.10.3 Low TC Poly Resistor Model Worst Case Model

Following resistor SPICE parameters are varied within the worst case corner parameter sets:

rsh	sheet resistance
wd	width reduction
ld	length reduction
TCR1	linear temperature coefficient
TCR2	quadratic temperature coefficient

2.11 Poly and MIM Capacitor Model

The voltage and temperature modeling of CPOLY, CMIM and CPMIM is taken into account by the following equations:

Area and perimeter dependence: $C_0(A,P) = C_A * A + C_P * P$

C_0…capacitance at zero bias, C_A…area capacitance, A…area, C_P…perimeter capacitance, P…perimeter

Temperature dependence: $C(T) = C_0 * [1 + TC1 * (T - T_{nom})]$

$TC1$…linear temperature coefficient, T…temperature, T_{nom}…nominal temperature (27°C)

Voltage dependence: $C(V) = C(T) * (1 + VC1 * V + VC2 * V^2)$

$VC1$…linear voltage coefficient, $VC2$…quadratic voltage coefficient, V…applied voltage

Geometry behaviour of the quadratic voltage coefficient for MIM:

$$VC2(A/P) = d + \frac{e}{(A/P)^f}$$

A/P…area to perimeter ratio, d, e, f…fit parameters

Geometry behaviour of voltage coefficients for CPMIM:

$$VC1(A/P) = a + \frac{b}{(A/P)^c} \text{ and } VC2(A/P) = d + \frac{e}{(A/P)^f}$$

A/P…area to perimeter ratio, a, b, c, d, e, f…fit parameters

2.11.1 Poly, MIM and PMIM Capacitor Model Features

- Area and perimeter proportion
- Temperature and voltage dependency
- Area to perimeter ratio for voltage dependent modeling
- Modeling temperature range validity -40°C up to 180°C
- Device mismatch modeling

2.11.2 Poly, MIM and PMIM Capacitor Model Limitations and Restrictions

- frequency dependency is modeled in the RF model only
- parasitic capacitance is modeled in the RF model only

2.11.3 Poly, MIM and PMIM Capacitor Worst Case Model

Following capacitance SPICE parameters are varied within the worst case corner parameter sets:

$\boldsymbol{C_A}$	area capacitance (related to CPOX/CMIM/CPMIM)
$\boldsymbol{VC1, VC2}$	voltage coefficients (only for CMIM and CPMIM)

2.12 MOS Capacitor Model

2.12.1 MOS Capacitor Model Features

- Modeling of area and perimeter cap.

2.12.2 MOS Capacitor Model Limitations and Restrictions

- The MOS capacitor model is simplified to an area and perimeter gate cap and does not include any MOS transistor parasitic capacitances, voltage, temperature, noise or mismatch dependency.

2.12.3 MOS Capacitor Worst Case Model

ca area capacitance (related to COX)
cp perimeter capacitance (related to COX)

2.13 Diode Model

2.13.1 Diode Model Features

- We support a reverse diode model including area and perimeter capacitance the diode leakage current and temperature coefficient.
- Modeling temperature range validity -40°C up to 180°C

2.13.2 Diode Model Limitations and Restrictions

- Diode models are only intended for the simulation of reverse leakage current and junction capacitance. It is not recommended to use ND, PD and NWD in forward operation.
- 1/f noise modeling and mismatch modeling is not included.

2.13.3 Diode Worst Case Model

The diode model does not include any corner parameters.

2.14 Zener Diode Model

2.14.1 Diode Model Features

- A p-diffusion to n-diffusion in n-well Zener diode is available as a programmable element. It is modeled as a sub-circuit of four diodes and a voltage source.
- The model includes the parasitic n-well diode and a series resistor plus a programmable parallel resistor for zapping.

2.14.2 Diode Model Limitations and Restrictions

- The Zener diode ZD2SM24 is available as a programmable element. ZD2SM24 must not be used as a voltage reference.

2.14.3 Zener Diode Worst Case Model

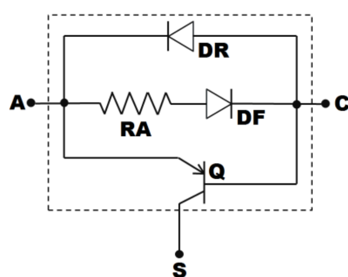
RZ zap resistor
RS seriesresistor of diode
BV reverse breakdown of "dbvt"
ISF saturation current for "dfor"
ISR saturation current for "drev"
ISR2 saturation current for "drev2"
CJ0 junction capacitor

2.15 Schottky Barrier Diode Model

For accurate modeling of the Schottky barrier diode we supply SPICE parameters for a subcircuit (Figure 2.3) including SGP bipolar transistor, two diodes and a resistor. The combination of a forward diode and an anode resistor compose the main Schottky barrier diode. The reverse diode is used to model reverse leakage current. The bipolar transistor is used to model the substrate current.

2.15.1 Schottky Barrier Diode Model Features

- In particular, the forward current and substrate current are modeled more accurately.
- Modeling temperature range validity -40 up to 125°C.
- SOAC Models: Models including Safe Operating Area Check (SOAC) are provided for simulators SPECTRE and ELDO. The models enable the interactive checking of operating conditions during circuit simulation. It is highly recommended to use those models for high voltage design application.



A/C/S	Anode/Cathode/Substrate
Q	Bipolar (SGP model)
DF	Forward Diode
DR	Reverse Diode
RA	Anode Resistor

Fig. 2.3 Sub-circuit model of the Schottky barrier diode.

2.15.2 Schottky Barrier Diode Model Limitations and Restrictions

- The model accuracy in the reverse gummel plot of the substrate bipolar is modest and it is not recommended to use the Schottky barrier diode in this bias condition.
- 1/f noise and mismatch parameters are not available for SBD5.

2.15.3 Schottky Barrier Diode Worst Case Corner Model

Following SPICE parameters are varied within the worst case corner parameter sets:

is	forward diode saturation current (related to IFW12SBD5)
rs	forward diode sheet resistance (related to IFW12SBD5)
r	anode resistance (related to IFW12SBD5)
is	reverse diode saturation current (related to IS12SBD5)
is	substrate diode saturation current (related to ISNW12SBD5)
rc	substrate resistance (related to ISNW12SBD5)
cje	anode-cathode capacitance (related to CJSBD5)
cjc	substrate capacitance (related to CJNWSBD5)

2.16 Model Feature Overview Table

Model Features / Device	Geometry scalable model	1/f Noise Model	Temp. Modeling -40 °C 125°C	WC Model	MC Model	Mismatch Model	1/f Noise Corner Model
NMOS	X	X	X*	X	X	X	X
PMOS	X	X	X*	X	X	X	X
NMOSW	X		X*	X	X	X	
PMOSW	X		X*	X	X	X	
NMOSH		X	X*	X	X		
VERT10		X	X*	X	X	X	
LAT2			X*	X	X	X	
SUBDIODE	X		X*				
WELLDIODE	X		X*				
NWD	X		X*				
NGATECAP	X						
CVAR	X		X	X	X		
RDIFFP	X		X*	X	X	X	
RDIFFN	X		X*	X	X	X	
RNWELL	X		X*	X	X	X	
RPOLY1	X	X	X	X	X	X	X
ZD2SM24			X	X	X		
RPOLY2 RPOLY2P RPOLY2PH	X	X	X*	X	X	X	X
CPOLY	X			X	X	X	
RPOLYH	X	X	X*	X	X	X	X
RPOLYZ	X		X*	X	X	X	
CMIM	X		X	X	X	X	
CPMIM	X		X	X	X	X	
NMOSM	X	X	X*	X	X	X	X
PMOSM	X	X	X*	X	X	X	X
NMOSMW	X		X*	X	X	X	
PMOSMW	X		X*	X	X	X	
NMOSL	X	X	X*	X	X	X	X
PMOSL	X	X	X*	X	X	X	X

Model Features / Device	Geometry scalable model	1/f Noise Model	Temp. Modeling -40 °C 125°C	WC Model	MC Model	Mismatch Model	1/f Noise Corner Model
NMOSHL		X	X	X	X		
NMOSML	X	X	X*	X	X	X	X
PMOSML	X	X	X*	X	X	X	X
NMOSMHL		X	X	X	X		
SBD5	X		X	X	X		

*) Temperature modeling is supported up to 180°C.

2.17 Summary of Simulation Models

Please refer to further application notes within the actual model files.

The following devices are available for design:

Core Process / Device	Device Name	Model Name	Model	Model Rev.
3.3 Volt NMOS	NMOS	modn	BSIM3v3.24 HiSIM2.5.1	4.0 1.0
3.3 Volt PMOS	PMOS	modp	BSIM3v3.24 HiSIM2.5.1	4.0 1.0
3.3 Volt waffle NMOS	NMOSW	modnw	BSIM3v3.24 subcircuit	1.0
3.3 Volt waffle PMOS	PMOSW	modpw	BSIM3v3.24 subcircuit	1.0
3.3 Volt high-voltage NMOS	NMOSH	modnh	BSIM3v3.24	4.0
Vertical PNP bipolar transistor	VERT10	vert10	Gummel-Poon	5.0
Lateral PNP bipolar transistor	LAT2	lat2	Gummel-Poon subcircuit	1.0
Diode NDIFF / PSUB	SUBDIODE	nd	diode	4.0
Diode PDIFF / NWELL	WELLDIODE	pd	diode	4.0
Diode NWELL / PSUB	NWD	nwd	diode	4.0
POLY1-DIFF capacitor	NGATECAP	ngatecap	capacitor	4.0
thin-oxide RF MOS Varactor	CVAR	cvar	BSIM3v3.24 subcircuit	4.0
PDIFF resistor	RDIFFP	rdiffp	resistor	4.0
NDIFF resistor	RDIFFN	rdiffn	resistor	4.0
NWELL resistor	RNWELL	rnwell	resistor	4.0
POLY1 resistor	RPOLY1	rpoly1	resistor	5.0
Zener diode	ZD2SM24	zd2sm24	diode subcircuit	1.0

CPOLY Module / Device	Device Name	Model Name	Model Rev.
POLY2 resistor	RPOLY2	rpoly2	5.0
POLY2 resistor	RPOLY2P	rpoly2p	1.0
CPOLY capacitor	CPOLY	cpoly	4.0

High resistive poly Module / Device	Device Name	Model Name	Model Rev.
POLY2 resistor	RPOLY2PH	rpoly2ph	1.0
POLYH resistor	RPOLYH	rpolyh	5.0

Low TC resistive Module / Device	Device Name	Model Name	Model Rev.
POLYZ resistor	RPOLYZ	rpolyz	1.0

CMIM Module / Device	Device Name	Model Name	Model Rev.
METAL2-METALC capacitor	CMIM	cmim	4.0
POLY2/METAL2-METALC capacitor	CPMIM	cpmim	1.0

5 VOLT Module / Device	Device Name	Model Name	Model	Model Rev.
5 Volt NMOS	NMOSM	modnm	BSIM3v3.24 HiSIM2.5.1	4.0 1.0
5 Volt PMOS	PMOSM	modpm	BSIM3v3.24 HiSIM2.5.1	4.0 1.0
5 Volt waffle NMOS	NMOSMW	modnmw	BSIM3v3.24 subcircuit	1.0
5 Volt waffle PMOS	PMOSMW	modpmw	BSIM3v3.24 subcircuit	1.0

Low VT Module / Device	Device Name	Model Name	Model	Model Rev.
Low VT 3.3 V NMOS	NMOSL	modnl	BSIM3v3.24 HiSIM2.5.1	5.0 1.0
Low VT 3.3 V PMOS	PMOSL	modpl	BSIM3v3.24 HiSIM2.5.1	5.0 1.0
Low VT 3.3 V high-voltage NMOS	NMOSHL	modnhl	BSIM3v3.24	4.0
Low VT 5 V NMOS	NMOSML	modnml	BSIM3v3.24 HiSIM2.5.1	5.0 1.0
Low VT 5 V PMOS	PMOSML	modpml	BSIM3v3.24 HiSIM2.5.1	5.0 1.0
Low VT 5 V high-voltage NMOS	NMOSMHL	modnmhl	BSIM3v3.24	4.0

Schottky Barrier Diode Module / Device	Device Name	Model Name	Model	Model Rev.
Schottky barrier diode	SBD5	sbd5	Gummel-Poon subcircuit	2.0

Note: Minor changes of the simulation models might be generated due to continuous improvement of device and circuit simulation. Minor changes of models are described within the actual model data files and within the intranet ams AG.

2.18 Circuit Simulators and Models

The models are supported and qualified for the specified simulator revision. Previous simulator versions are also supported, for detailed questions please contact us at support@ams.com.

Simulator	MOSFET-Model		
	BSIM3v3.24	HiSIM2.5.1	Monte Carlo & Matching
Spectre	MMSIM12	MMSIM12	MMSIM12
Eldo	2011.2		
HSPICE	2009.9		
ADSsim	2009		
Smash	4.3.5 (level 8)		
Smartspice	2.6.4.R		

The following models are supported for all simulators mentioned above:

Bipolar transistors: SPICE Gummel-Poon
Diodes : D level 1
Resistors : R / JFET level 1
Capacitors : C

Updates of model revision:
http://asic.ams.com/hitkit/parameters/index.html

Updates of netlist format:
http://asic.ams.com/hitkit/circuit_sim/netlist_format.html

Updates of simulation parameters/download area:
http://asic.ams.com/download/parameters.html

3 Characteristic Curves

3.1 Introduction

This section contains characteristic curves for MOS transistors, CMOS compatible bipolar transistors, resistors and capacitors which have been measured on typical wafers. The circuit simulation parameters for the typical mean process condition (refer to section "2. Simulation Model") have been extracted from the same wafers.

The characteristic curves are intended for checking the correct implementation of the SPICE models and SPICE parameters in a particular simulator. In addition, the accuracy of the different models is compared and the quality of the parameter extraction is shown.

MOS Transistors

Output characteristics, transfer characteristics, transconductance (gm), outputconductance (gds) and capacitance-voltage characteristics of several transistor geometries are shown. The figures contain the measured and the simulated characteristics for the BSIM3v3.24 and for the HiSIM2.5.1 model.

Waffle Transistors

Output and transfer characteristics of several transistor geometries are shown. The figures contain the measured and the simulated drain current for the BSIM3v3.24 sub-circuit model.

HV MOS Transistors

Output and transfer characteristics of several transistor geometries are shown. The figures contain the measured and the simulated drain current modeled with the BSIM3v3.24 sub-circuit model.

Bipolar Transistors

Gummel plots and current gain plots of vertical and lateral bipolar transistors for several collector voltages are shown. The figures contain the measured and the simulated current for the SPICE Gummel-Poon model.

Well Resistors

Resistance characteristics of several resistor geometries for several bulk voltages are shown. The figures contain the measured and the simulated resistance for the SPICE JFET model.

Poly1-Poly2 and Metal2-MetalC capacitors

The figures show the linearity of the CPOLY and CMIM capacitance at several temperatures.

Schottky Barrier Diode

The figures show the anode and substrate current at different substrate voltages.

3.2 MOS Transistor Characteristics

3.2.1 3.3V MOS Transistor Characteristics

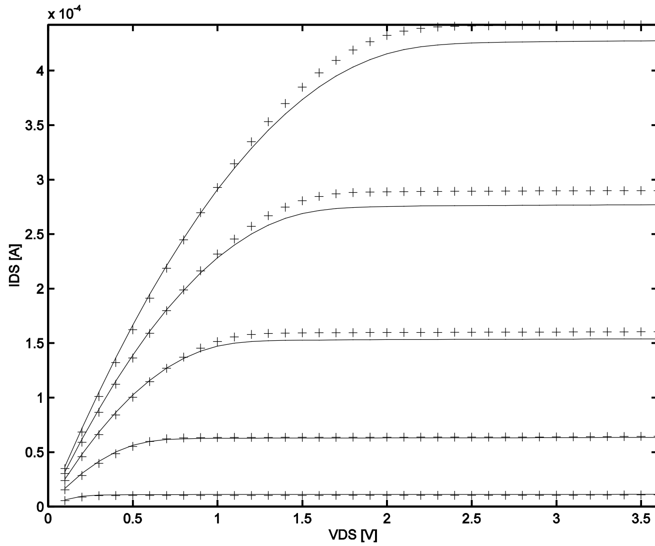


Fig.3.1 **NMOS** output characteristic of a typical wafer. W/L = 10/10, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

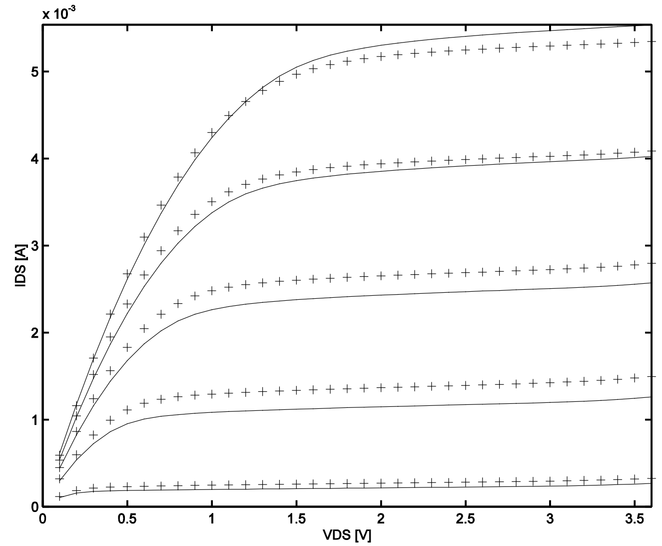


Fig. 3.2 **NMOS** output characteristic of a typical wafer. W/L = 10/0.35, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

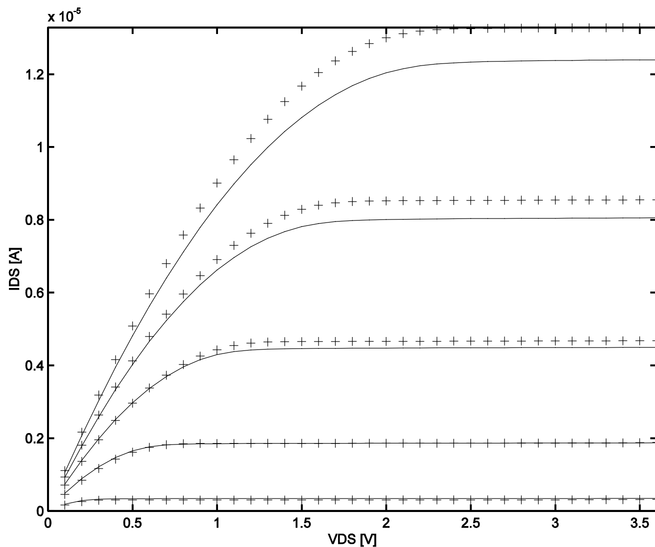


Fig. 3.3 **NMOS** output characteristic of a typical wafer. W/L = 0.4/10, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

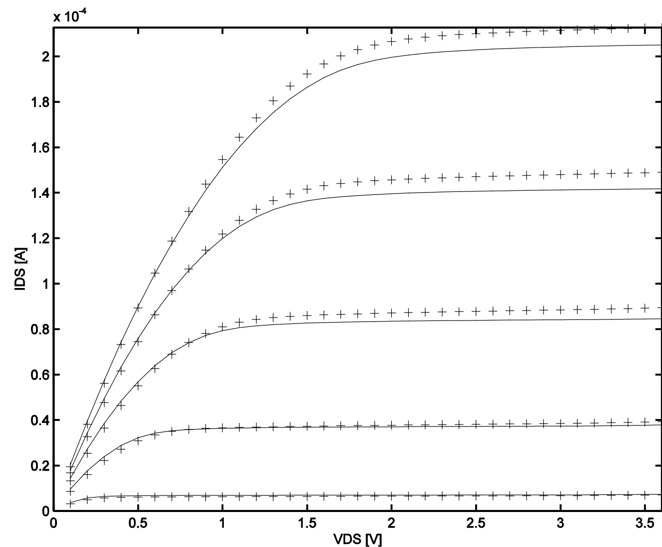


Fig. 3.4 **NMOS** output characteristic of a typical wafer. W/L = 0.8/1.0, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

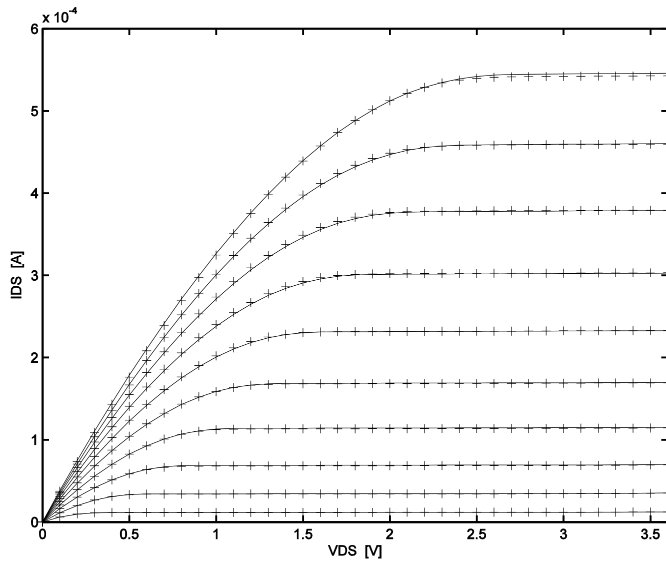


Fig.3.5 **NMOS** output characteristic of a typical wafer. W/L = 10/10, VGS=0.9,1.2,1.5,1.8,2.1,2.4,2.7,3.0,3.3,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

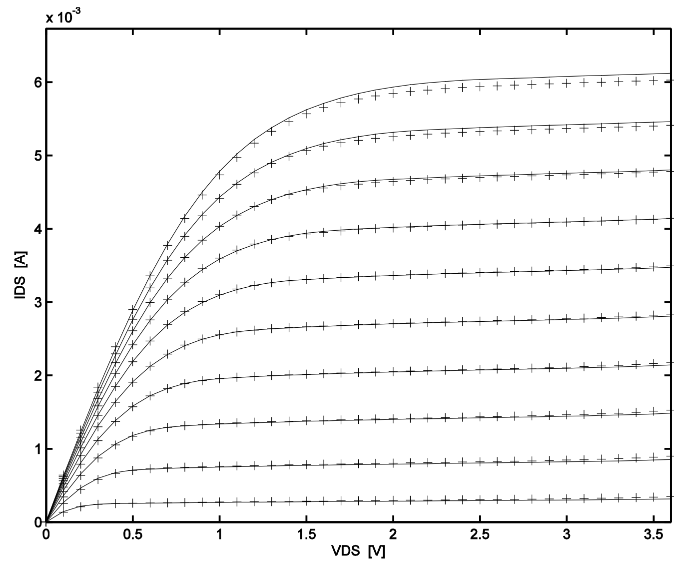


Fig. 3.6 **NMOS** output characteristic of a typical wafer. W/L = 10/0.35, VGS=0.9,1.2,1.5,1.8,2.1,2.4,2.7,3.0,3.3,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

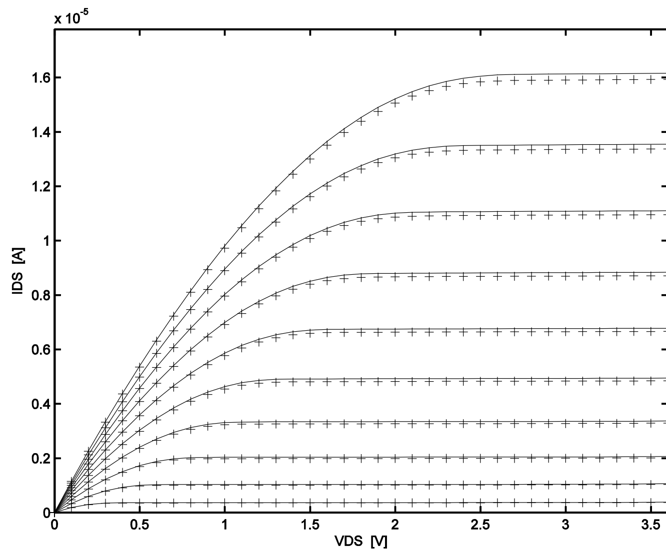


Fig. 3.7 **NMOS** output characteristic of a typical wafer. W/L = 0.36/10, VGS=0.9,1.2,1.5,1.8,2.1,2.4,2.7,3.0,3.3,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

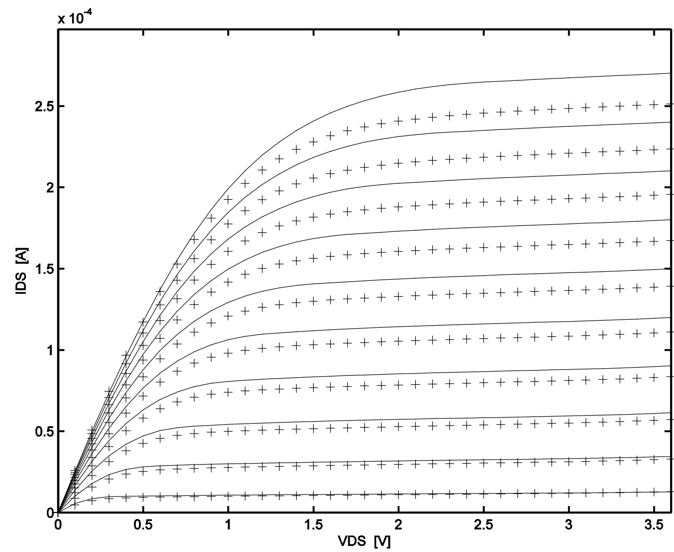


Fig. 3.8 **NMOS** output characteristic of a typical wafer. W/L = 0.36/0.35, VGS=0.9,1.2,1.5,1.8,2.1,2.4,2.7,3.0,3.3,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

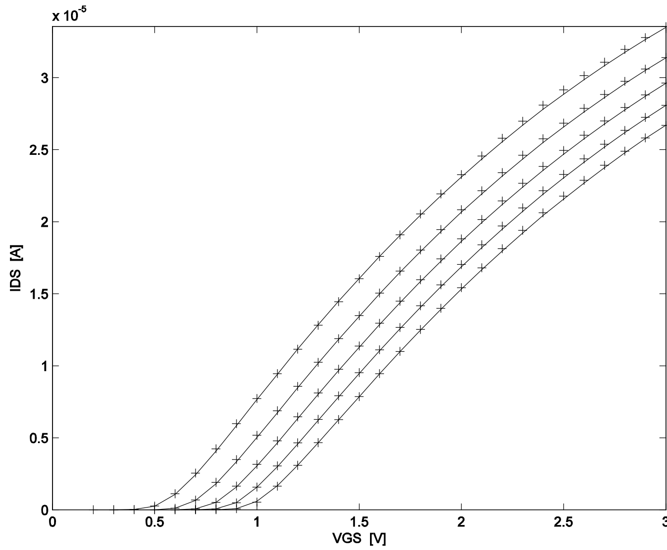


Fig. 3.10 **NMOS** transfer characteristic of a typical wafer. W/L = 10/10,
VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

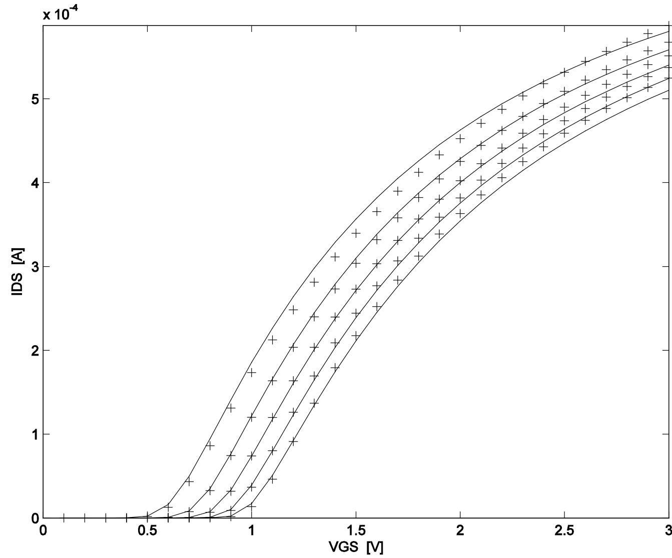


Fig. 3.11 **NMOS** transfer characteristic of a typical wafer. W/L = 10/0.35,
VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

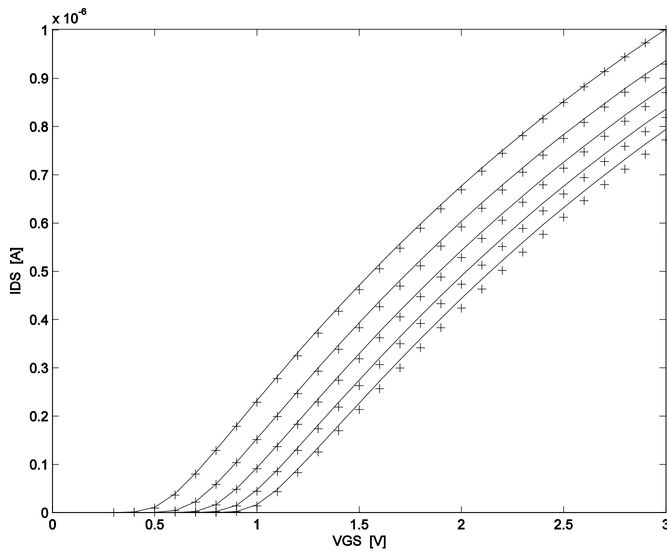


Fig. 3.13 **NMOS** transfer characteristic of a typical wafer. W/L = 0.36/10,
VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

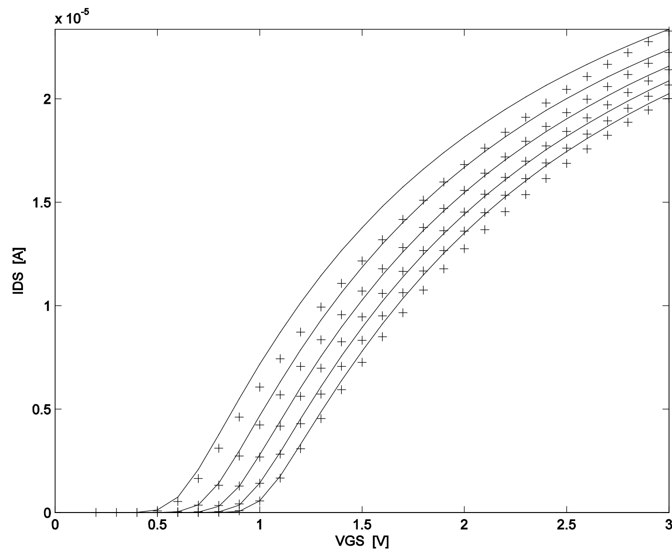


Fig. 3.14 **NMOS** transfer characteristic of a typical wafer. W/L = 0.36/0.35,
VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

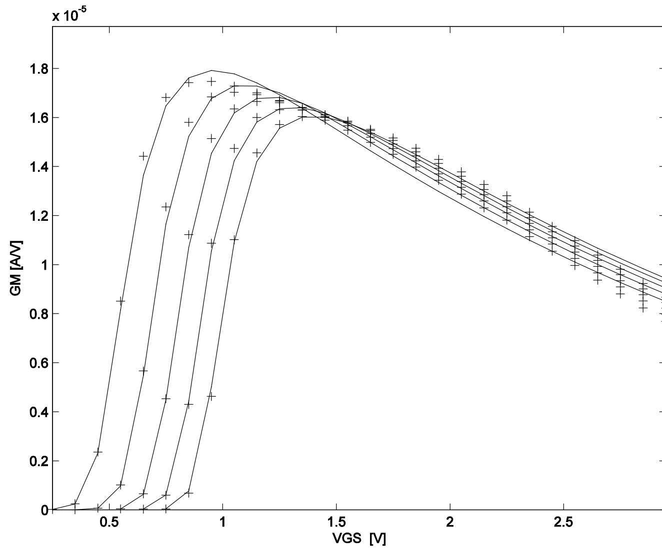


Fig. 3.16 **NMOS** Gm characteristic of a typical wafer. W/L = 10/10,
VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

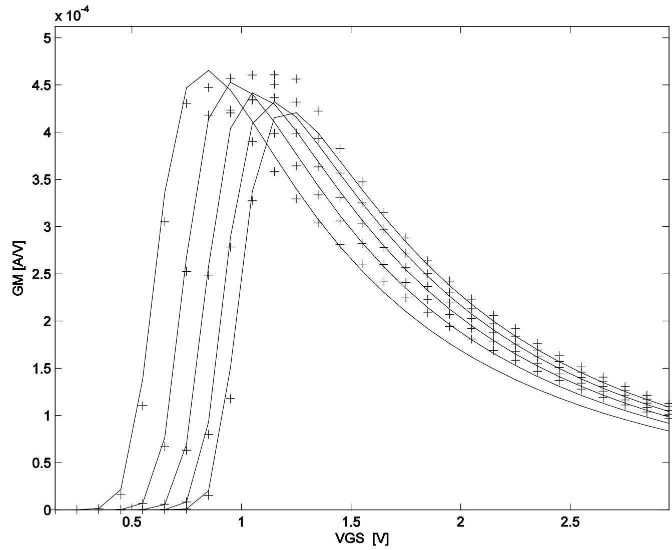


Fig. 3.17 **NMOS** Gm characteristic of a typical wafer. W/L = 10/0.35,
VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

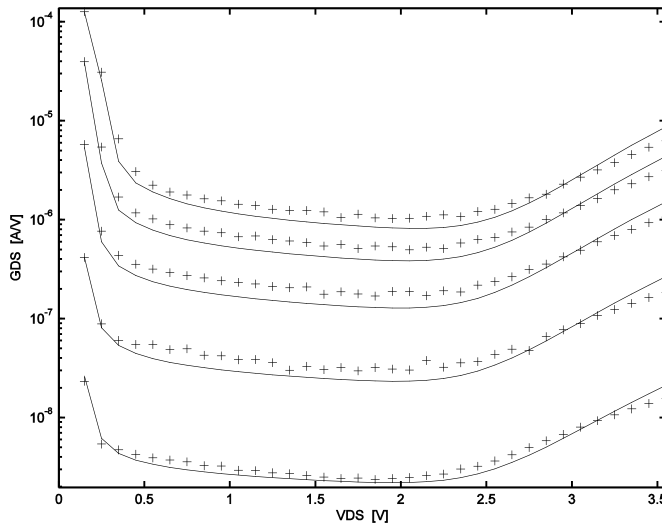


Fig. 3.18 **NMOS** Gds characteristic of a typical wafer. W/L = 10/1.2,
VGS=0.4,0.5,0.6,0.7,0.8 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

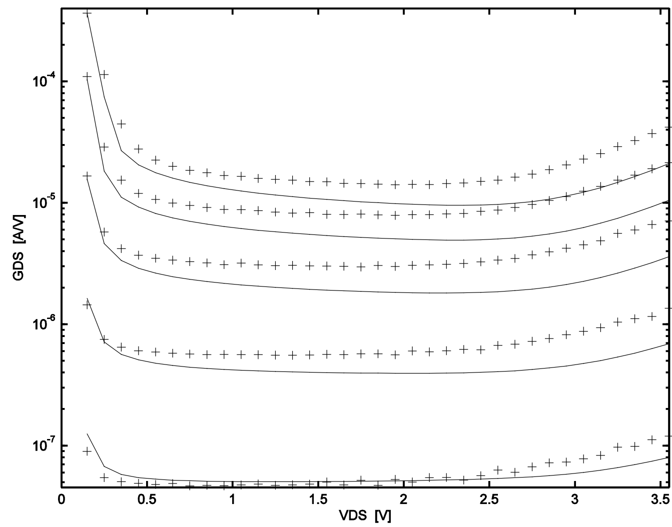


Fig. 3.19 **NMOS** Gds characteristic of a typical wafer. W/L = 10/0.35,
VGS=0.4,0.5,0.6,0.7,0.8 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

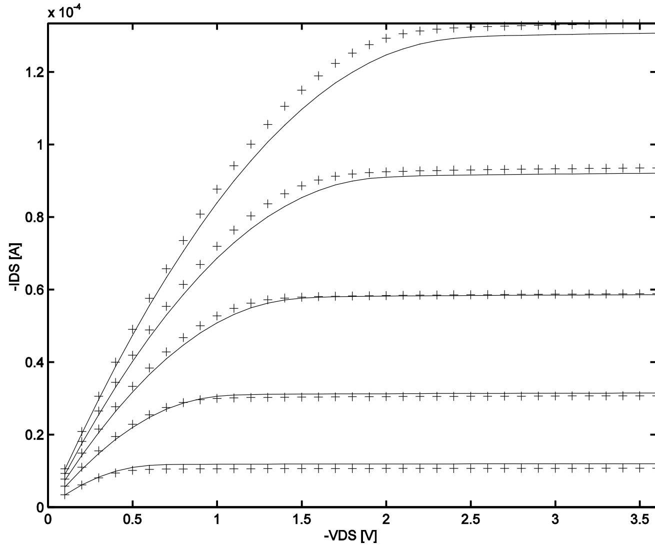


Fig. 3.20 **PMOS** output characteristic of a typical wafer. W/L = 10/10, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

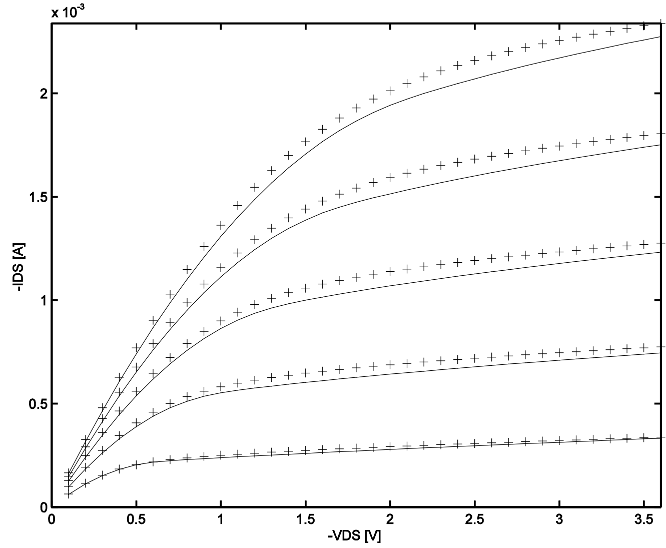


Fig. 3.21 **PMOS** output characteristic of a typical wafer. W/L = 10/0.35, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

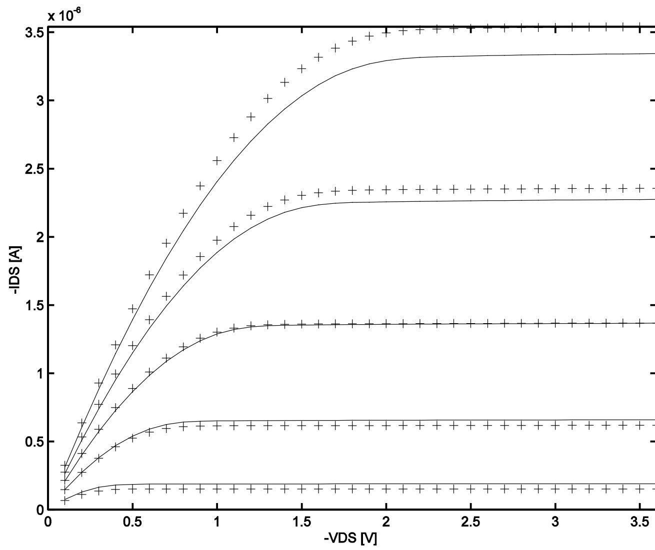


Fig. 3.23 **PMOS** output characteristic of a typical wafer. W/L = 0.4/10, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

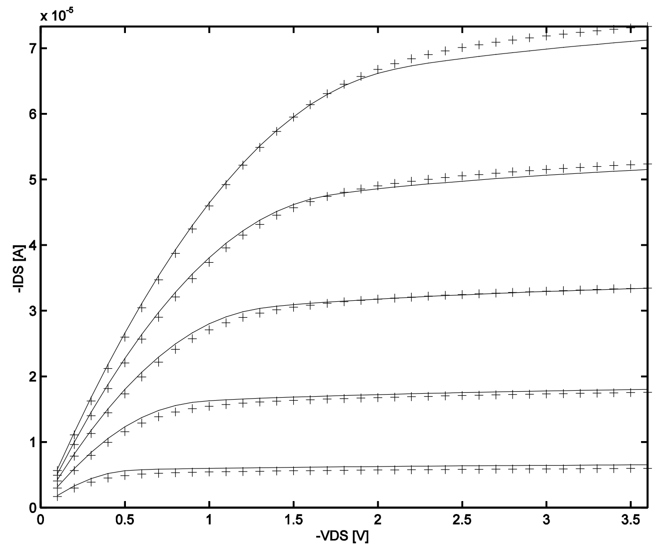


Fig. 3.24 **PMOS** transfer characteristic of a typical wafer. W/L = 0.8/1.0, VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V + = measured, — = BSIM3v3 model

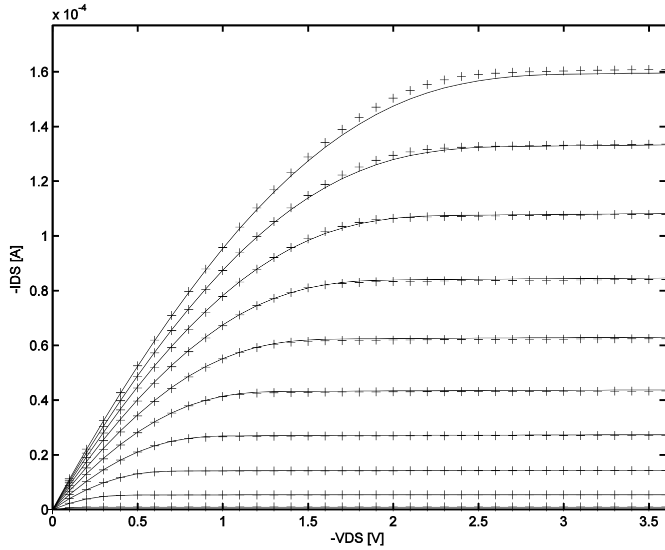


Fig. 3.26 **PMOS** output characteristic of a typical wafer. W/L = 10/10, VGS=-0.9,-1.2,-1.5,-1.8,-2.1,-2.4,-2.7,-3.0,-3.3,-3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

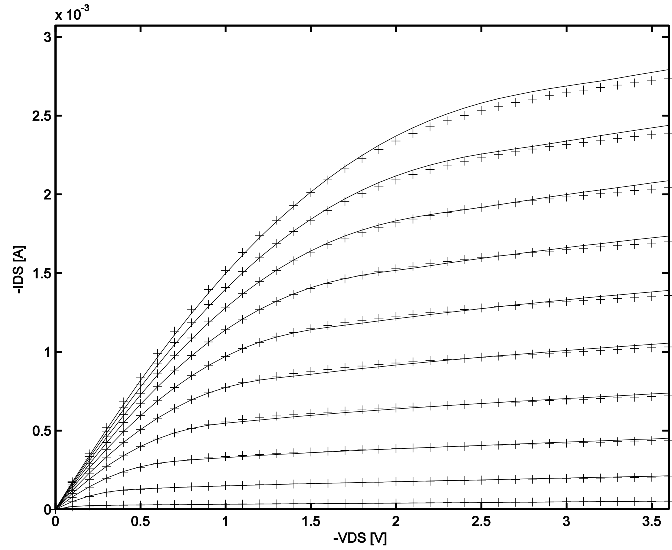


Fig. 3.27 **PMOS** output characteristic of a typical wafer. W/L = 10/0.35, VGS=-0.9,-1.2,-1.5,-1.8,-2.1,-2.4,-2.7,-3.0,-3.3,-3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

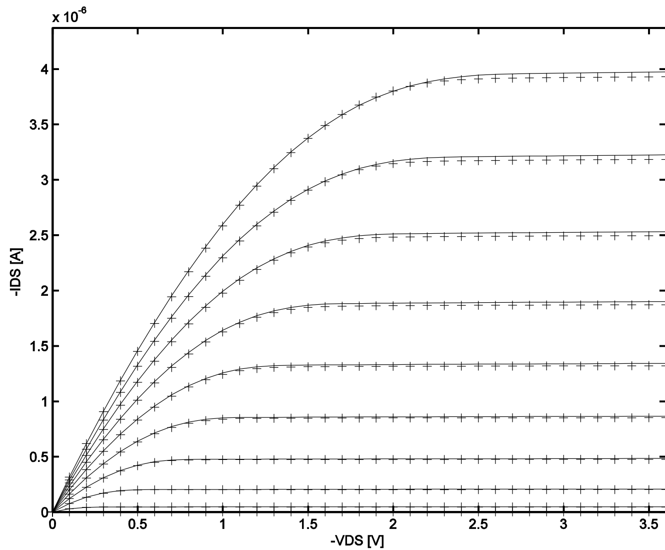


Fig. 3.29 **PMOS** output characteristic of a typical wafer. W/L = 0.36/10, VGS=-0.9,-1.2,-1.5,-1.8,-2.1,-2.4,-2.7,-3.0,-3.3,-3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

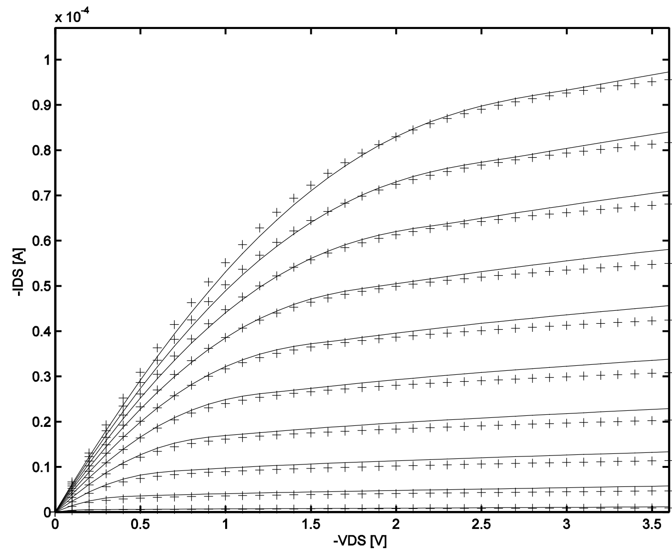


Fig. 3.30 **PMOS** transfer characteristic of a typical wafer. W/L = 0.36/0.35, VBS =-0.9,-1.2,-1.5,-1.8,-2.1,-2.4,-2.7,-3.0,-3.3,-3.6 V, VDS = -0.1V + = measured, — = HiSIM2.5.1 model

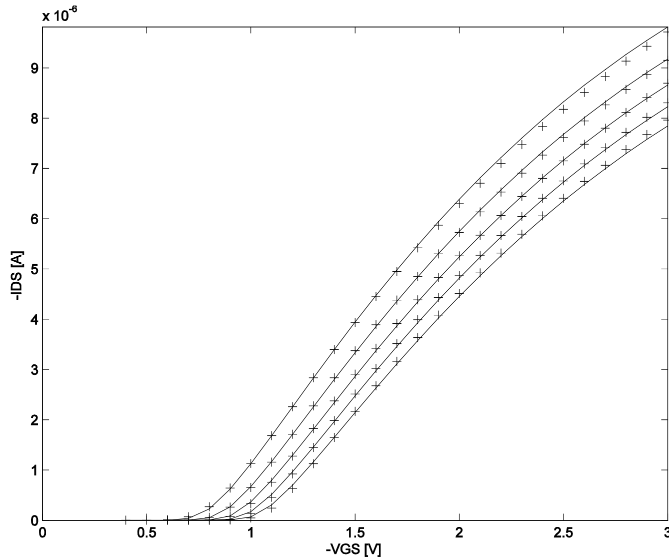


Fig. 3.32 **PMOS** transfer characteristic of a typical wafer. W/L = 10/10, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

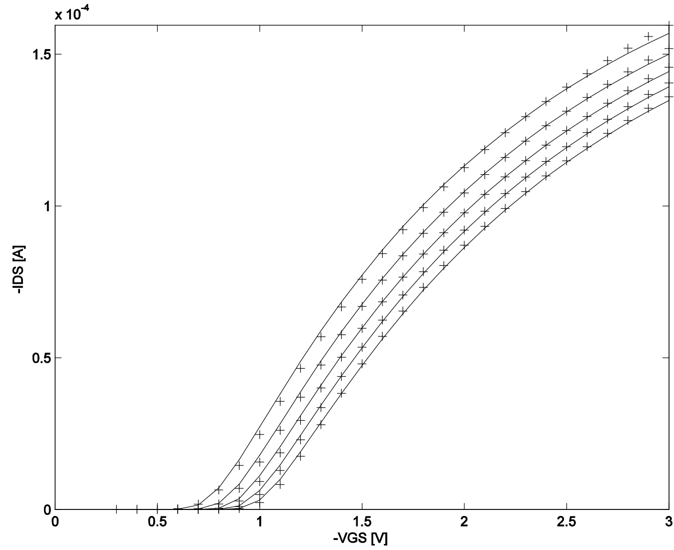


Fig. 3.33 **PMOS** transfer characteristic of a typical wafer. W/L = 10/0.35, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

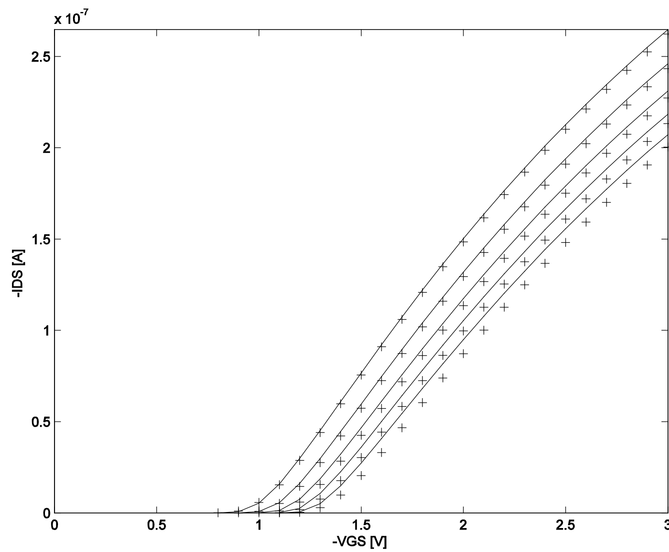


Fig. 3.35 **PMOS** transfer characteristic of a typical wafer. W/L = 0.36/10, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

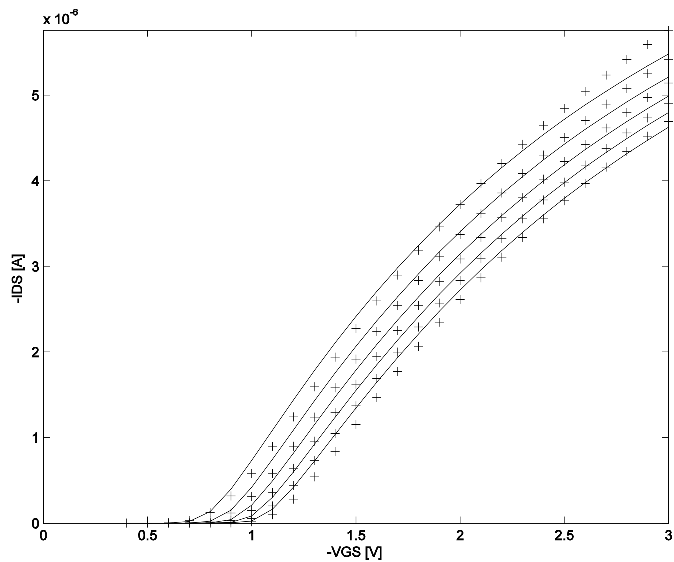


Fig. 3.36 **PMOS** output characteristic of a typical wafer. W/L = 0.36/0.35, VGS=0,0.5,1.0,1.5,2.0 V; VDS = -0.1 V,
+ = measured, — = HiSIM2.5.1 model

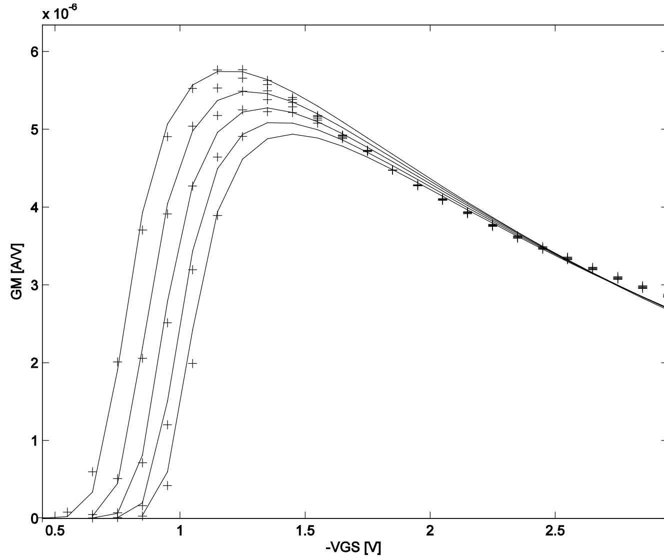


Fig. 3.38 **PMOS** Gm characteristic of a typical wafer. W/L = 10/10,
VBS =0,0.5,1.0,1.5,2.0 V, VDS =- 0.1 V
+ = measured, — = HiSIM2.5.1 model

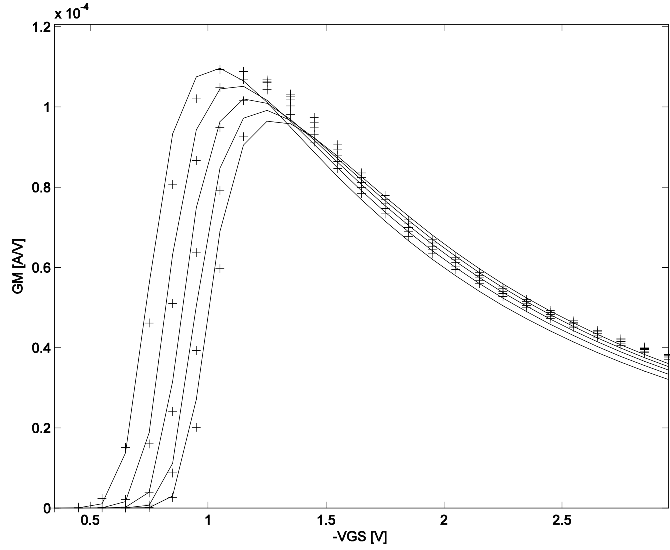


Fig. 3.39 **PMOS** Gm characteristic of a typical wafer. W/L = 10/0.35,
VBS =0,0.5,1.0,1.5,2.0 V, VDS =- 0.1 V
+ = measured, — = HiSIM2.5.1 model

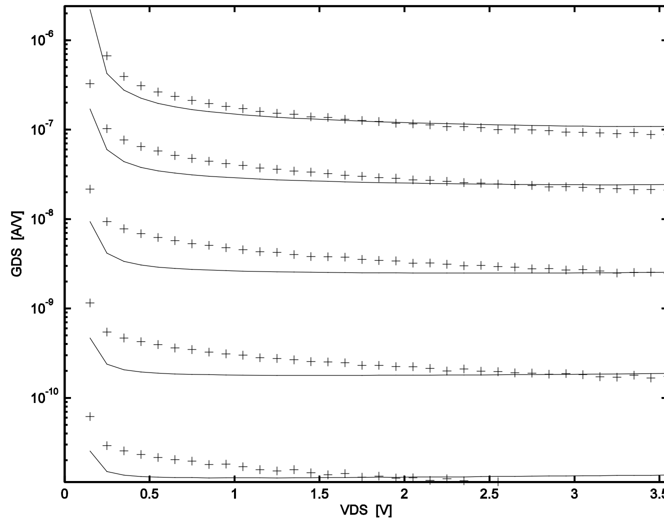


Fig. 3.40 **PMOS** Gds characteristic of a typical wafer. W/L = 10/1.2,
VGS=-0.4,-0.5,-0.6,-0.7,-0.8 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

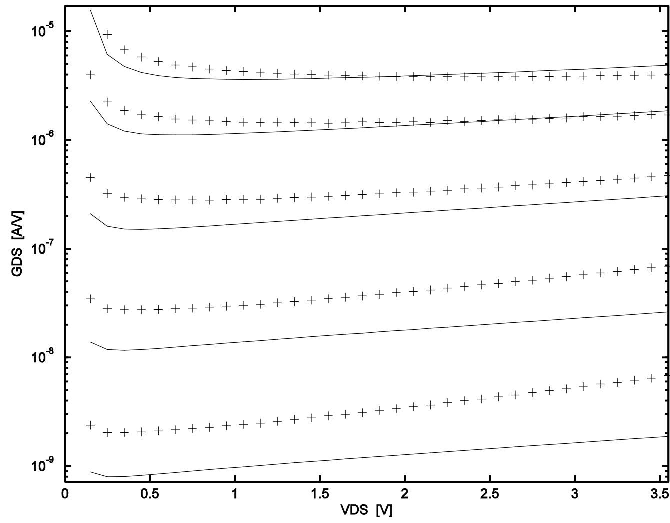


Fig. 3.41 **PMOS** Gds characteristic of a typical wafer. W/L = 10/0.35,
VGS=-0.4,-0.5,-0.6,-0.7,-0.8 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

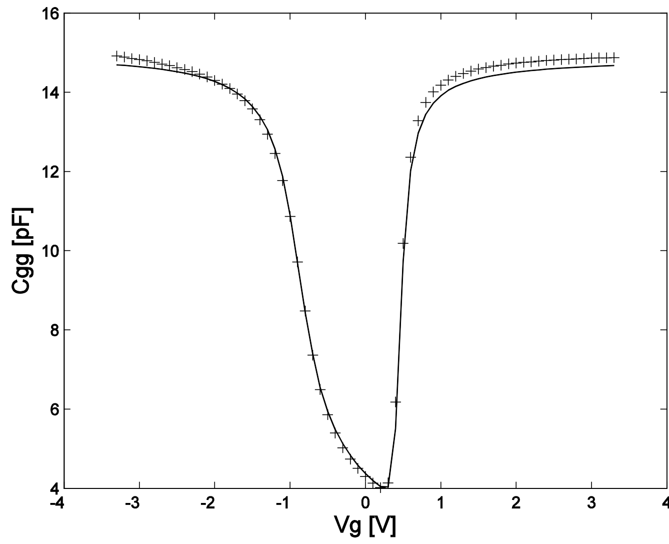


Fig. 3.42 **NMOS** total gate capacitance of a typical wafer. W/L = 40/80,
+ = measured, — = HiSIM2.5.1 model

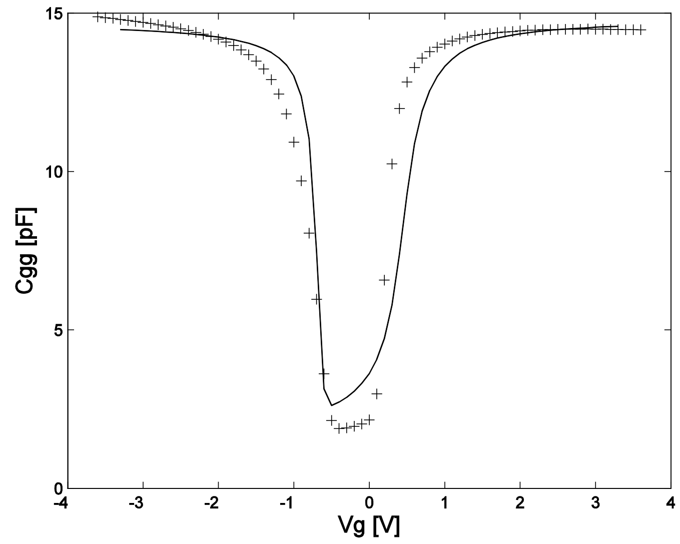


Fig. 3.43 **PMOS** total gate capacitance of a typical wafer. W/L = 40/80,
+ = measured, — = HiSIM2.5.1 model

3.2.2 3.3V Waffle Transistor Characteristics

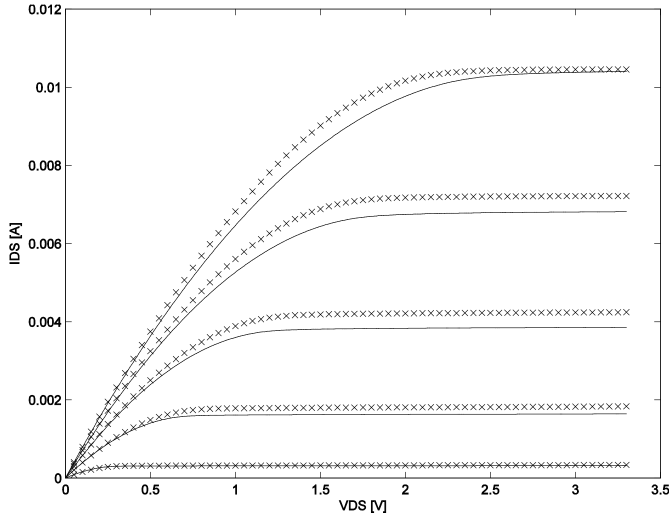


Fig. 3.45 **NMOSW** output characteristic of a typical wafer. W/L = 64/3, VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V
+ = measured, — = BSIM3v3 sub-circuit model

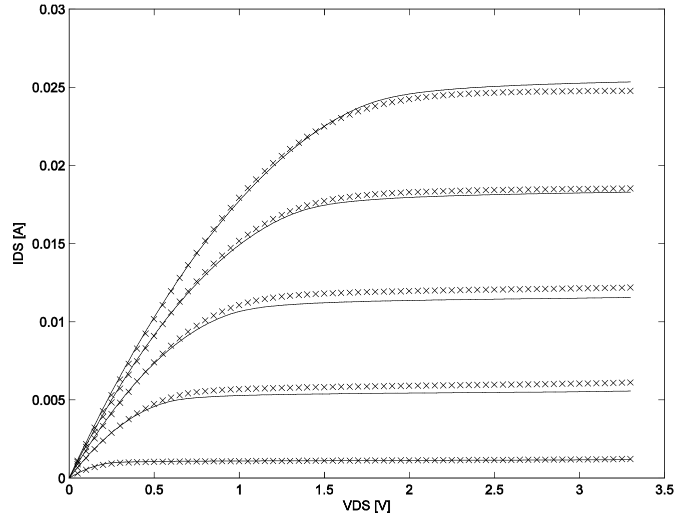


Fig. 3.46 **NMOSW** output characteristic of a typical wafer. W/L = 64/0.5, VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V
+ = measured, — = BSIM3v3 sub-circuit model

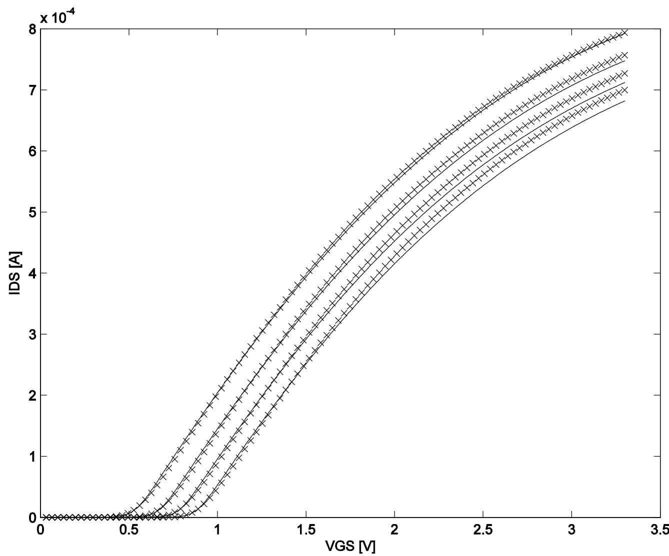


Fig. 3.47 **NMOSW** transfer characteristic of a typical wafer. W/L = 64/3, VBS =0,-0.5,-1.0,-1.5 V, VDS = 0.1 V
+ = measured, — = BSIM3v3 sub-circuit model

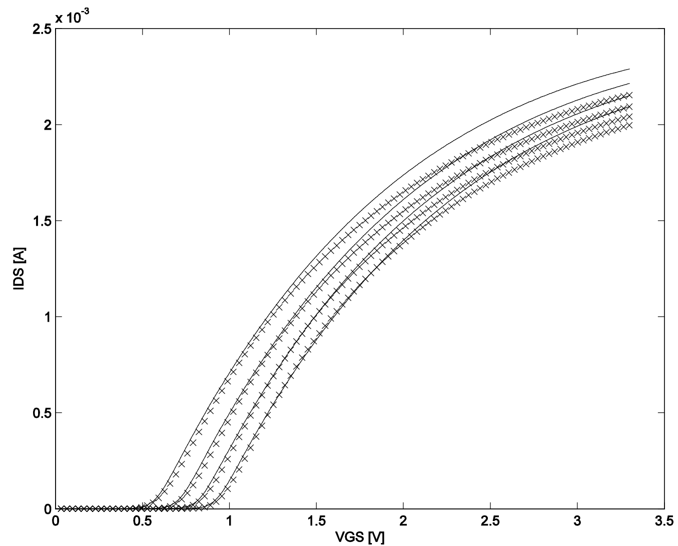


Fig. 3.48 **NMOSW** transfer characteristic of a typical wafer. W/L = 64/0.5, VBS =0,-0.5,-1.0,-1.5 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

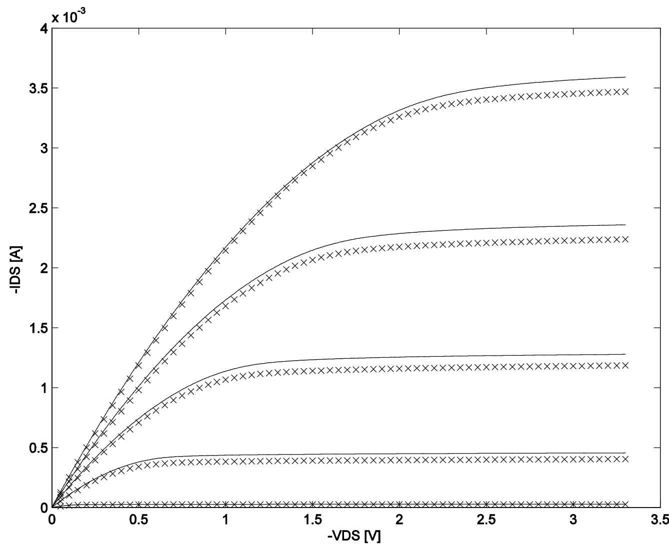


Fig. 3.49 **PMOSW** output characteristic of a typical wafer. W/L = 64/3, VGS = -0.9,-1.5,-2.1,-2.7,-3.3 V, VBS = 0 V
+ = measured, —— = BSIM3v3 sub-circuit model

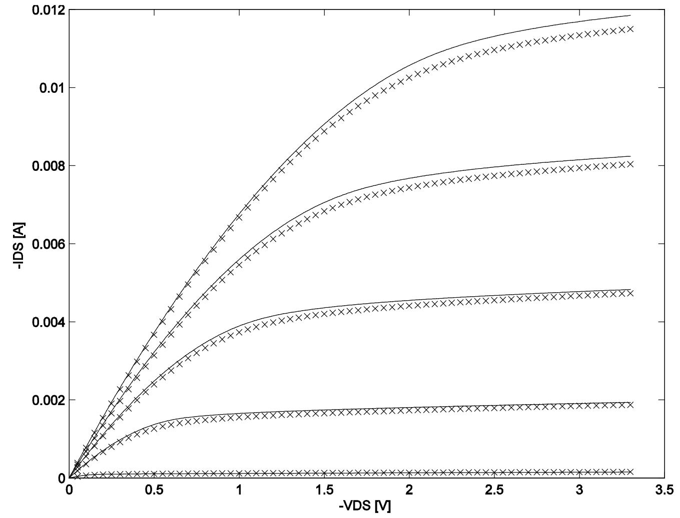


Fig. 3.50 **PMOSW** output characteristic of a typical wafer. W/L = 64/0.5, VGS = -0.9,-1.5,-2.1,-2.7,-3.3 V, VBS = 0 V
+ = measured, —— = BSIM3v3 sub-circuit model

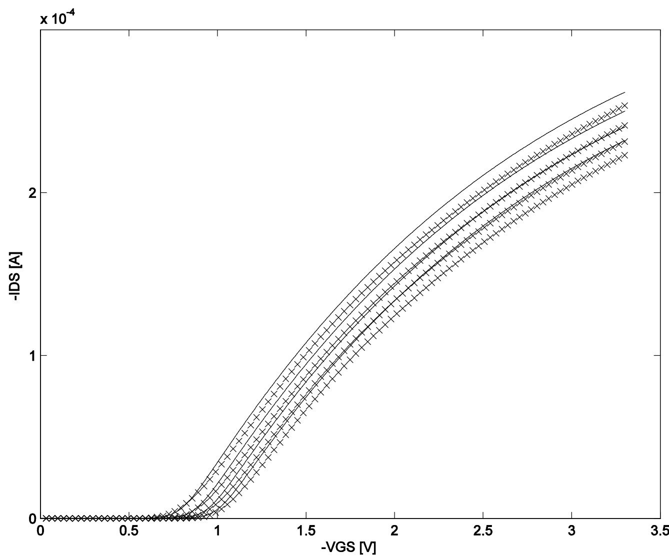


Fig. 3.51 **PMOSW** transfer characteristic of a typical wafer. W/L = 64/3, VBS =0,0.5,1.0,1.5 V, VDS = -0.1 V
+ = measured, —— = BSIM3v3 sub-circuit model

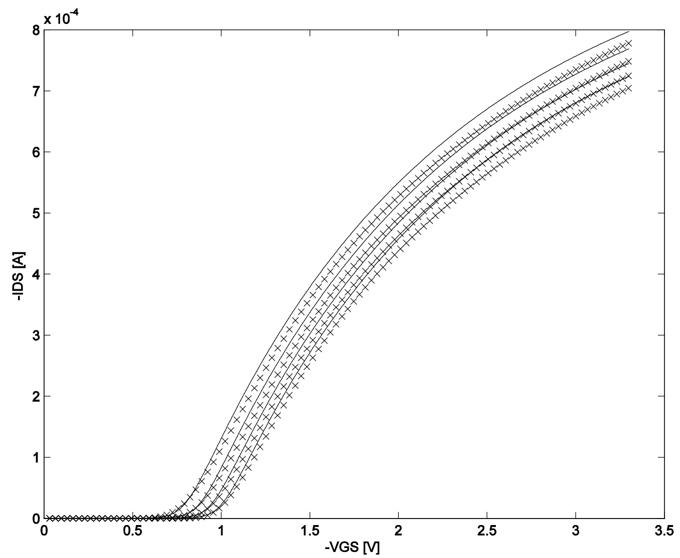


Fig. 3.52 **PMOSW** transfer characteristic of a typical wafer. W/L = 64/0.5, VBS =0,0.5,1.0,1.5 V, VDS = -0.1 V
+ = measured, —— = HiSIM2.5.1 model

3.2.3 3.3V HV-MOS Transistor Characteristics

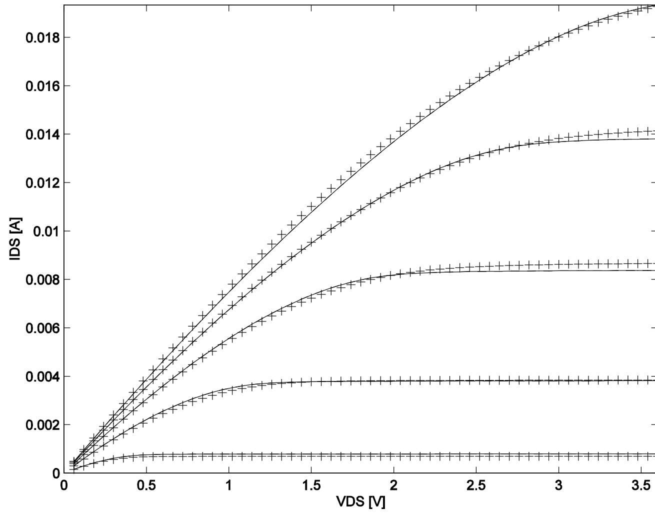


Fig. 3.53 **NMOSH** output characteristic of a typical wafer. W/L = 100/3, VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V
+ = measured, —— = BSIM3v3 model

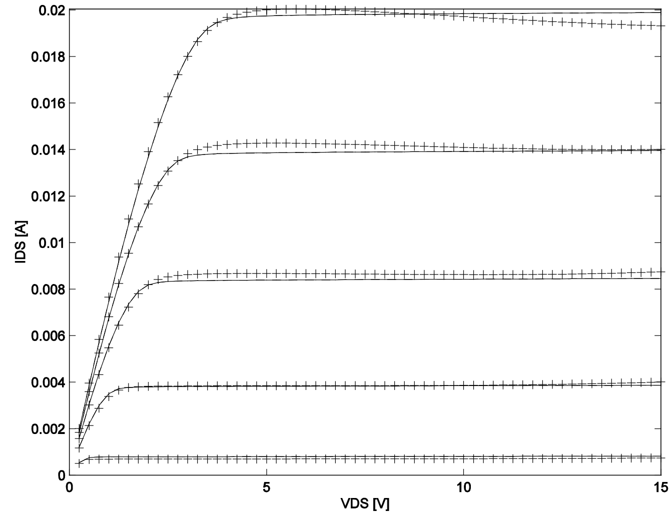


Fig. 3.54 **NMOSH** output characteristic of a typical wafer. W/L = 100/3, VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V
+ = measured, —— = BSIM3v3 model

3.2.4 5V MOS Transistor Characteristics

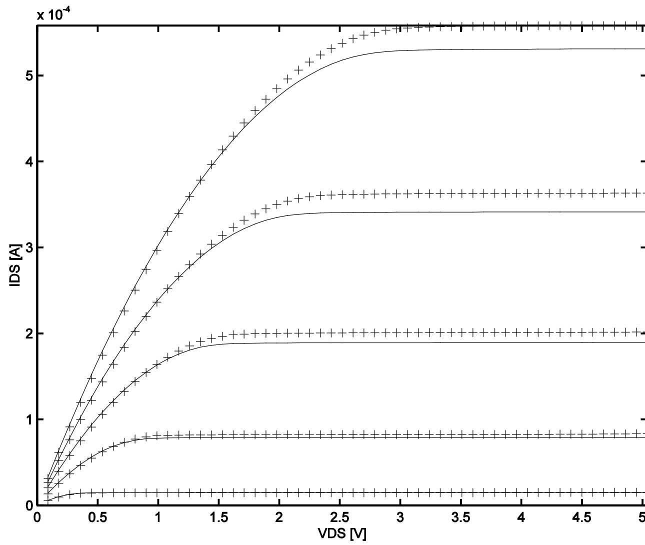


Fig. 3.55 **NMOSM** output characteristic of a typical wafer. W/L = 10/10,
VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

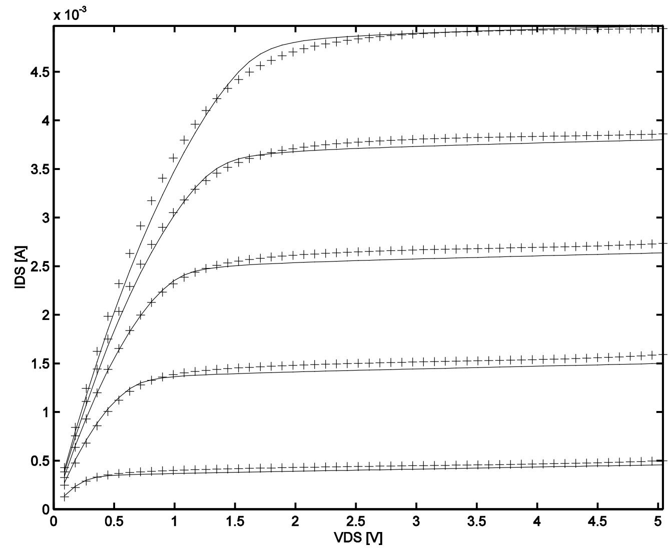


Fig. 3.56 **NMOSM** output characteristic of a typical wafer. W/L = 10/0.5,
VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

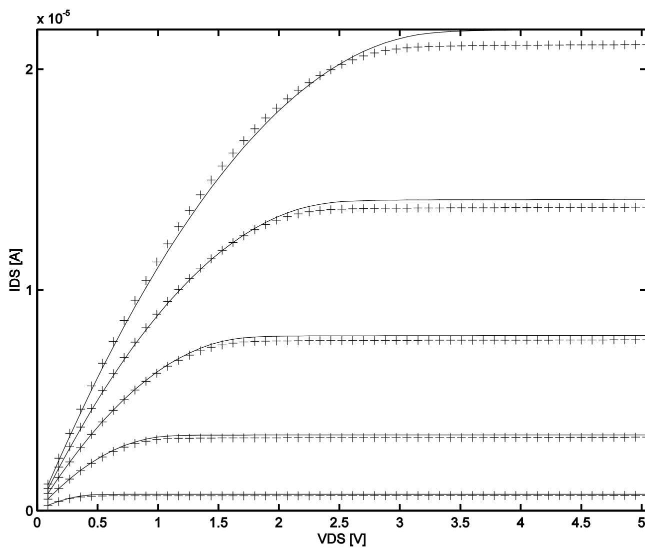


Fig. 3.57 **NMOSM** output characteristic of a typical wafer. W/L = 0.4/10,
VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

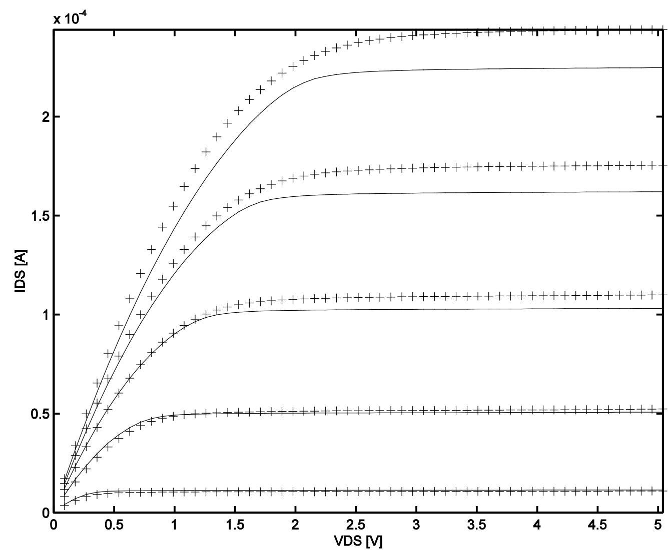


Fig. 3.58 **NMOSM** output characteristic of a typical wafer. W/L = 0.8/1.0,
VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

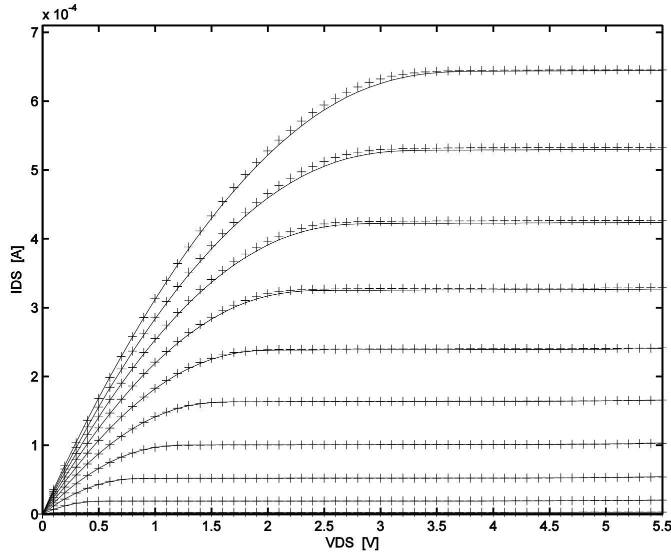


Fig. 3.60 **NMOSM** output characteristic of a typical wafer. W/L = 10/10,
VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

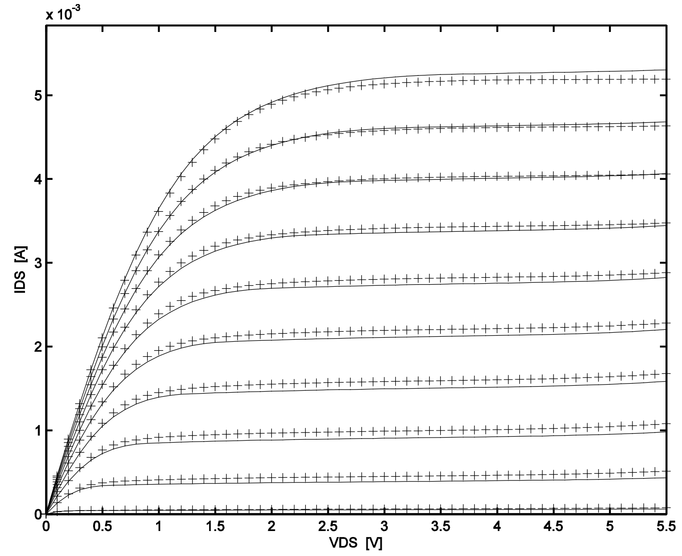


Fig. 3.61 **NMOSM** output characteristic of a typical wafer. W/L = 10/0.5,
VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

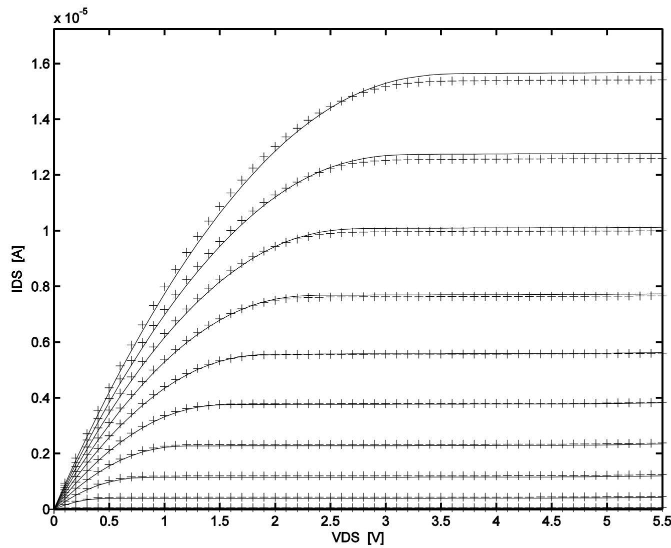


Fig. 3.62 **NMOSM** output characteristic of a typical wafer. W/L = 0.36/10,
VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

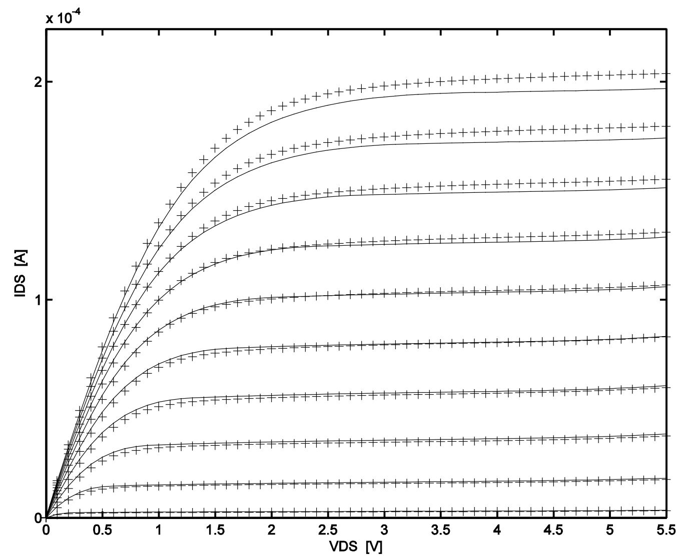


Fig. 3.63 **NMOSM** output characteristic of a typical wafer. W/L = 0.36/0.5,
VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

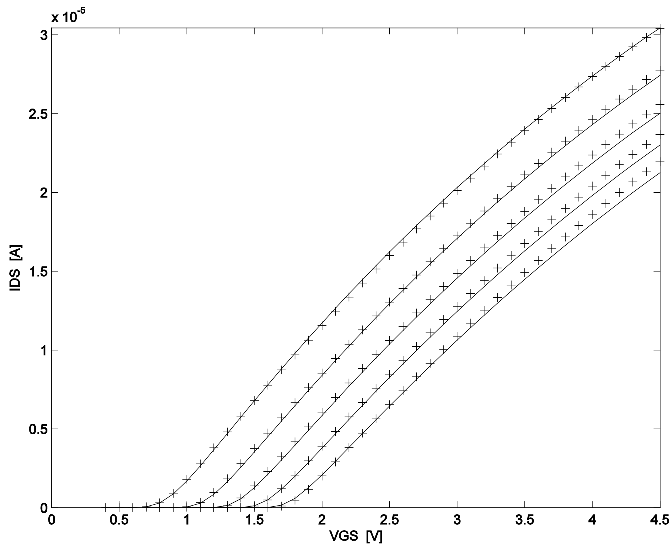


Fig. 3.65 **NMOSM** transfer characteristic of a typical wafer. W/L = 10/10, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

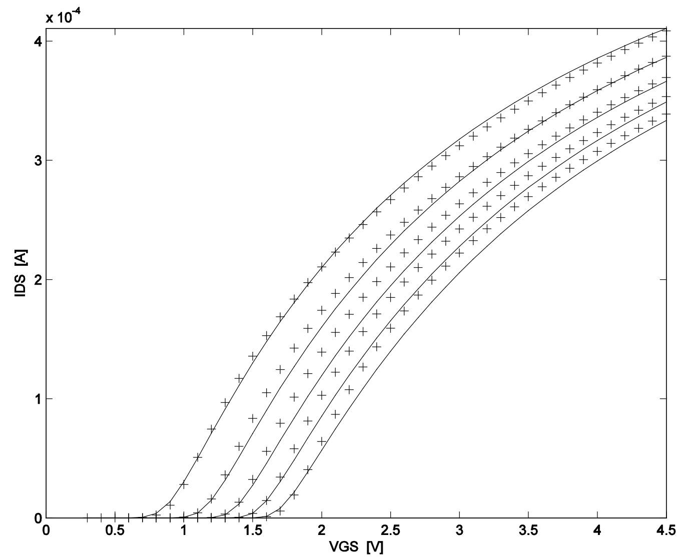


Fig. 3.66 **NMOSM** transfer characteristic of a typical wafer. W/L = 10/0.5, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

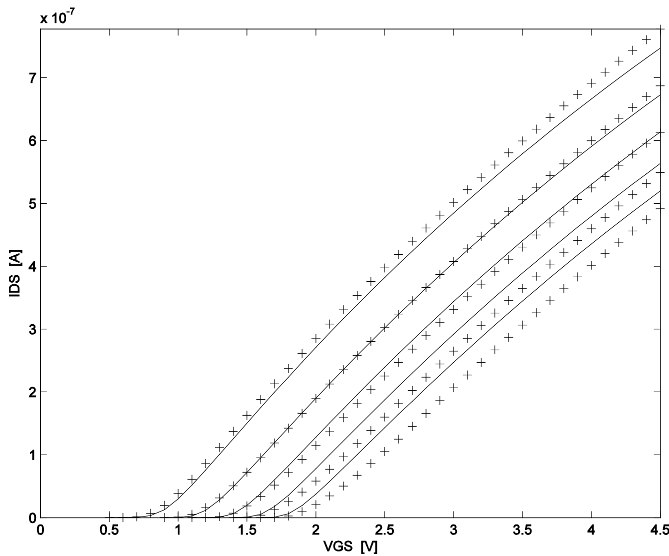


Fig. 3.68 **NMOSM** transfer characteristic of a typical wafer. W/L = 0.36/10, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

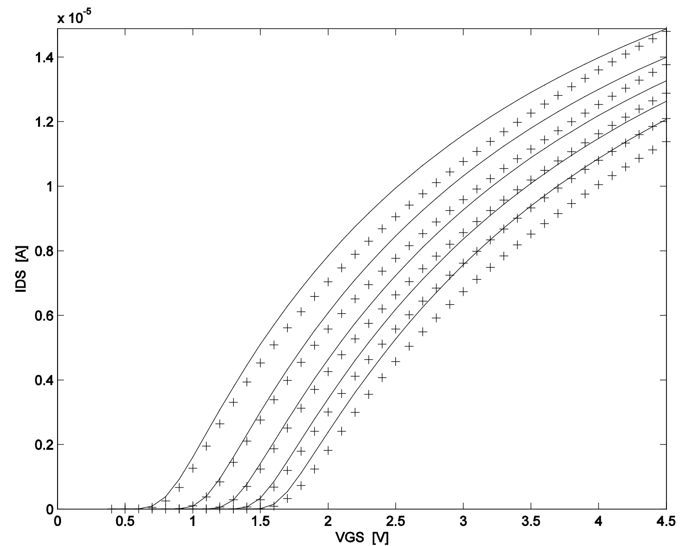


Fig. 3.69 **NMOSM** transfer characteristic of a typical wafer. W/L = 0.36/0.5, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

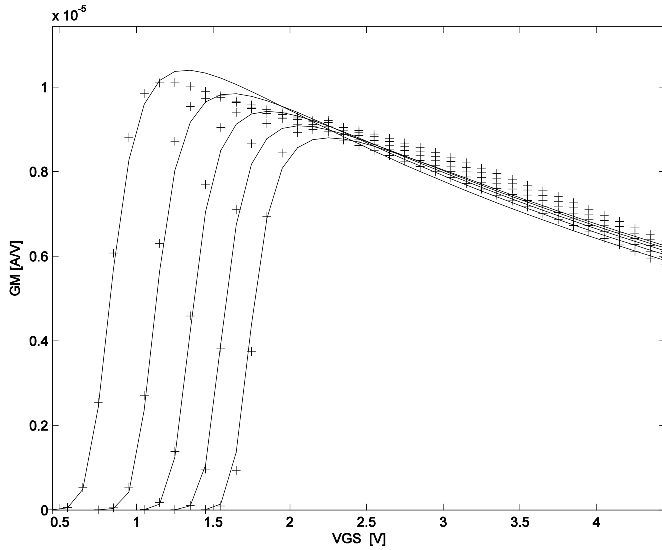


Fig. 3.71 **NMOSM** Gm characteristic of a typical wafer. W/L = 10/10, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

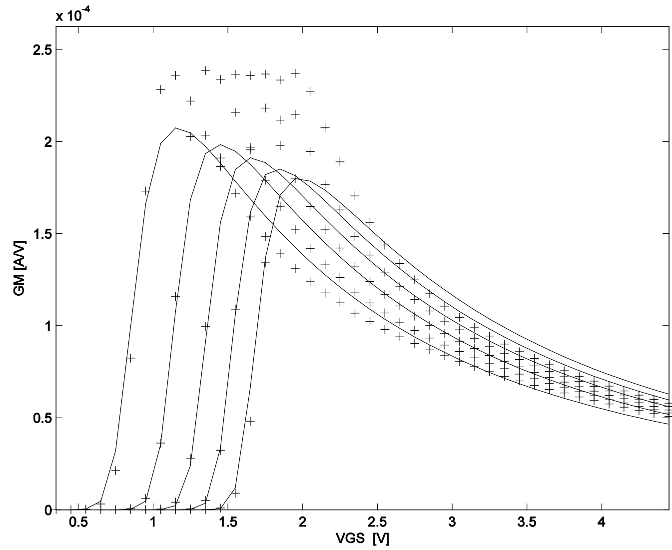


Fig. 3.72 **NMOSM** Gm characteristic of a typical wafer. W/L = 10/0.5, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

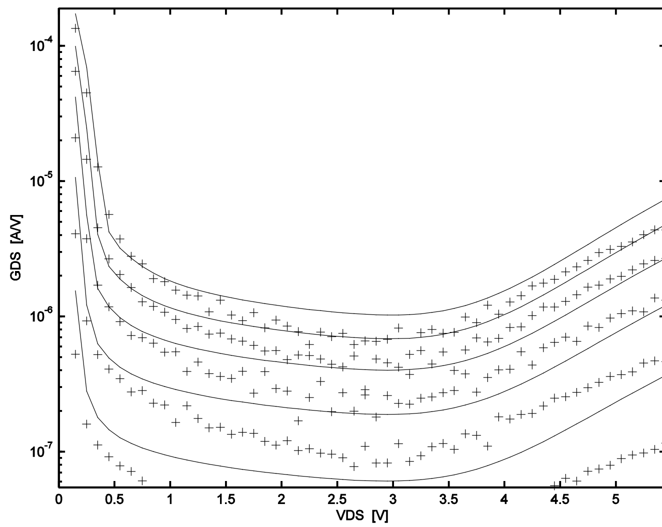


Fig. 3.73 **NMOSM** Gds characteristic of a typical wafer. W/L = 10/1.2, VGS=0.8,0.9,1.0,1.1,1.2 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

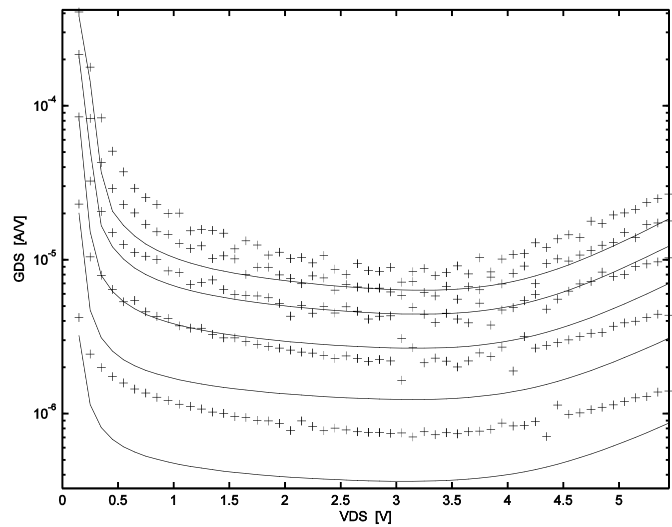


Fig. 3.74 **NMOSM** Gds characteristic of a typical wafer. W/L = 10/0.5, VGS=0.8,0.9,1.0,1.1,1.2 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

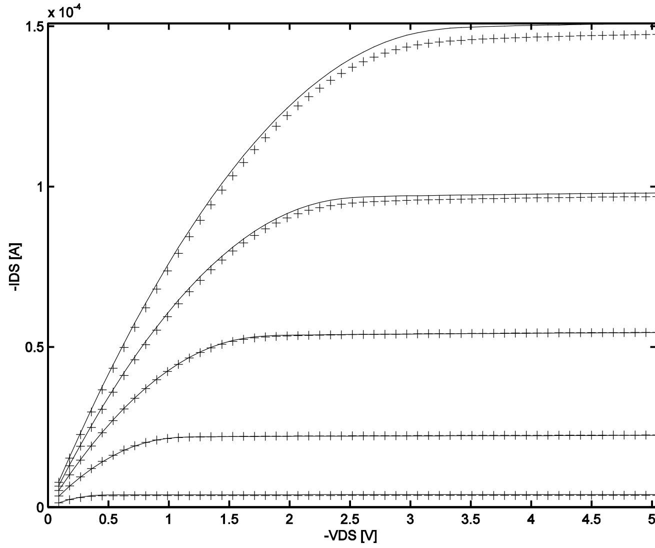


Fig. 3.75 **PMOSM** output characteristic of a typical wafer. W/L = 10/10,
VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

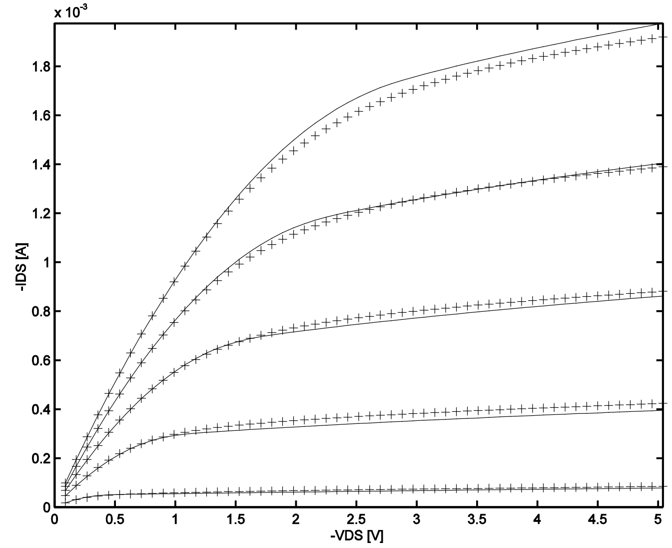


Fig. 3.76 **PMOSM** output characteristic of a typical wafer. W/L = 10/0.5,
VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

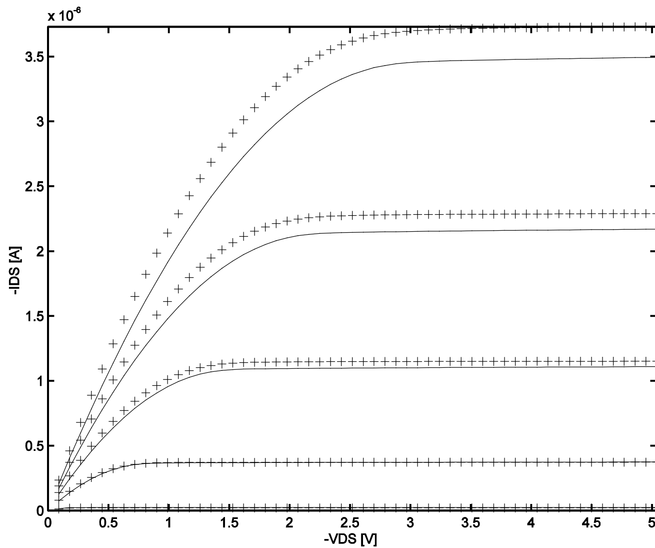


Fig. 3.78 **PMOSM** output characteristic of a typical wafer. W/L = 0.4/10,
VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

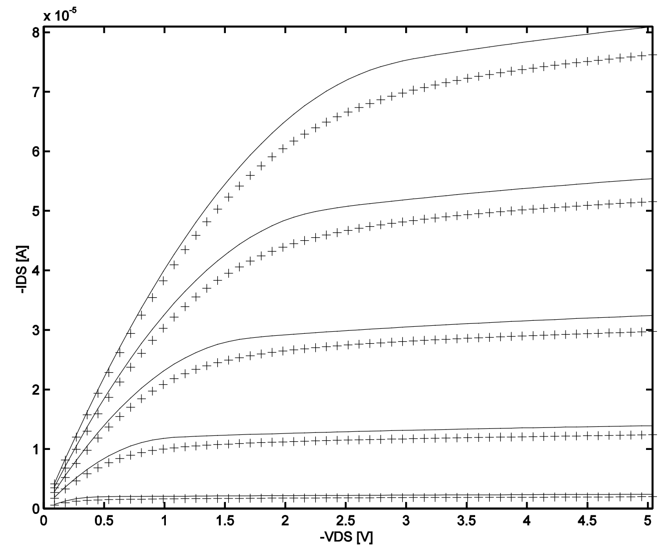


Fig. 3.79 **PMOSM** output characteristic of a typical wafer. W/L = 0.8/1.0,
VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

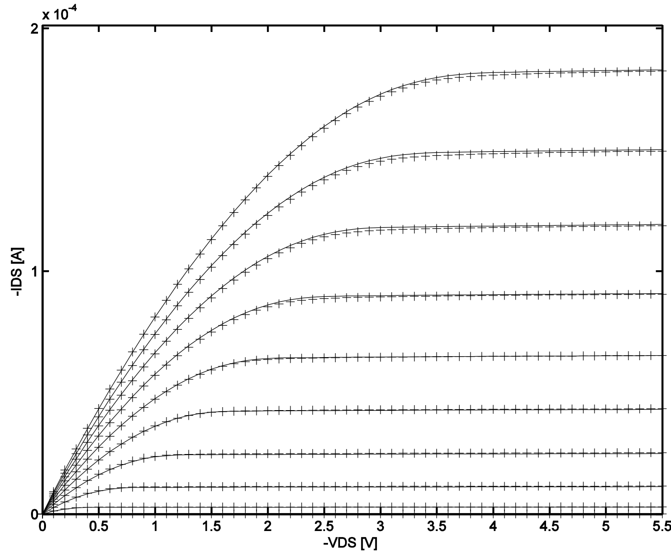


Fig. 3.81 **PMOSM** output characteristic of a typical wafer. W/L = 10/10,
VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

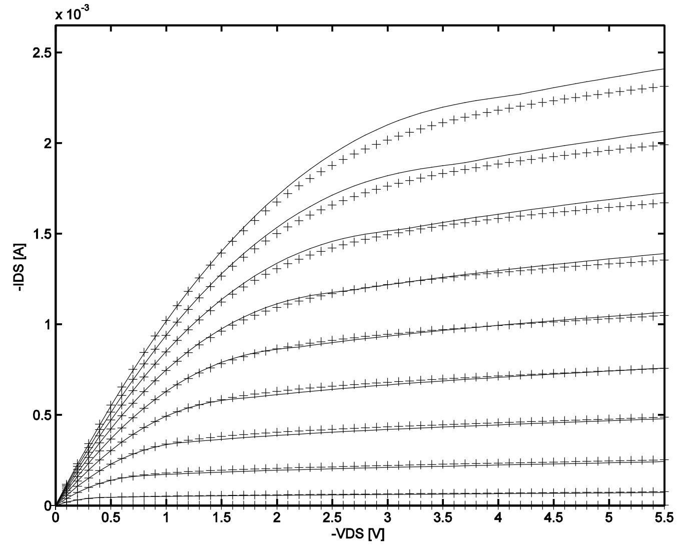


Fig. 3.82 **PMOSM** output characteristic of a typical wafer. W/L = 10/0.5,
VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

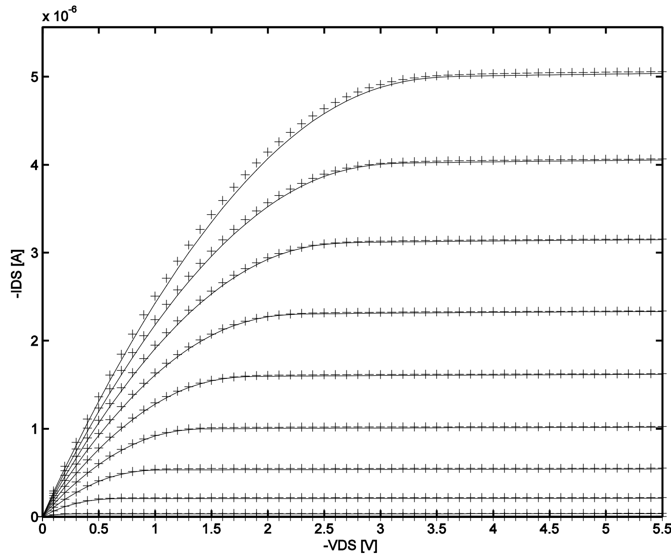


Fig. 3.84 **PMOSM** output characteristic of a typical wafer. W/L = 0.36/10,
VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

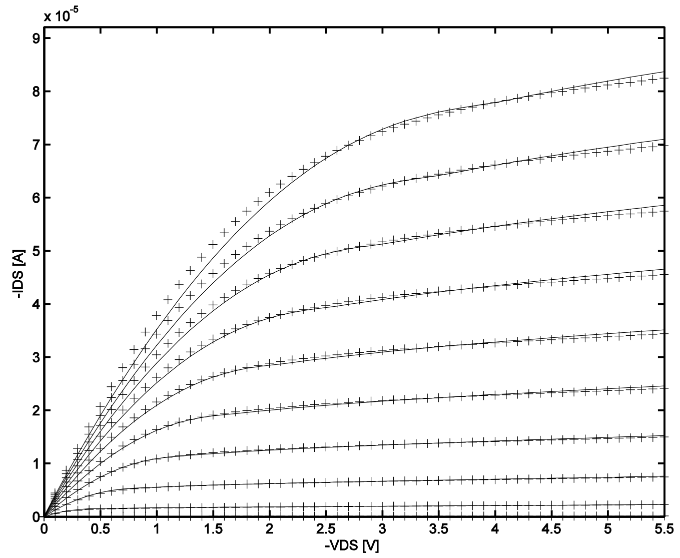


Fig. 3.85 **PMOSM** output characteristic of a typical wafer. W/L = 0.36/0.5,
VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

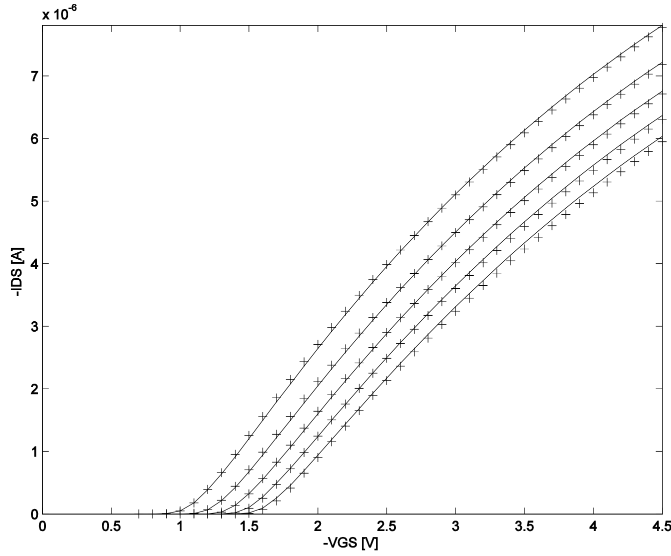


Fig. 3.87 **PMOSM** transfer characteristic of a typical wafer. W/L = 10/10,
VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

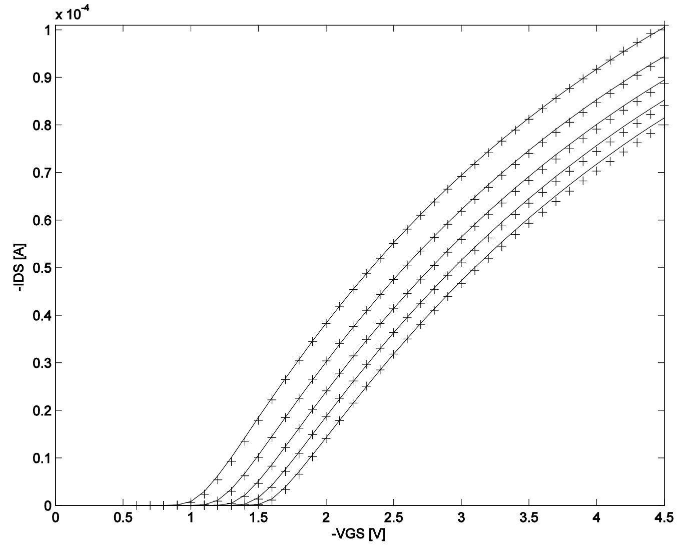


Fig. 3.88 **PMOSM** transfer characteristic of a typical wafer. W/L = 10/0.5,
VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

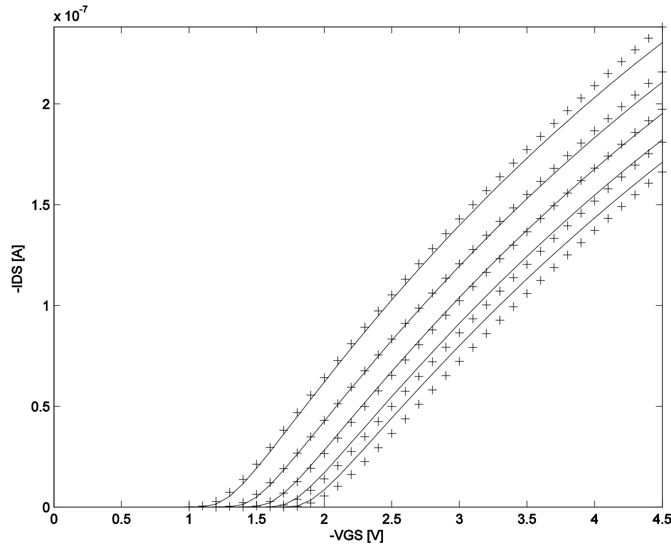


Fig. 3.90 **PMOSM** transfer characteristic of a typical wafer. W/L = 0.36/10,
VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

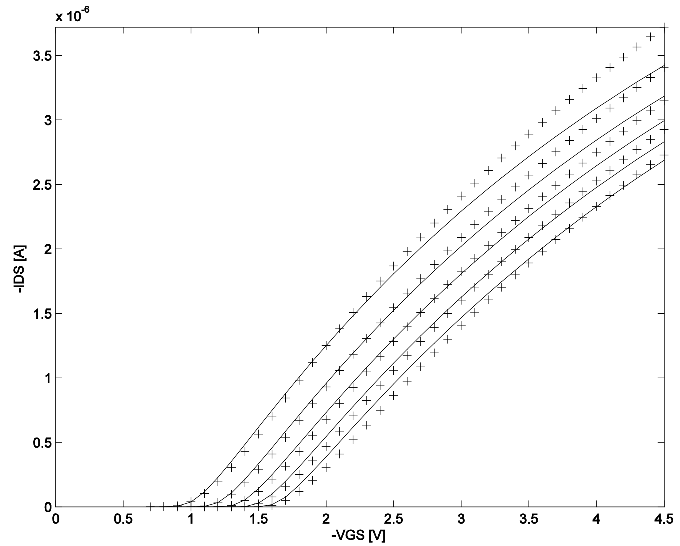


Fig. 3.91 **PMOSM** transfer characteristic of a typical wafer. W/L = 0.36/0.5,
VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

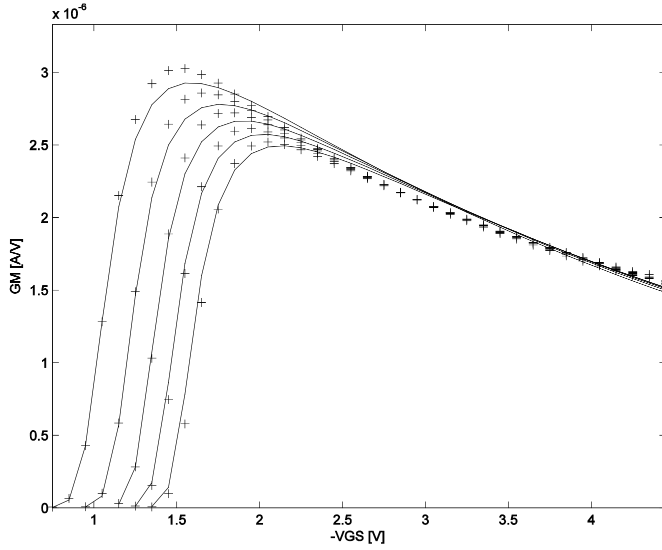


Fig. 3.93 **PMOSM** Gm characteristic of a typical wafer. W/L = 10/10,
VBS =0,0.6,1.2,1.8,2.4 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

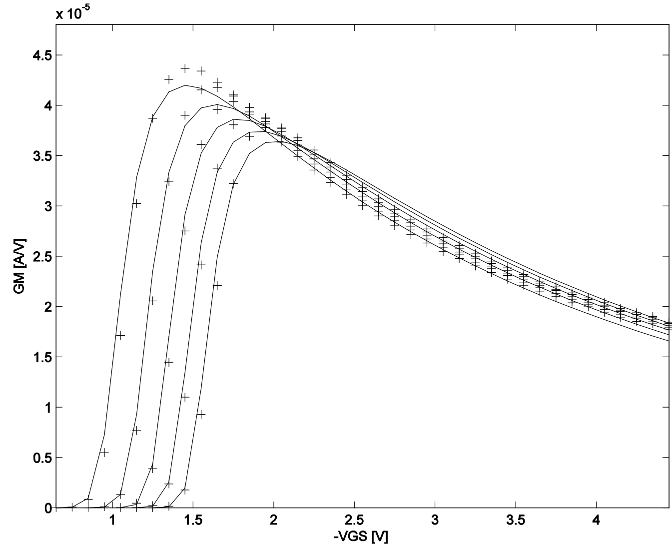


Fig. 3.94 **PMOSM** Gm characteristic of a typical wafer. W/L = 10/0.5,
VBS =0,0.6,1.2,1.8,2.4 V, VDS =- 0.1 V
+ = measured, — = HiSIM2.5.1 model

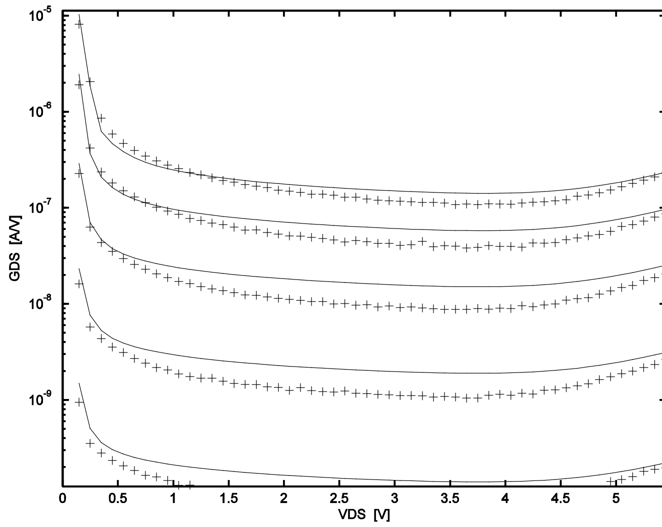


Fig. 3.95 **PMOSM** Gds characteristic of a typical wafer. W/L = 10/1.2,
VGS=-0.8,-0.9,-1.0,-1.1,-1.2 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

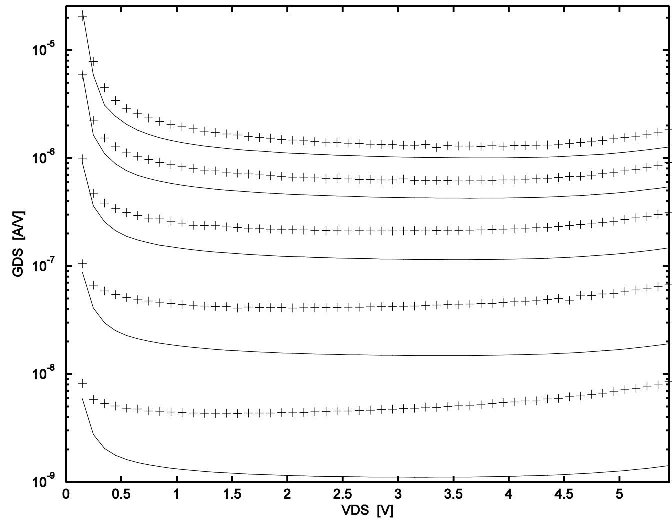


Fig. 3.96 **PMOSM** Gds characteristic of a typical wafer. W/L = 10/0.5,
VGS=-0.8,-0.9,-1.0,-1.1,-1.2 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

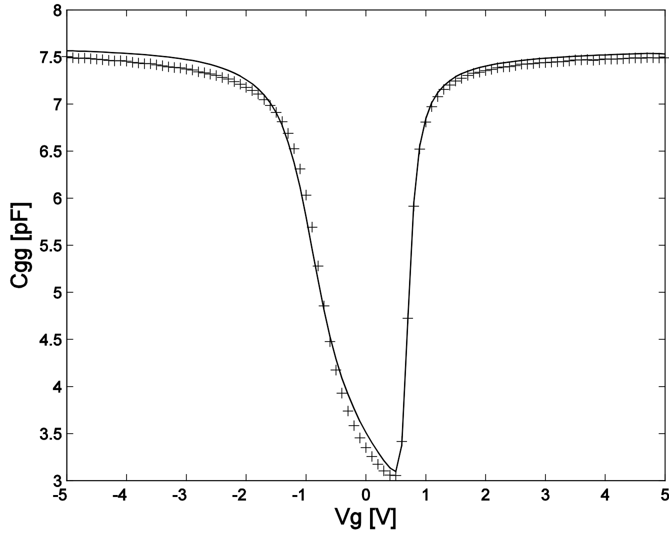


Fig. 3.97 **NMOSM** total gate capacitance of a typical wafer. W/L = 40/80,
+ = measured, — = HiSIM2.5.1 model

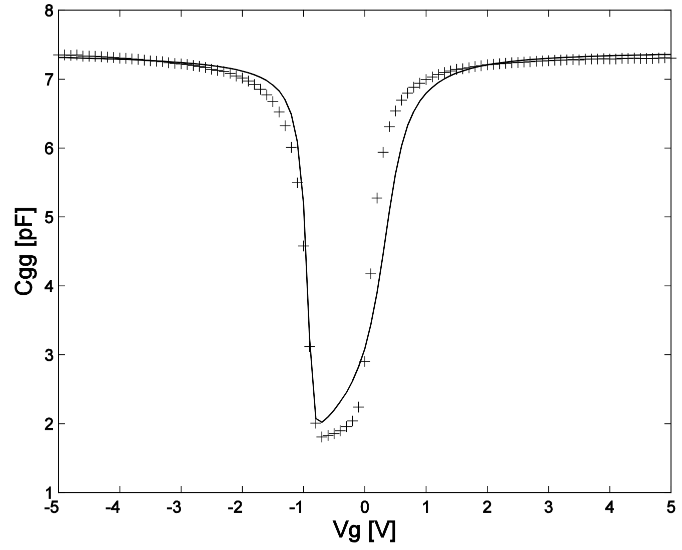


Fig. 3.98 **PMOSM** total gate capacitance of a typical wafer. W/L = 40/80,
+ = measured, — = HiSIM2.5.1 model

3.2.5 5V Waffle Transistor Characteristics

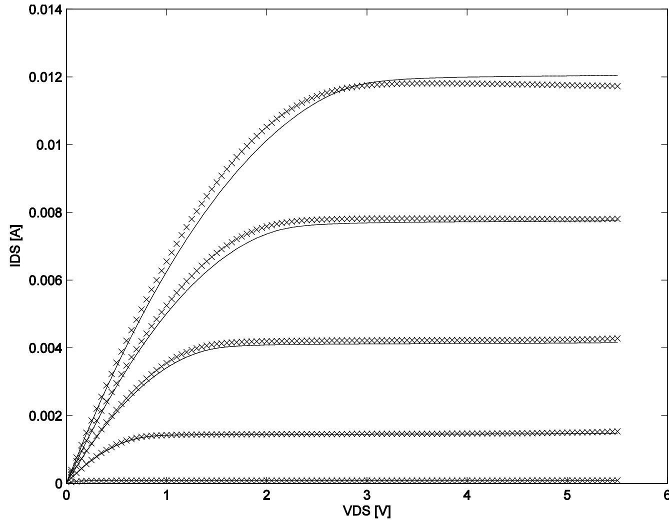


Fig. 3.99 **NMOSMW** output characteristic of a typical wafer. W/L = 64/3, VGS = 1,2,3,4,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 sub-circuit model

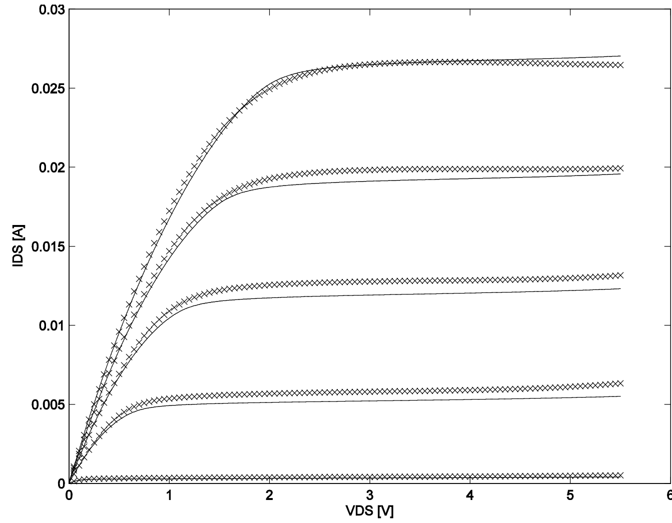


Fig. 3.100 **NMOSMW** output characteristic of a typical wafer. W/L = 64/0.5, VGS = 1,2,3,4,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 sub-circuit model

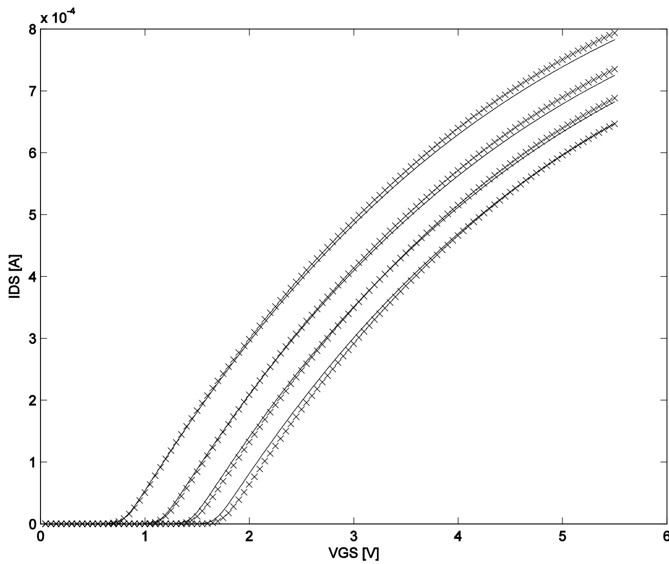


Fig. 3.101 **NMOSMW** transfer characteristic of a typical wafer. W/L = 64/3, VBS =0,-0.8,-1.6,-2.4 V, VDS = 0.1 V
+ = measured, — = BSIM3v3 sub-circuit model

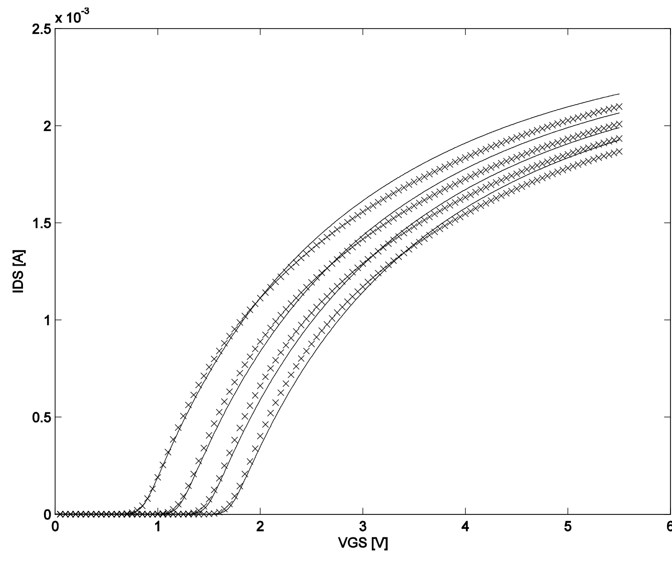


Fig. 3.102 **NMOSMW** transfer characteristic of a typical wafer. W/L = 64/0.5, VBS =0,-0.8,-1.6,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

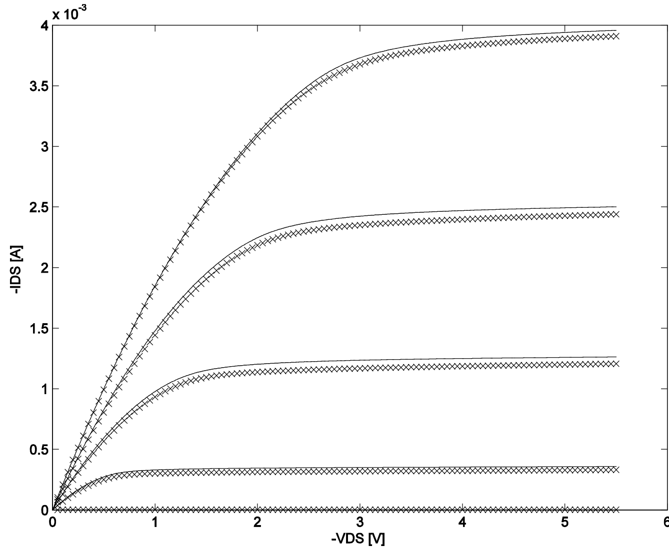


Fig. 3.103 **PMOSMW** output characteristic of a typical wafer. W/L = 64/3, VGS = -1,-2,-3,-4,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 sub-circuit model

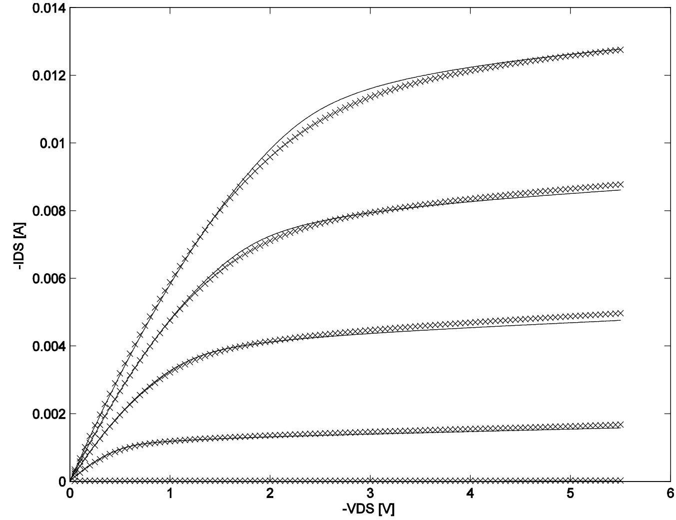


Fig. 3.104 **PMOSMW** output characteristic of a typical wafer. W/L = 64/0.5, VGS = -1,-2,-3,-4,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 sub-circuit model

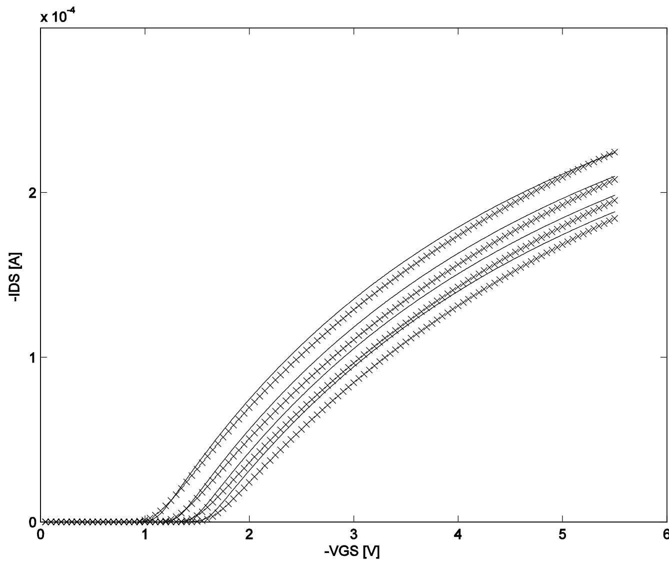


Fig. 3.105 **PMOSMW** transfer characteristic of a typical wafer. W/L = 64/3, VBS =0,0.8,1.6,2.4 V, VDS = -0.1 V
+ = measured, — = BSIM3v3 sub-circuit model

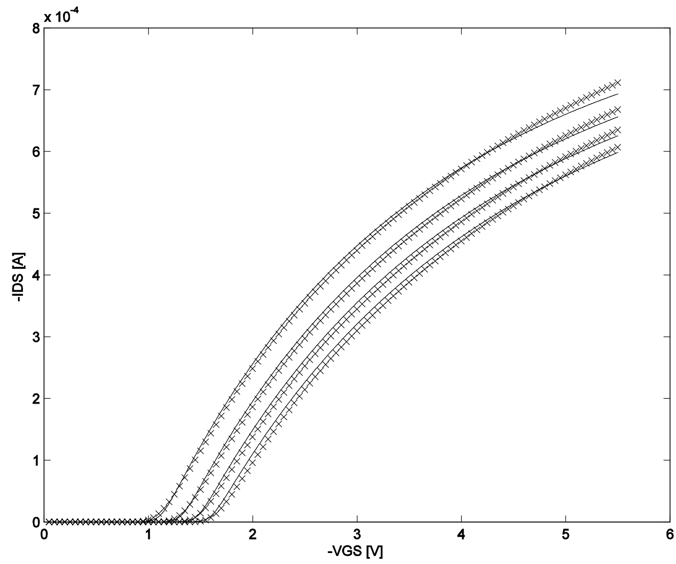


Fig. 3.106 **PMOSMW** transfer characteristic of a typical wafer. W/L = 64/0.5, VBS =0,0.8,1.6,2.4 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

3.2.6 5V HV-MOS Transistor Characteristics

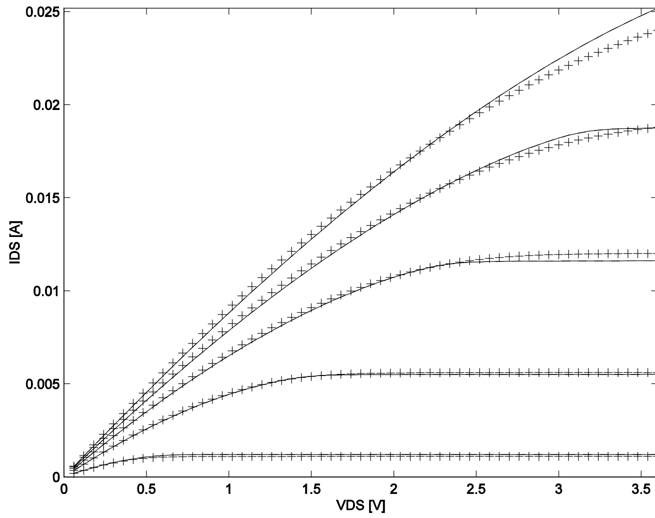


Fig. 3.107 **NMOSMH** output characteristic of a typical wafer. W/L = 100/3, VGS = 1.4,2.4,3.4,4.4,5.4 V, VBS = 0 V
+ = measured, —— = BSIM3v3 model

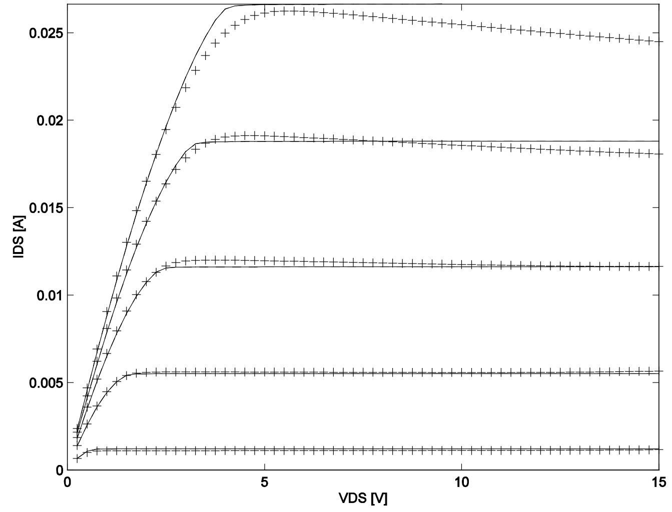


Fig. 3.108 **NMOSMH** output characteristic of a typical wafer. W/L = 100/3, VGS = 1.4,2.4,3.4,4.4,5.4 V, VBS = 0 V
+ = measured, —— = BSIM3v3 model

3.2.7 3.3V Low VT MOS Transistor Characteristics

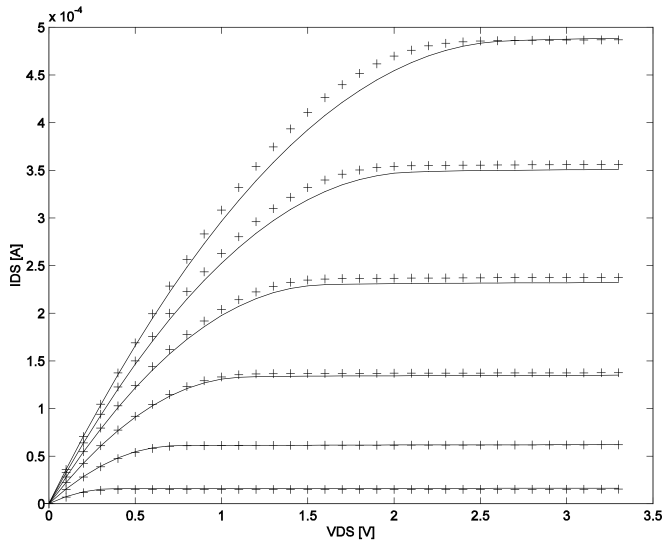


Fig.3.109 **NMOSL** output characteristic of a typical wafer. W/L = 10/10, VGS=0.9,1.38,1.86,2.34,2.82,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

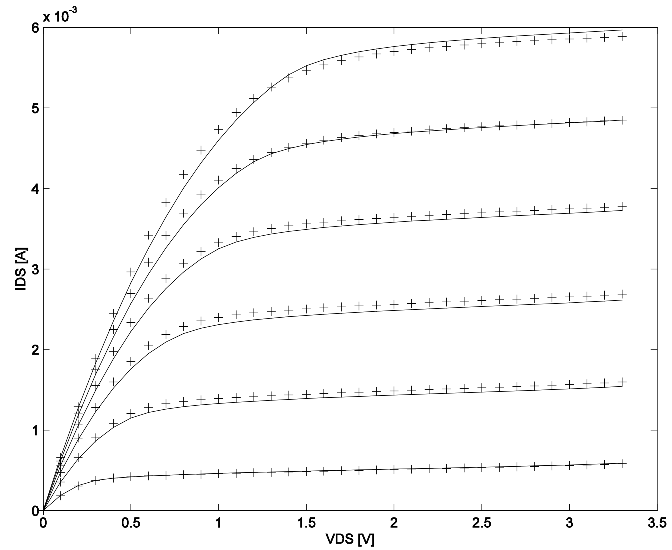


Fig. 3.110 **NMOSL** output characteristic of a typical wafer. W/L = 10/0.35, VGS=0.9,1.38,1.86,2.34,2.82,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

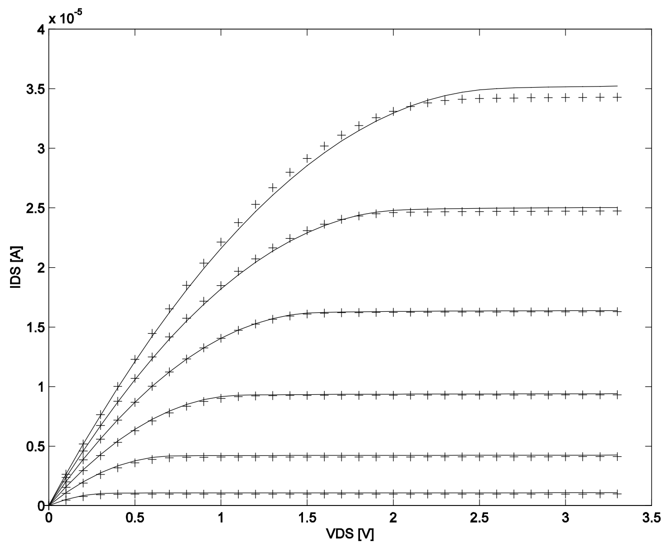


Fig. 3.111 **NMOSL** output characteristic of a typical wafer. W/L = 0.8/10, VGS=0.9,1.38,1.86,2.34,2.82,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

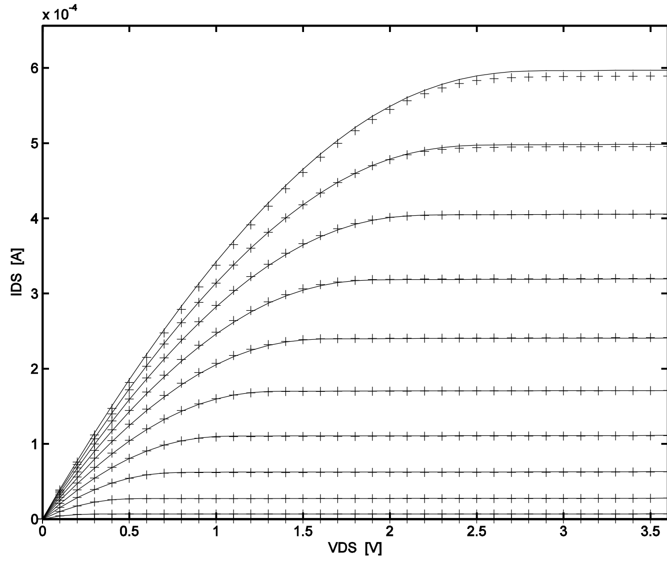


Fig.3.112 **NMOSL** output characteristic of a typical wafer. W/L = 10/10, VGS=0.4,0.72,1.04,1.36,1.68,2.0,2.32,2.64,2.96,3.28,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

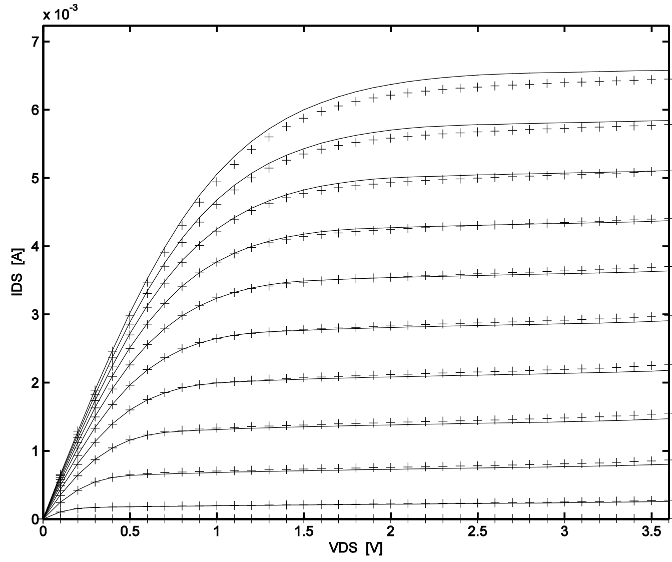


Fig. 3.113 **NMOSL** output characteristic of a typical wafer. W/L = 10/0.35, VGS=0.4,0.72,1.04,1.36,1.68,2.0,2.32,2.64,2.96,3.28,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

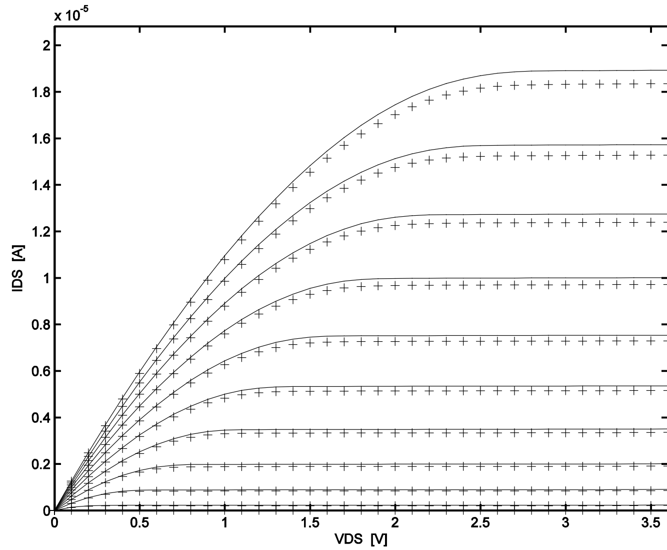


Fig. 3.114 **NMOSL** output characteristic of a typical wafer. W/L = 0.36/10, VGS=0.4,0.72,1.04,1.36,1.68,2.0,2.32,2.64,2.96,3.28,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

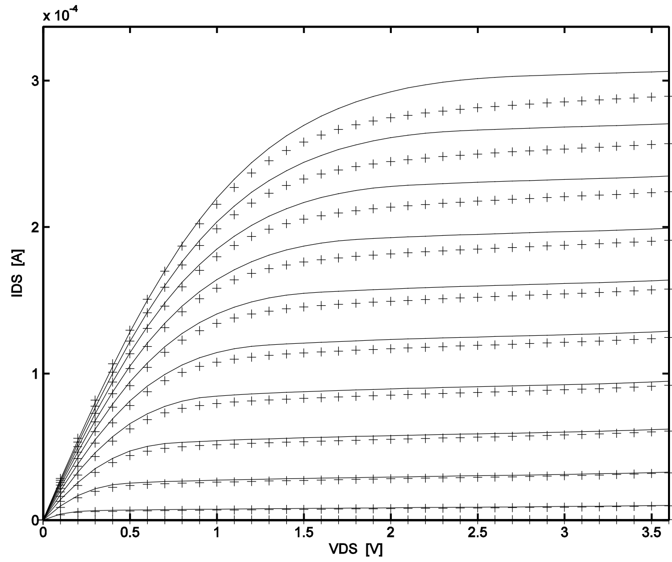


Fig. 3.115 **NMOSL** output characteristic of a typical wafer. W/L = 0.36/0.0.35, VGS=0.4,0.72,1.04,1.36,1.68,2.0,2.32,2.64,2.96,3.28,3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

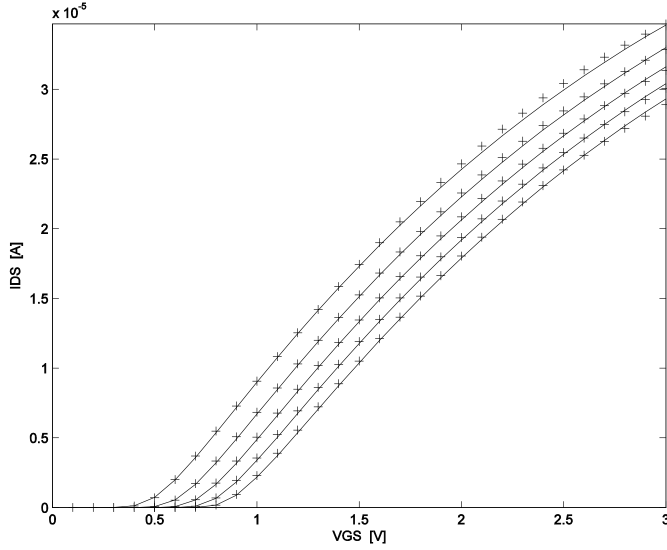


Fig. 3.116 **NMOSL** transfer characteristic of a typical wafer. W/L = 10/10, VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

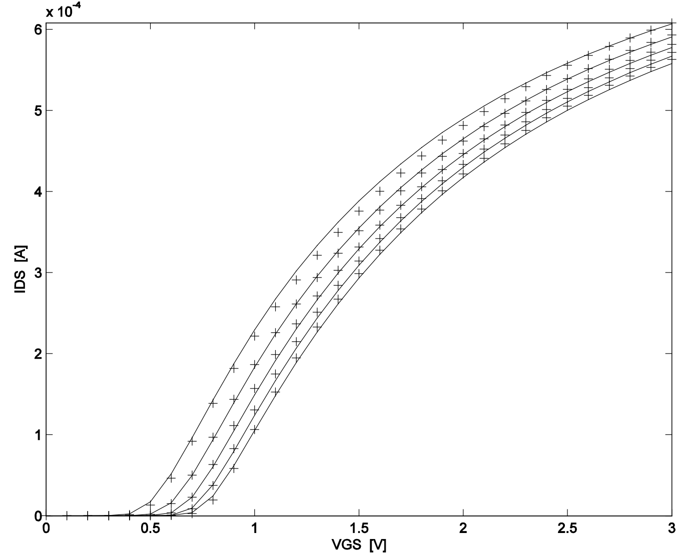


Fig. 3.117 **NMOSL** transfer characteristic of a typical wafer. W/L = 10/0.35, VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

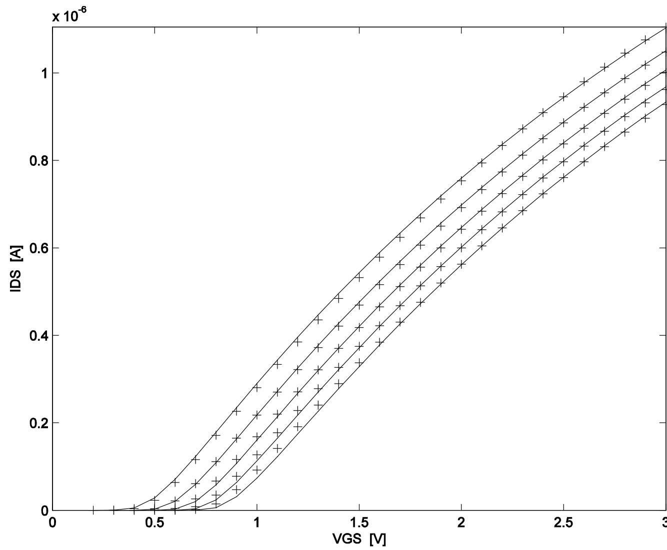


Fig. 3.119 **NMOSL** transfer characteristic of a typical wafer. W/L = 0.36/10, VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

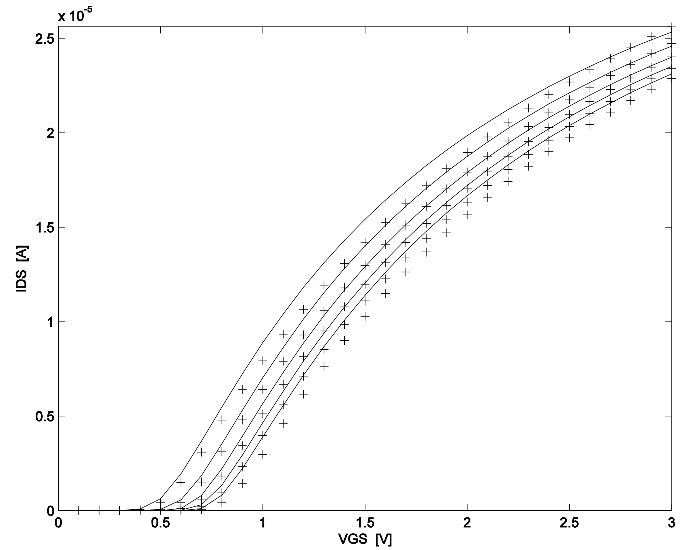


Fig. 3.120 **NMOSL** transfer characteristic of a typical wafer. W/L = 0.36/0.5, VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

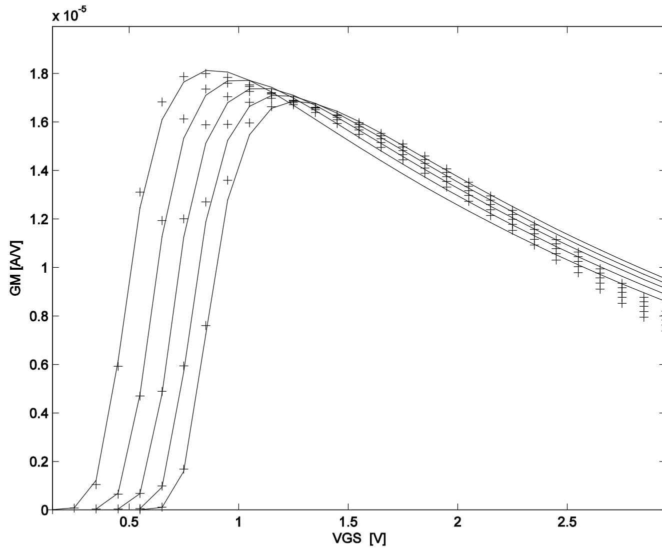


Fig. 3.121 **NMOSL** Gm characteristic of a typical wafer. W/L = 10/10, VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

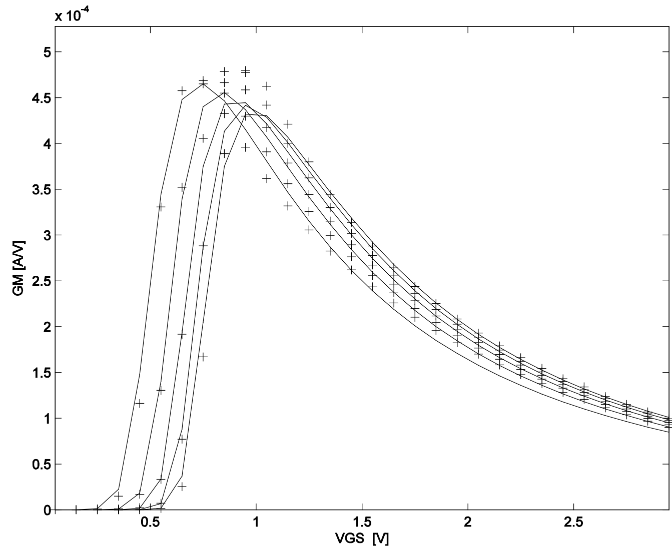


Fig. 3.122 **NMOSL** Gm characteristic of a typical wafer. W/L = 10/0.35, VBS =0,-0.5,-1.0,-1.5,-2.0 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

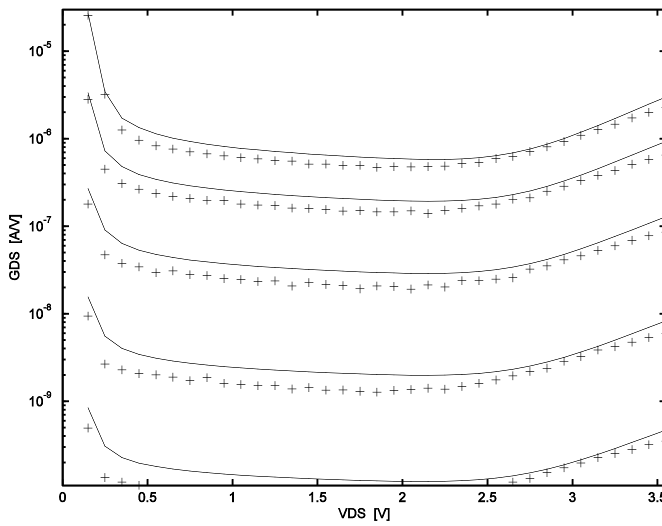


Fig. 3.123 **NMOSL** Gds characteristic of a typical wafer. W/L = 10/1.2, VGS=0.2,0.3,0.4,0.5,0.6 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

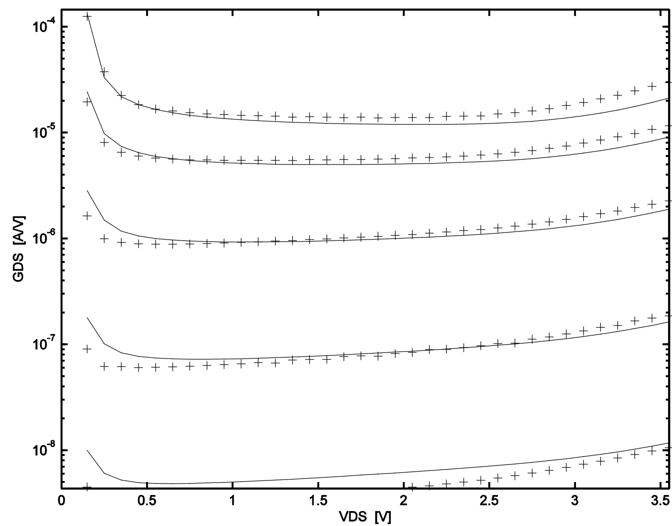


Fig. 3.124 **NMOSL** Gds characteristic of a typical wafer. W/L = 10/0.35, VGS=0.2,0.3,0.4,0.5,0.6 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

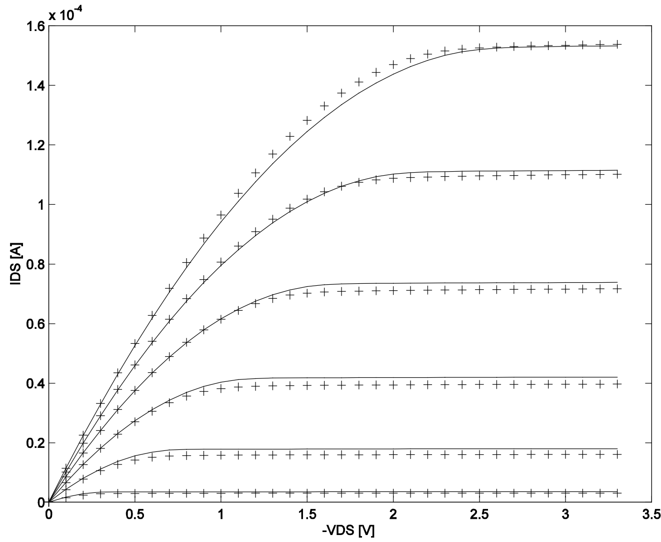


Fig. 3.125 **PMOSL** output characteristic of a typical wafer. W/L = 10/10, VGS=-0.9,-1.38,-1.86,-2.34,-2.82,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

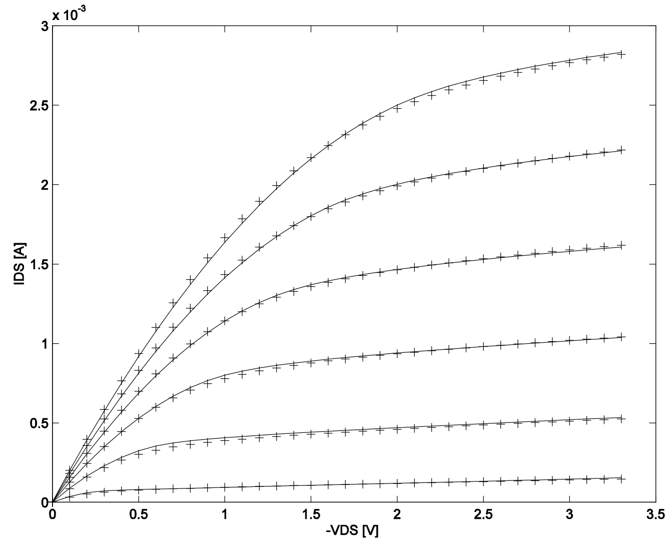


Fig. 3.126 **PMOSL** output characteristic of a typical wafer. W/L = 10/0.35, VGS=-0.9,-1.38,-1.86,-2.34,-2.82,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

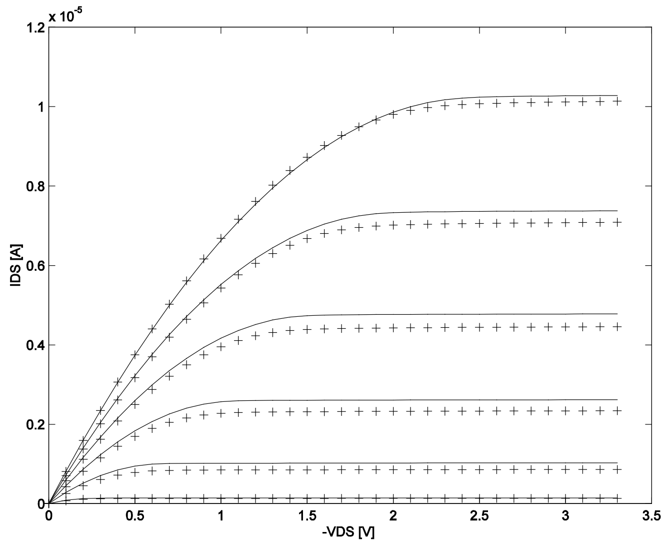


Fig. 3.128 **PMOSL** output characteristic of a typical wafer. W/L = 0.8/10, VGS=-0.9,-1.38,-1.86,-2.34,-2.82,-3.3 V, VBS = 0 V + = measured, — = BSIM3v3 model

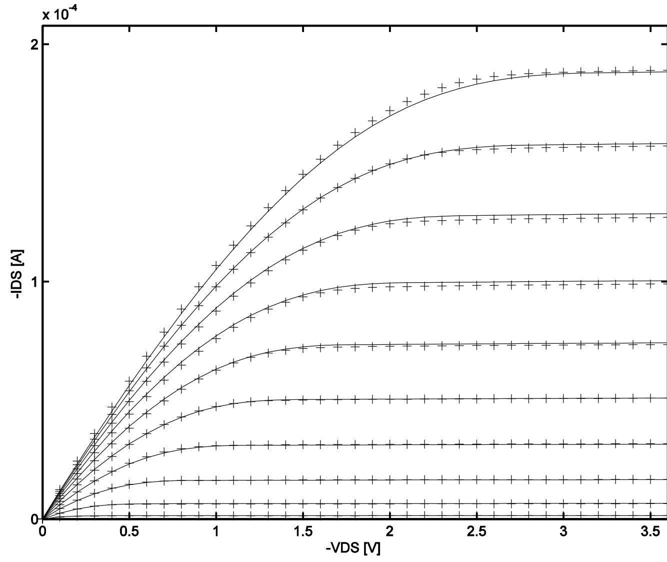


Fig. 3.129 **PMOSL** output characteristic of a typical wafer. W/L = 10/10, VGS=-0.4,-0.72,-1.04,-1.36,-1.68,-2.0,-2.32,-2.64,-2.96,-3.28,-3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

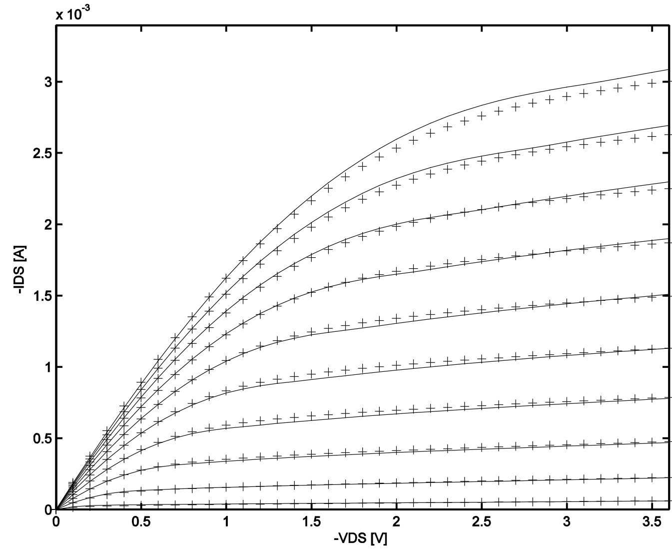


Fig. 3.130 **PMOSL** output characteristic of a typical wafer. W/L = 10/0.35, VGS=-0.4,-0.72,-1.04,-1.36,-1.68,-2.0,-2.32,-2.64,-2.96,-3.28,-3.6 V; VBS = 0 V, + = measured, — = HiSIM2.5.1 model

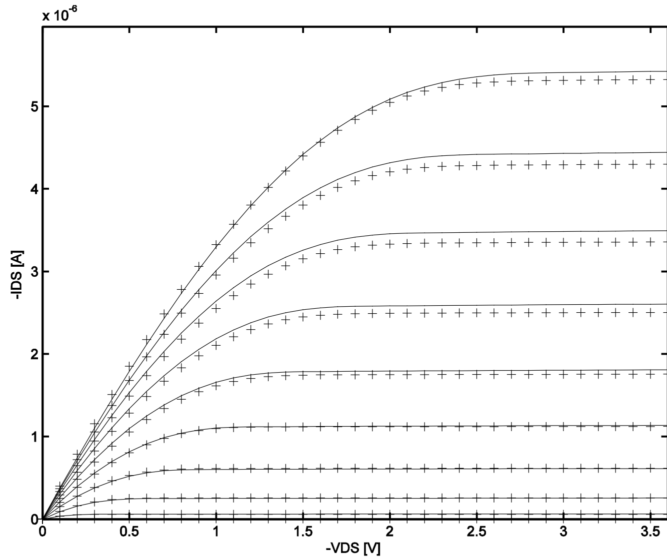


Fig. 3.132 **PMOSL** output characteristic of a typical wafer. W/L = 0.36/10, VGS=-0.4,-0.72,-1.04,-1.36,-1.68,-2.0,-2.32,-2.64,-2.96,-3.28,-3.6 V, VBS = 0 V, + = measured, — = HiSIM2.5.1 model

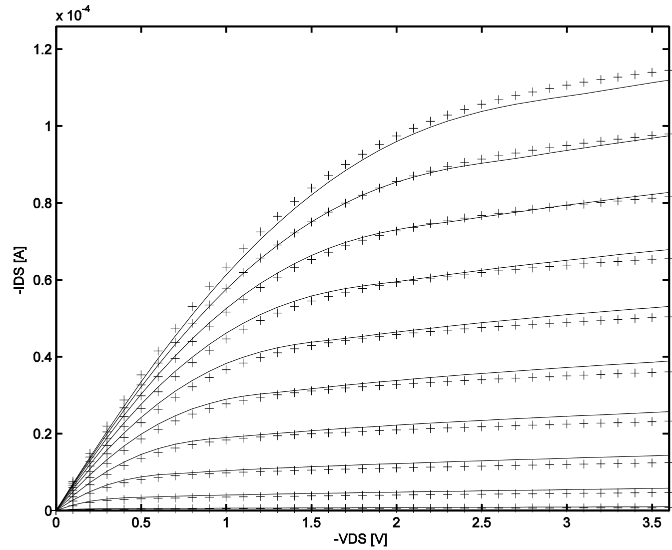


Fig. 3.133 **PMOSL** output characteristic of a typical wafer. W/L = 0.36/0.35, VGS=-0.4,-0.72,-1.04,-1.36,-1.68,-2.0,-2.32,-2.64,-2.96,-3.28,-3.6 V, VBS = 0 V + = measured, — = HiSIM2.5.1 model

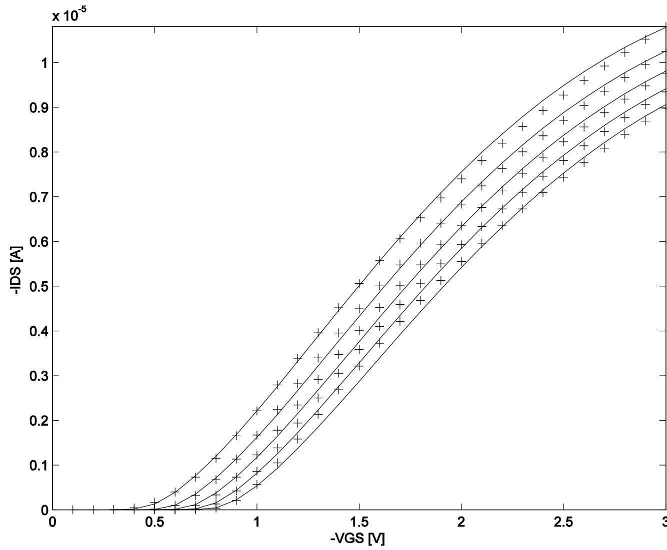


Fig. 3.134 **PMOSL** transfer characteristic of a typical wafer. W/L = 10/10, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

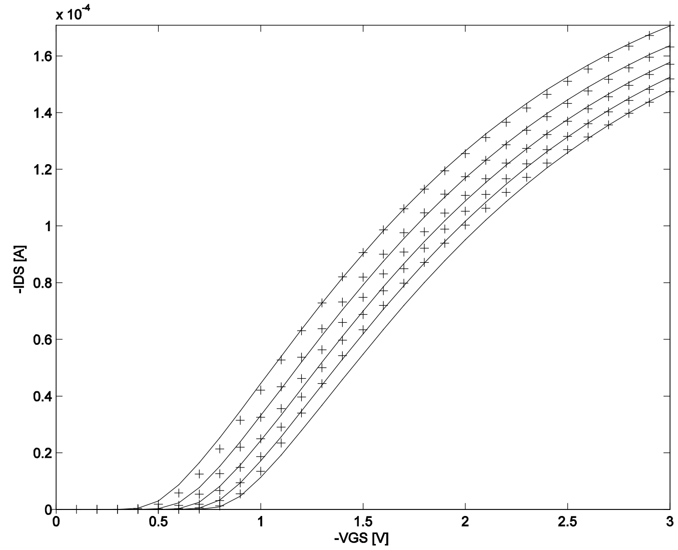


Fig. 3.135 **PMOSL** transfer characteristic of a typical wafer. W/L = 10/0.35, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

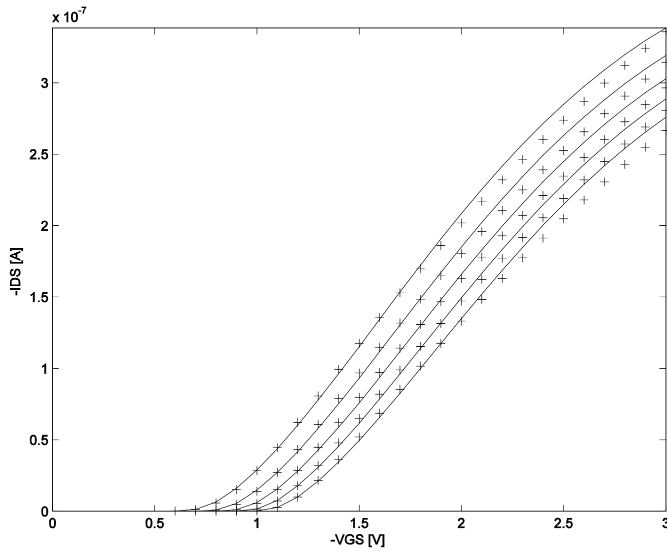


Fig. 3.139 **PMOSL** transfer characteristic of a typical wafer. W/L = 0.36/10, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

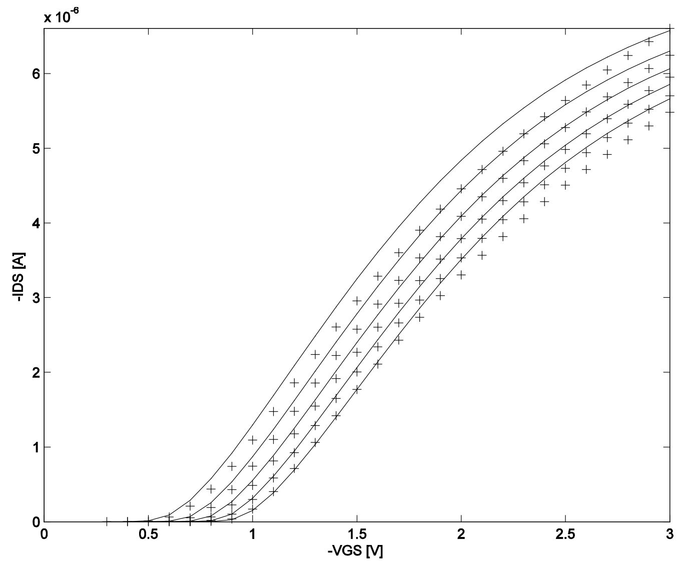


Fig. 3.140 **PMOSL** transfer characteristic of a typical wafer. W/L = 0.36/0.35, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

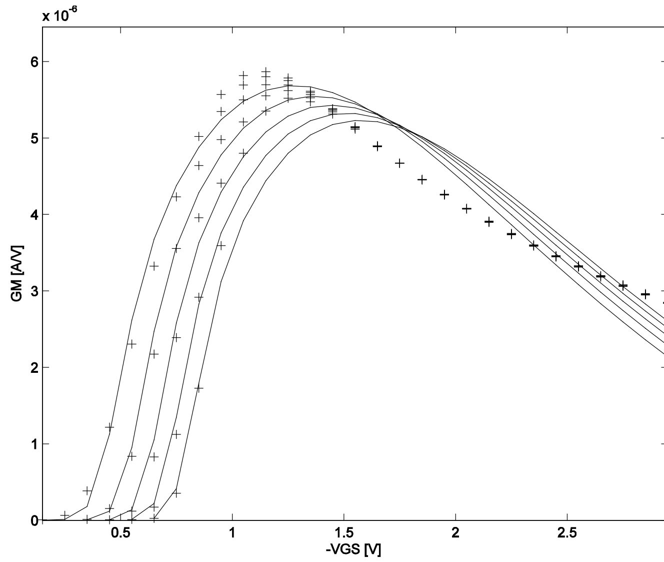


Fig. 3.142 **PMOSL** Gm characteristic of a typical wafer. W/L = 10/10, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

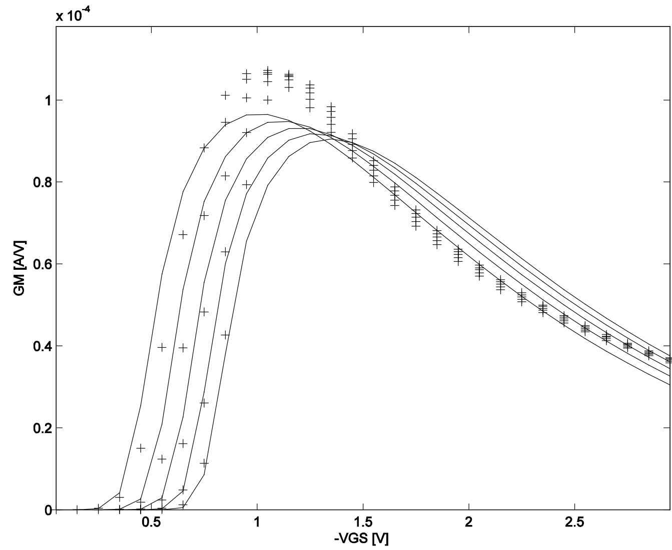


Fig. 3.143 **PMOSL** Gm characteristic of a typical wafer. W/L = 10/0.35, VBS =0,0.5,1.0,1.5,2.0 V, VDS = -0.1 V
+ = measured, — = HiSIM2.5.1 model

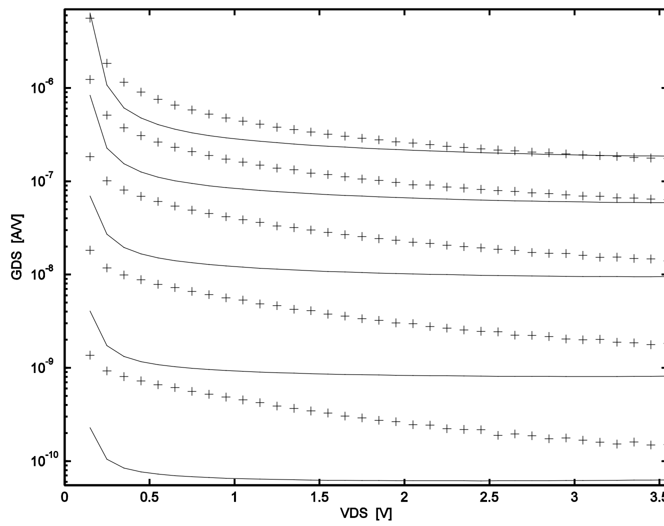


Fig. 3.144 **PMOSL** Gds characteristic of a typical wafer. W/L = 10/1.2, VGS=-0.2,-0.3,-0.4,-0.5,-0.6 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

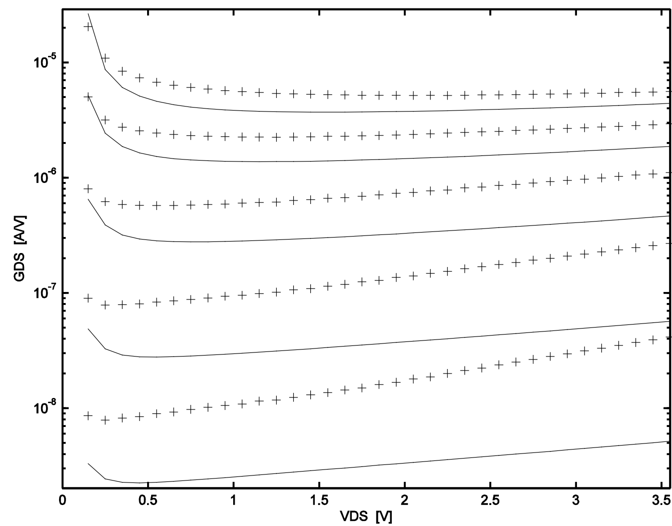


Fig. 3.145 **PMOSL** Gds characteristic of a typical wafer. W/L = 10/0.35, VGS=-0.2,-0.3,-0.4,-0.5,-0.6 V;
VBS = 0 V, + = measured, — = HiSIM2.5.1 model

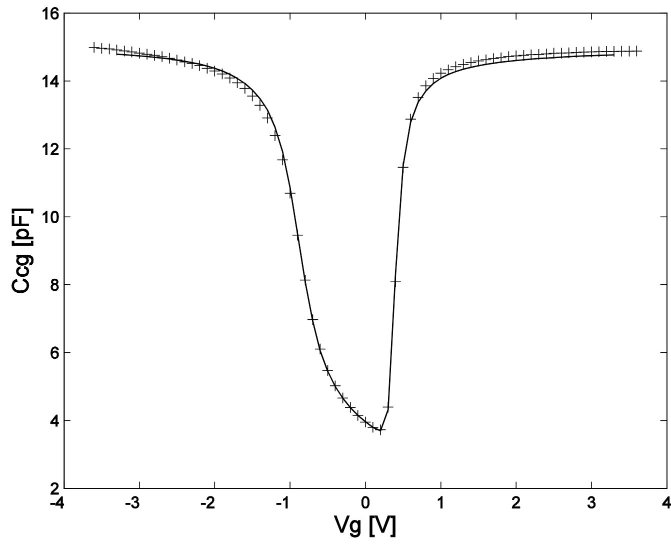


Fig. 3.146 **NMOSL** total gate capacitance of a typical wafer. W/L = 40/80,

+ = measured, — = HiSIM2.5.1 model

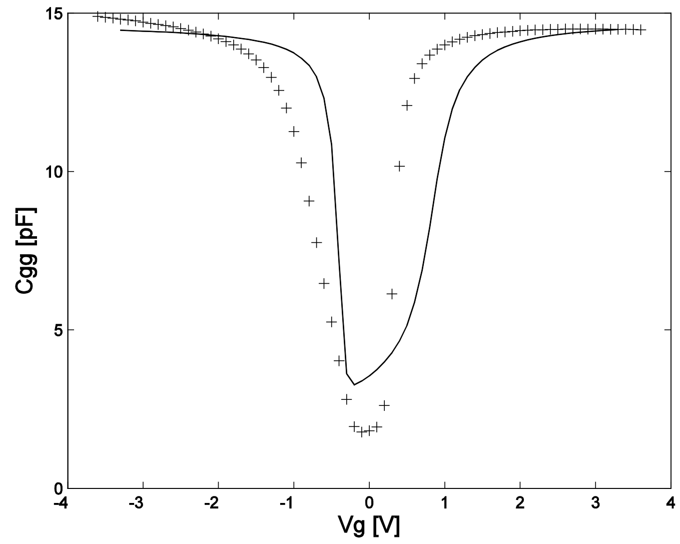


Fig. 3.147 **PMOSL** total gate capacitance of a typical wafer. W/L = 40/80,

+ = measured, — = HiSIM2.5.1 model

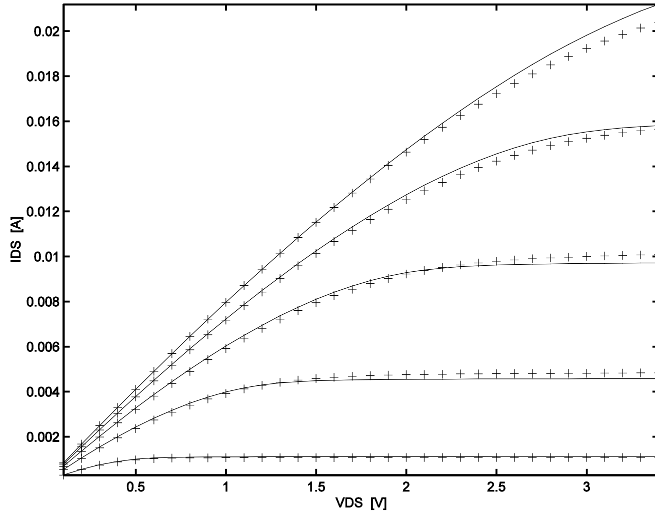


Fig. 3.148 **NMOSHL** output characteristic of a typical wafer. W/L = 100/3,

VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V

+ = measured, — = BSIM3v3 model

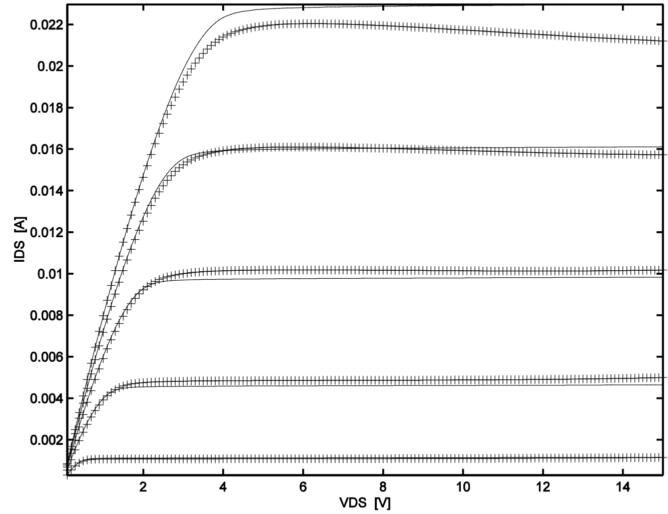


Fig. 3.149 **NMOSHL** output characteristic of a typical wafer. W/L = 100/3,

VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V

+ = measured, — = BSIM3v3 model

3.2.8 5V Low VT MOS Transistor Characteristics

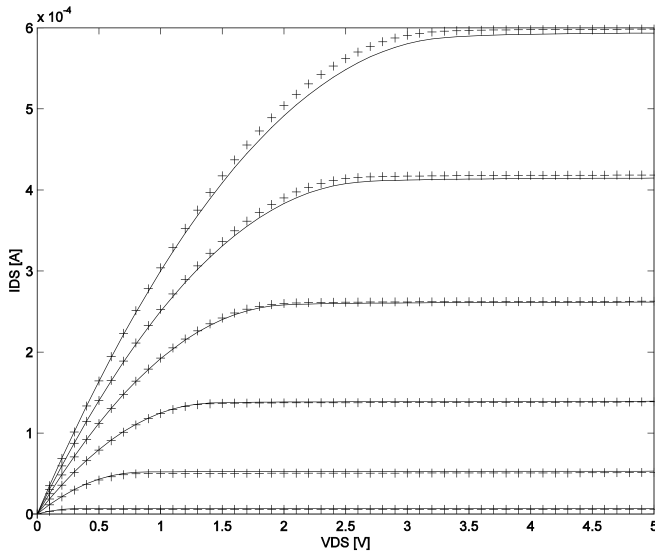


Fig. 3.150 **NMOSML** output characteristic of a typical wafer. W/L = 10/10, VGS = 1,1.8,2.6,3.4,4.2,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

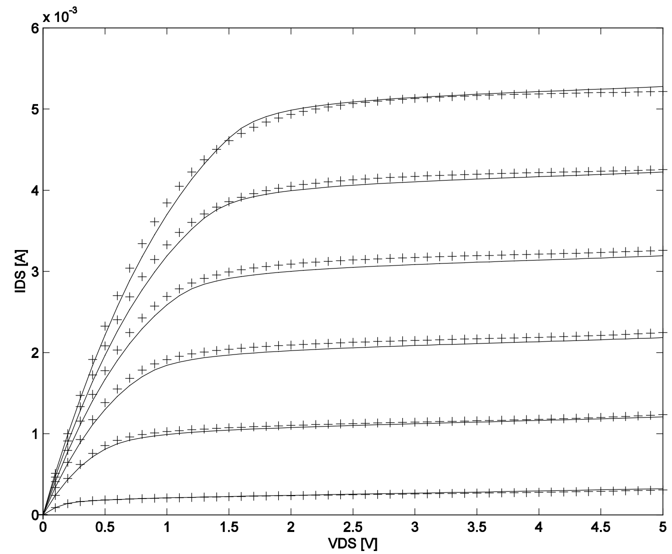


Fig. 3.151 **NMOSML** output characteristic of a typical wafer. W/L = 10/0.5, VGS = 1,1.8,2.6,3.4,4.2,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

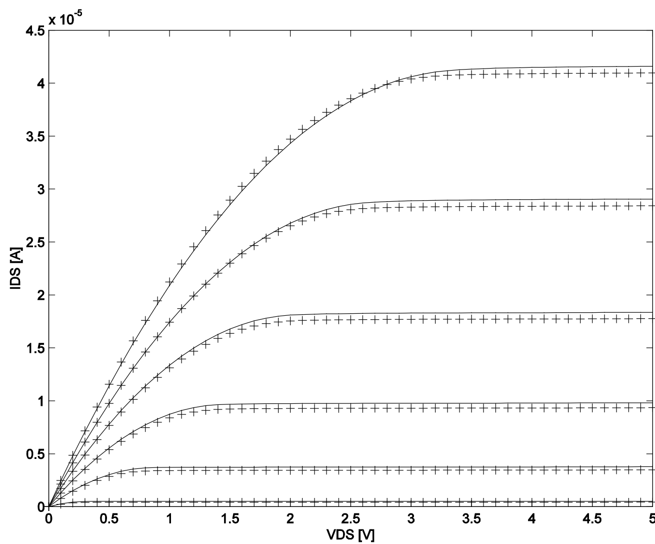


Fig. 3.152 **NMOSML** output characteristic of a typical wafer. W/L = 0.8/10, VGS = 1,1.8,2.6,3.4,4.2,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

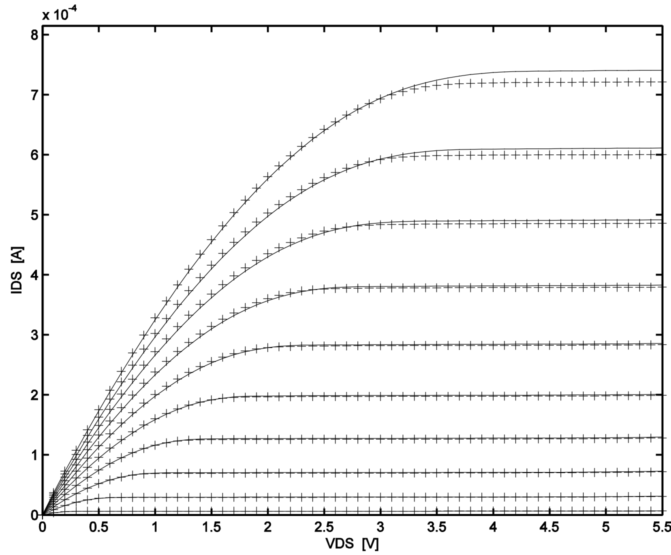


Fig. 3.153 **NMOSML** output characteristic of a typical wafer. W/L = 10/10, VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, —— = HiSIM2.5.1 model

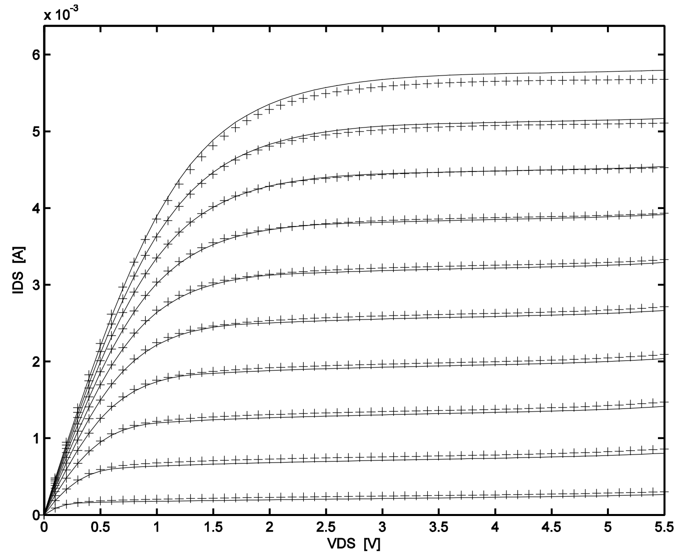


Fig. 3.154 **NMOSML** output characteristic of a typical wafer. W/L = 10/0.5, VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, —— = HiSIM2.5.1 model

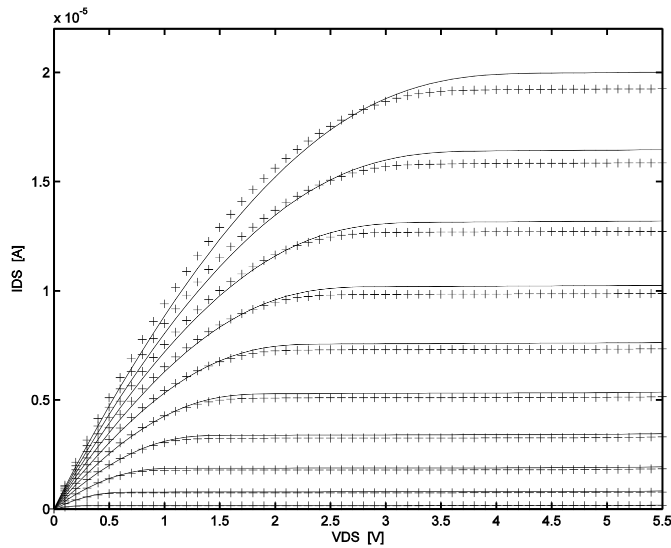


Fig. 3.155 **NMOSML** output characteristic of a typical wafer. W/L = 0.36/10, VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, —— = HiSIM2.5.1 model

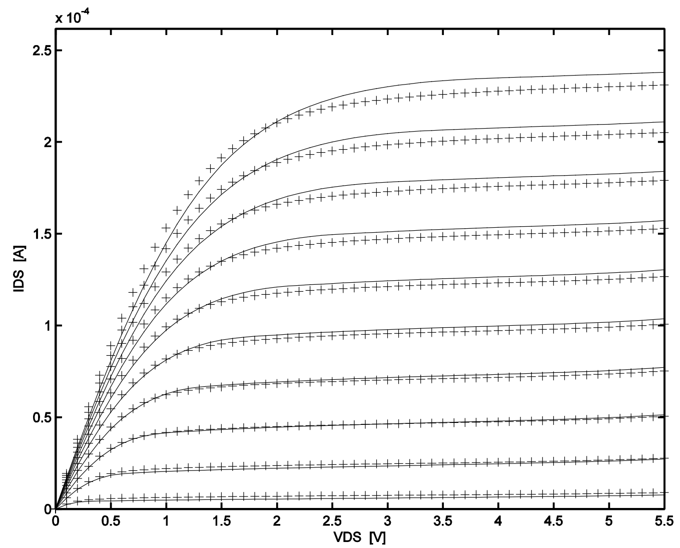


Fig. 3.156 **NMOSML** output characteristic of a typical wafer. W/L = 0.36/0.5, VGS = 1.0,1.5,2.0,2.5,3.0,3.5,4.0,4.5,5.0,5.5 V, VBS = 0 V
+ = measured, —— = HiSIM2.5.1 model

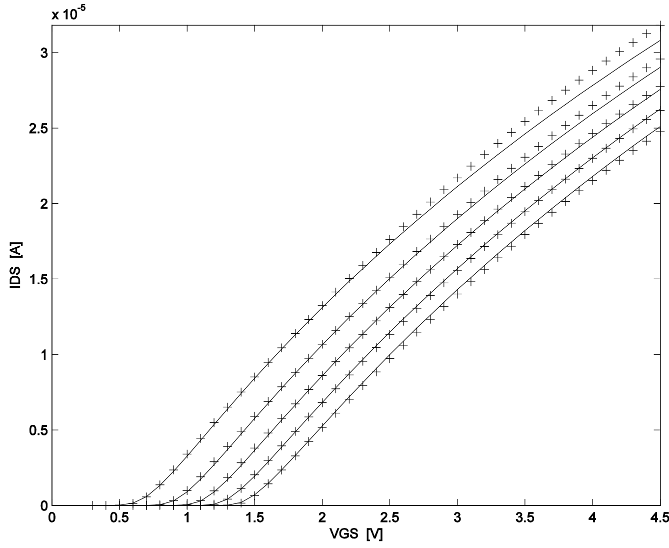


Fig. 3.157 **NMOSML** transfer characteristic of a typical wafer. W/L = 10/10, VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

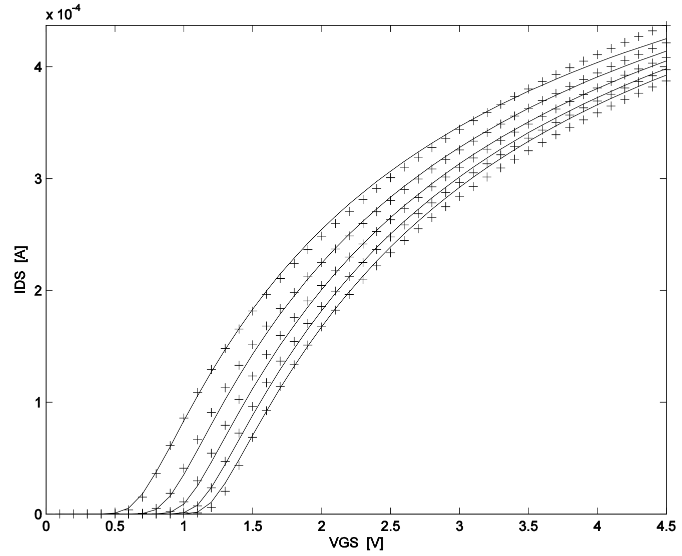


Fig. 3.158 **NMOSML** transfer characteristic of a typical wafer. W/L = 10/0.5, VBS = 0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

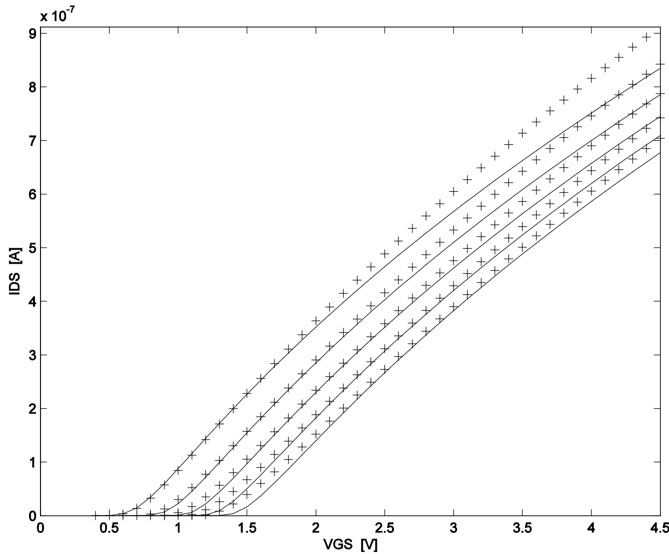


Fig. 3.160 **NMOSML** transfer characteristic of a typical wafer. W/L = 0.36/10, VBS = 0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

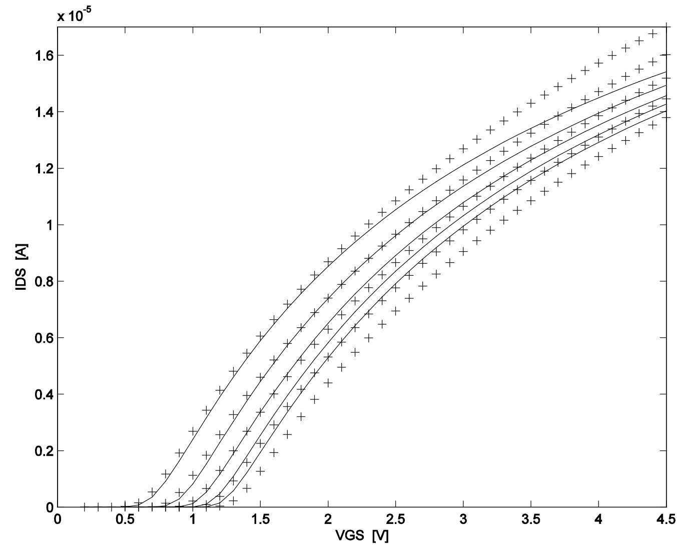


Fig. 3.161 **NMOSML** transfer characteristic of a typical wafer. W/L = 0.36/0.5, VBS = 0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V
+ = measured, — = HiSIM2.5.1 model

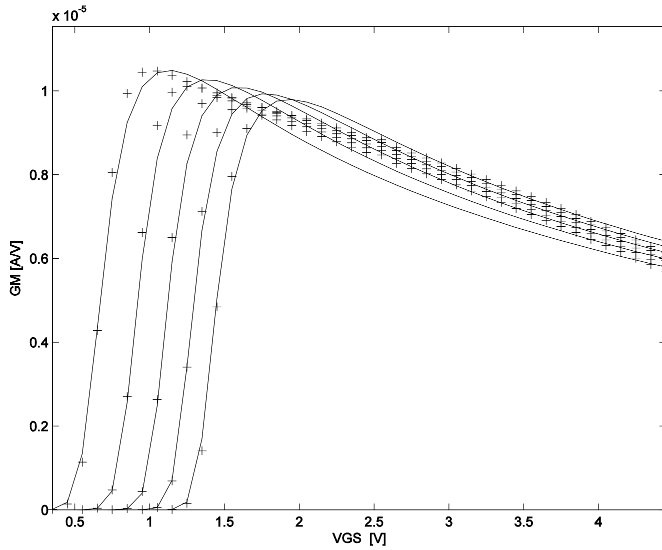


Fig. 3.162 **NMOSML** Gm characteristic of a typical wafer. W/L = 10/10,

VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V

+ = measured, — = HiSIM2.5.1 model

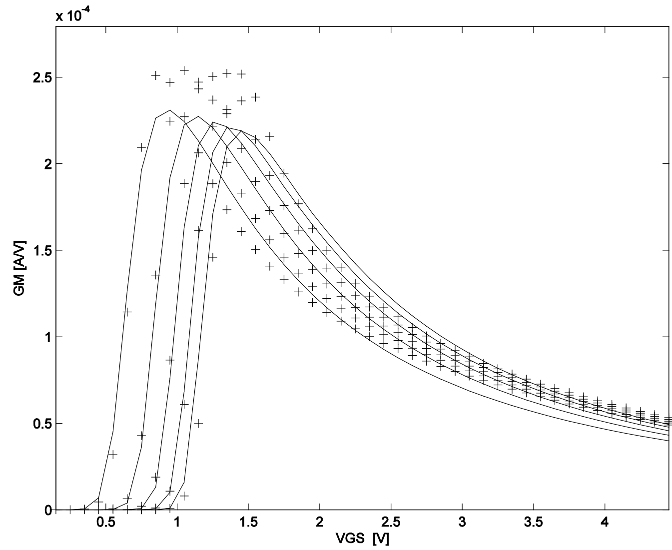


Fig. 3.163 **NMOSML** Gm characteristic of a typical wafer. W/L = 10/0.5,

VBS =0,-0.6,-1.2,-1.8,-2.4 V, VDS = 0.1 V

+ = measured, — = HiSIM2.5.1 model

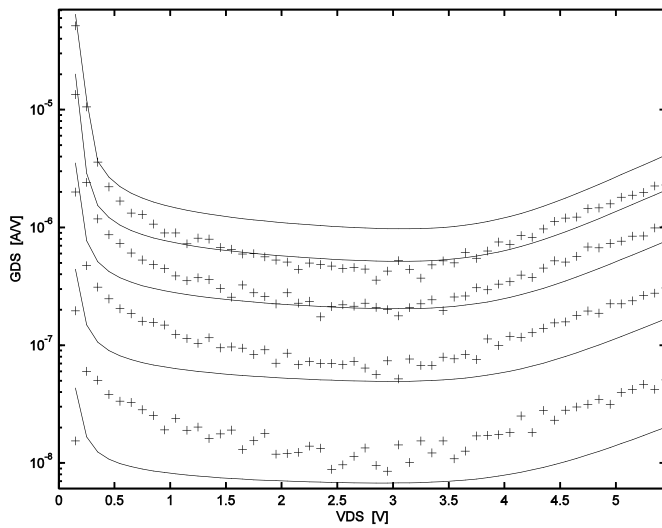


Fig. 3.164 **NMOSML** Gds characteristic of a typical wafer. W/L = 10/1.2,

VGS=0.5,0.6,0.7,0.8,0.9 V;

VBS = 0 V, + = measured, — = HiSIM2.5.1 model

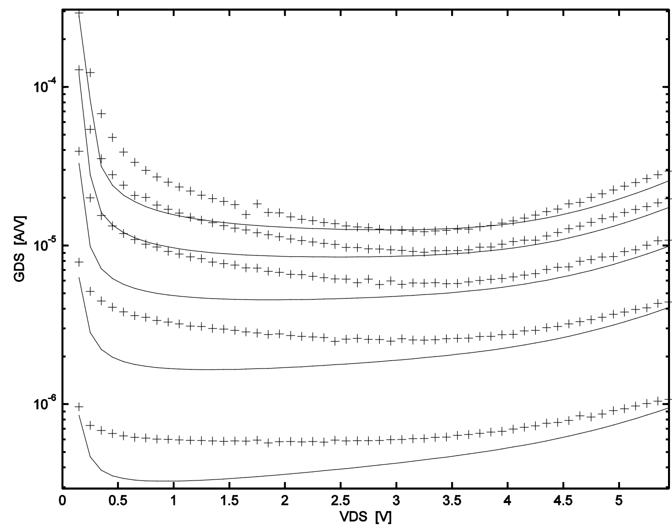


Fig. 3.165 **NMOSML** Gds characteristic of a typical wafer. W/L = 10/0.5,

VGS=0.5,0.6,0.7,0.8,0.9 V;

VBS = 0 V, + = measured, — = HiSIM2.5.1 model

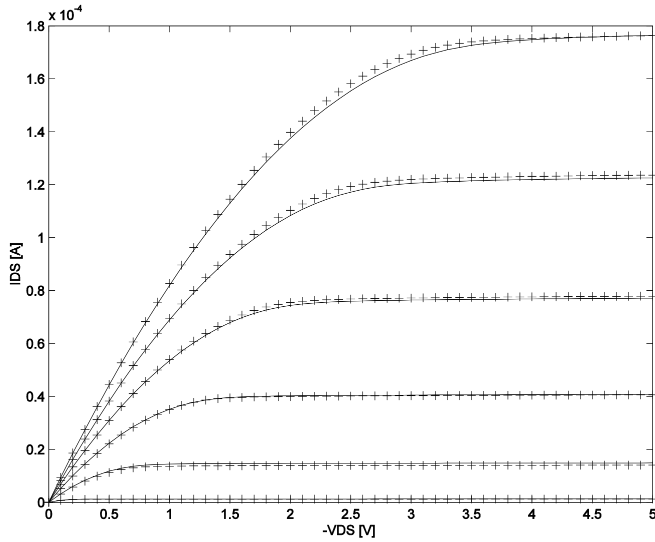


Fig. 3.166 **PMOSML** output characteristic of a typical wafer. W/L = 10/10, VGS = -1,-1.8,-2.6,-3.4,-4.2,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

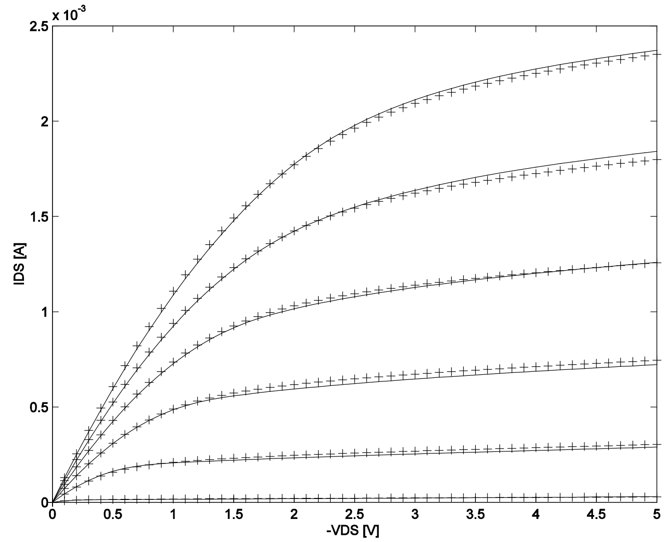


Fig. 3.167 **PMOSML** output characteristic of a typical wafer. W/L = 10/0.5, VGS = -1,-1.8,-2.6,-3.4,-4.2,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

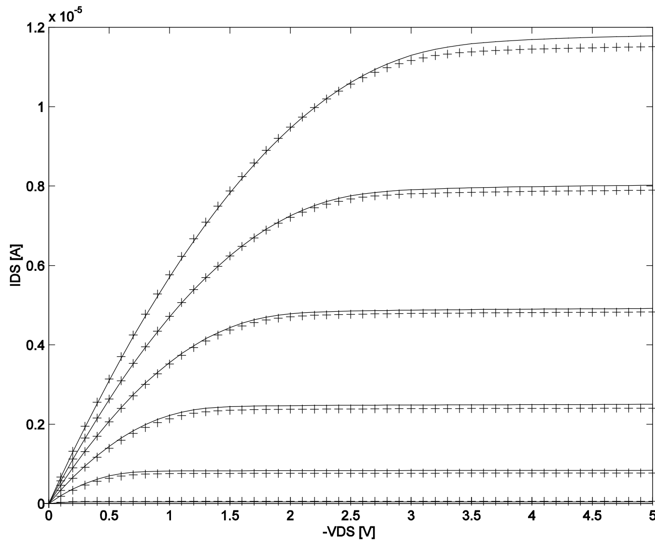


Fig. 3.169 **PMOSML** output characteristic of a typical wafer. W/L = 0.8/10, VGS = -1,-1.8,-2.6,-3.4,-4.2,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

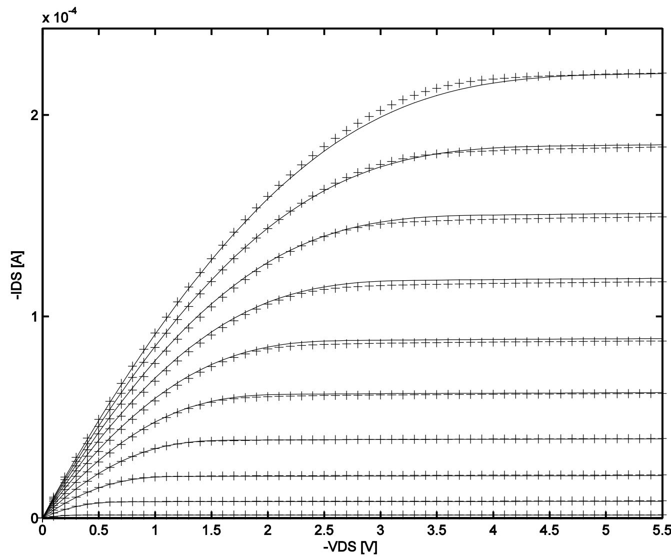


Fig. 3.170 **PMOSML** output characteristic of a typical wafer. W/L = 10/10, VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

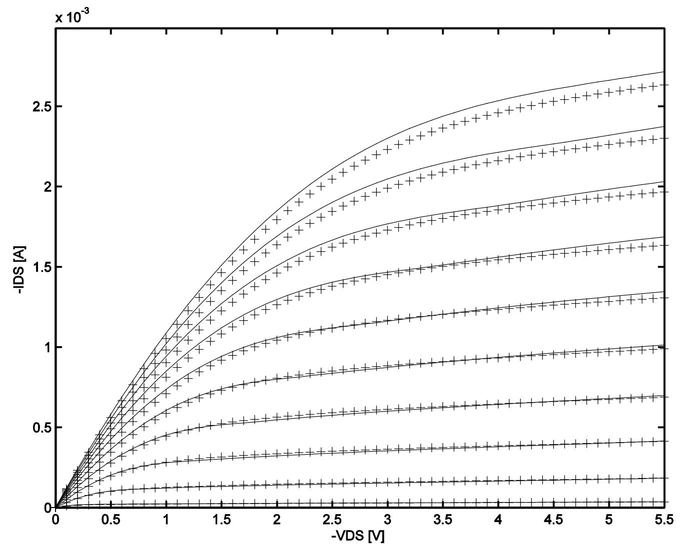


Fig. 3.171 **PMOSML** output characteristic of a typical wafer. W/L = 10/0.5, VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

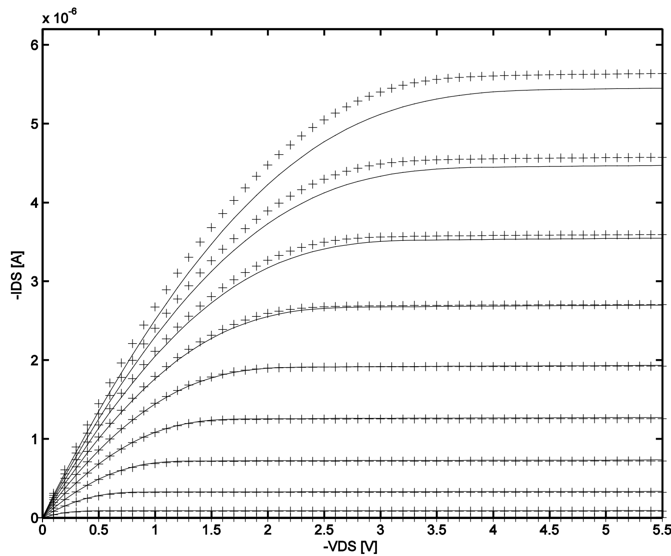


Fig. 3.173 **PMOSML** output characteristic of a typical wafer. W/L = 0.36/10, VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

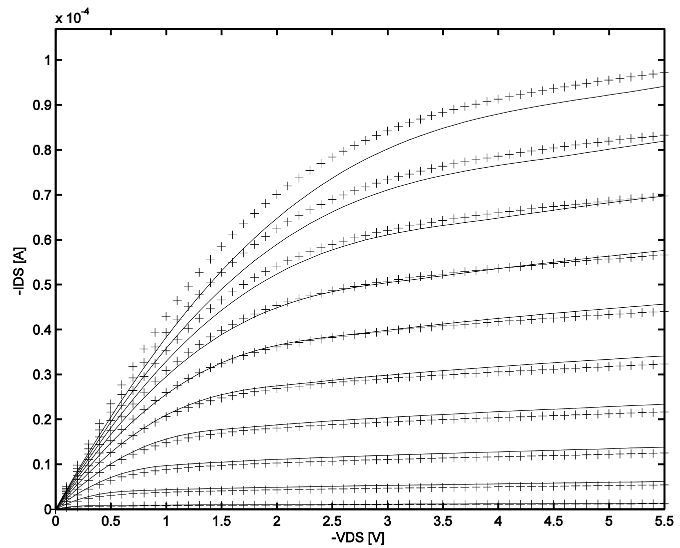


Fig. 3.174 **PMOSML** output characteristic of a typical wafer. W/L = 0.36/0.5, VGS = -1.0,-1.5,-2.0,-2.5,-3.0,-3.5,-4.0,-4.5,-5.0,-5.5 V, VBS = 0 V
+ = measured, — = HiSIM2.5.1 model

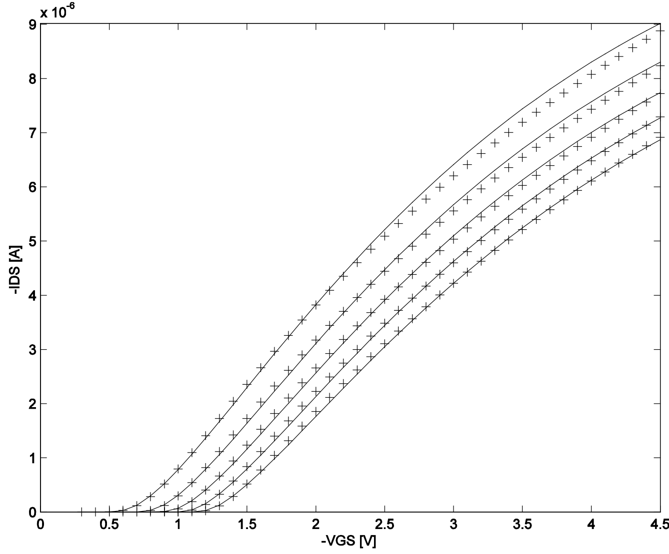


Fig. 3.175 **PMOSML** transfer characteristic of a typical wafer. W/L = 10/10, VBS = 0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

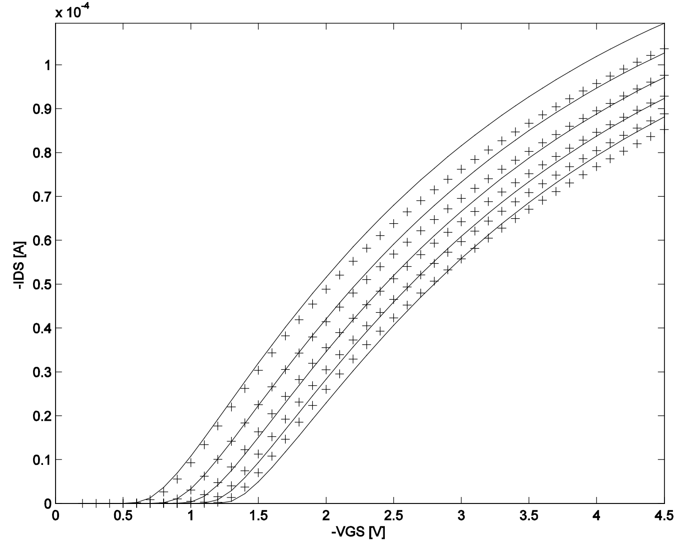


Fig. 3.176 **PMOSML** transfer characteristic of a typical wafer. W/L = 10/0.5, VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

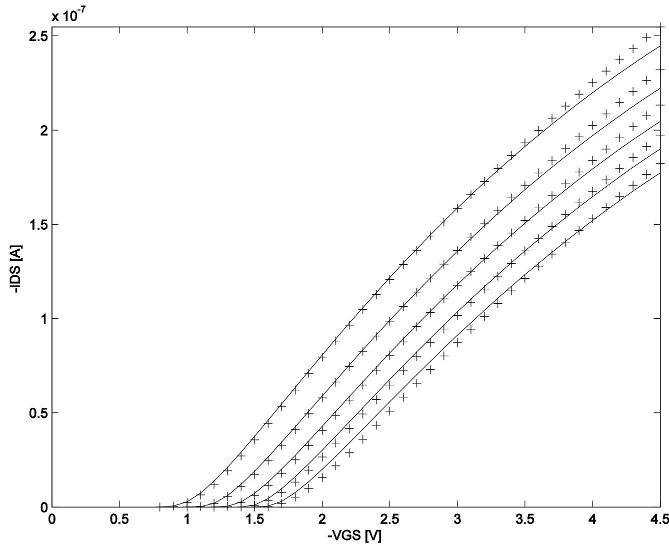


Fig. 3.180 **PMOSML** transfer characteristic of a typical wafer. W/L = 0.36/10, VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

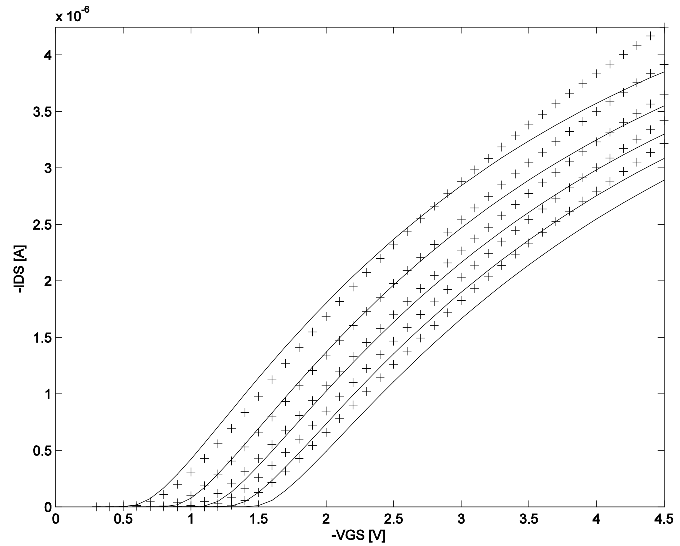


Fig. 3.181 **PMOSML** transfer characteristic of a typical wafer. W/L = 0.36/0.5, VBS =0,0.6,1.2,1.8,2.4 V, VDS =-0.1 V
+ = measured, — = HiSIM2.5.1 model

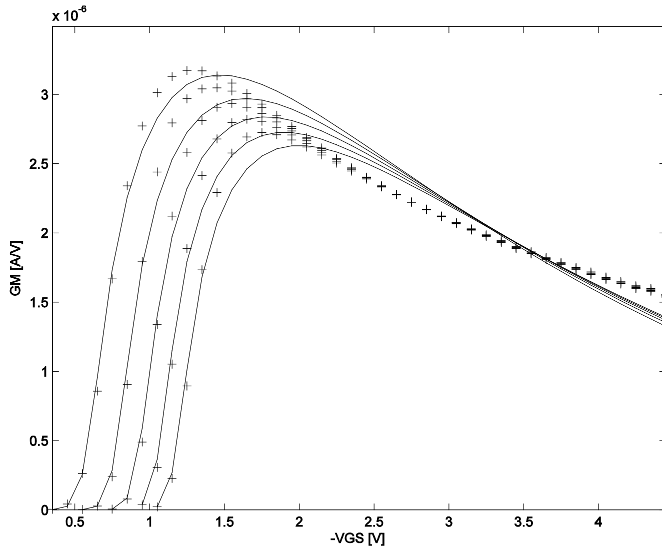


Fig. 3.182 **PMOSML** Gm characteristic of a typical wafer. W/L = 10/10,

VBS =0,0.6,1.2,1.8,2.4 V, VDS =- 0.1 V

+ = measured, — = HiSIM2.5.1 model

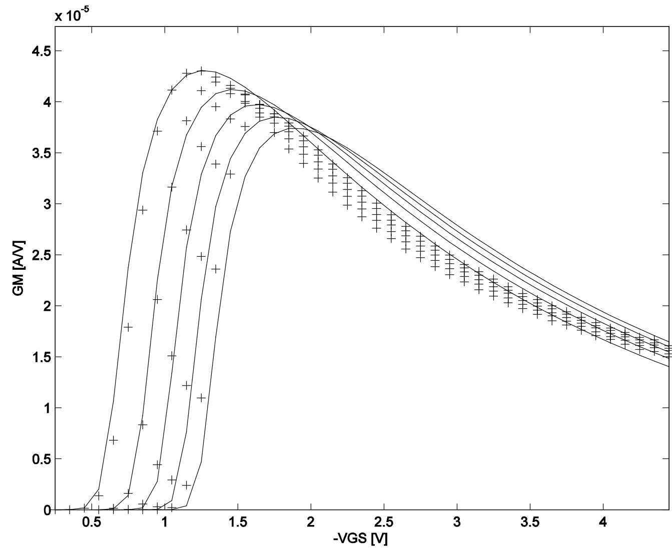


Fig. 3.183 **PMOSML** Gm characteristic of a typical wafer. W/L = 10/0.5,

VBS =0,0.6,1.2,1.8,2.4 V, VDS = -0.1 V

+ = measured, — = HiSIM2.5.1 model

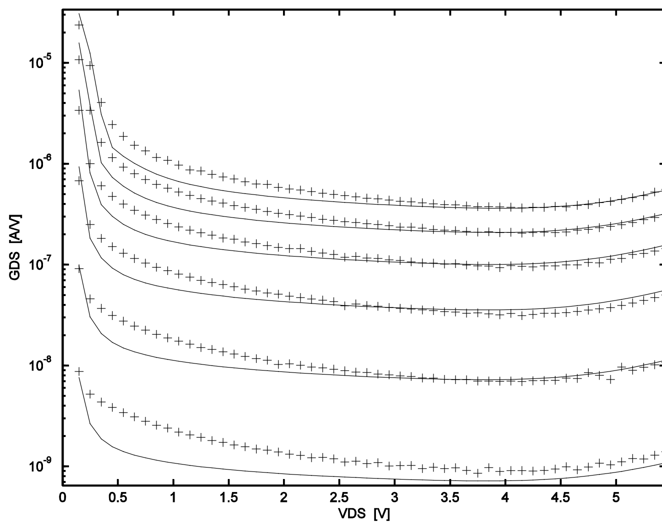


Fig. 3.18451 **PMOSML** Gds characteristic of a typical wafer. W/L = 10/1.2,

VGS=-0.5,-0.6,-0.7,-0.8,-0.9 V;

VBS = 0 V, + = measured, — = HiSIM2.5.1 model

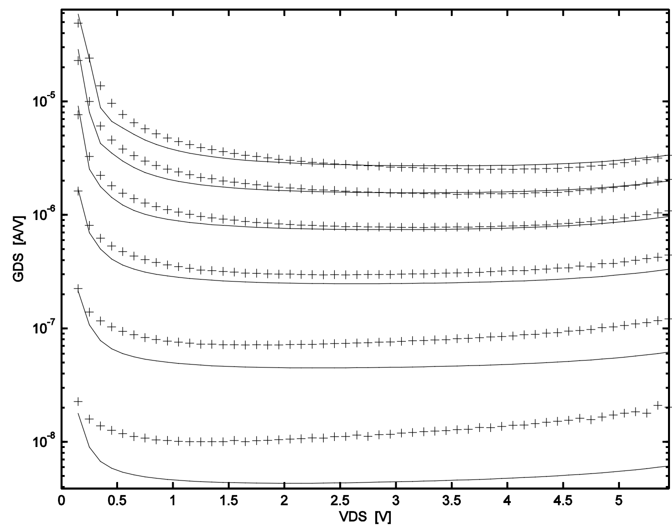


Fig. 3.185 **PMOSML** Gds characteristic of a typical wafer. W/L = 10/0.5,

VGS=-0.5,-0.6,-0.7,-0.8,-0.9 V;

VBS = 0 V, + = measured, — = HiSIM2.5.1 model

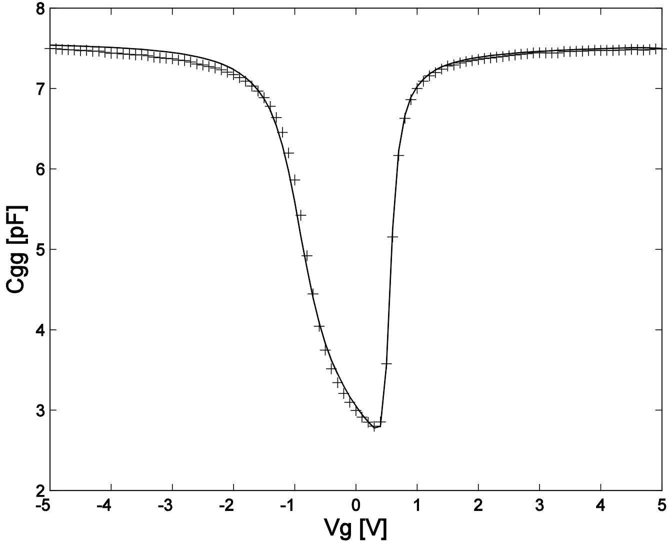


Fig. 3.18653 **NMOSML** total gate capacitance of a typical wafer. W/L = 40/80, + = measured, — = HiSIM2.5.1 model

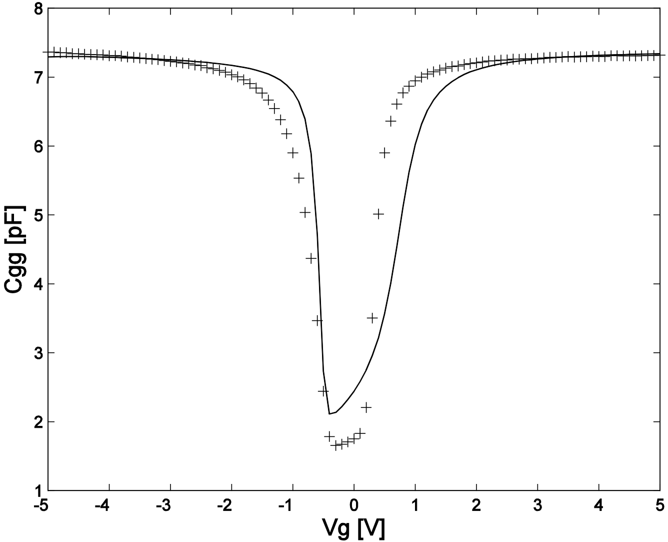


Fig. 3.187 **PMOSML** total gate capacitance of a typical wafer. W/L = 40/80, + = measured, — = HiSIM2.5.1 model

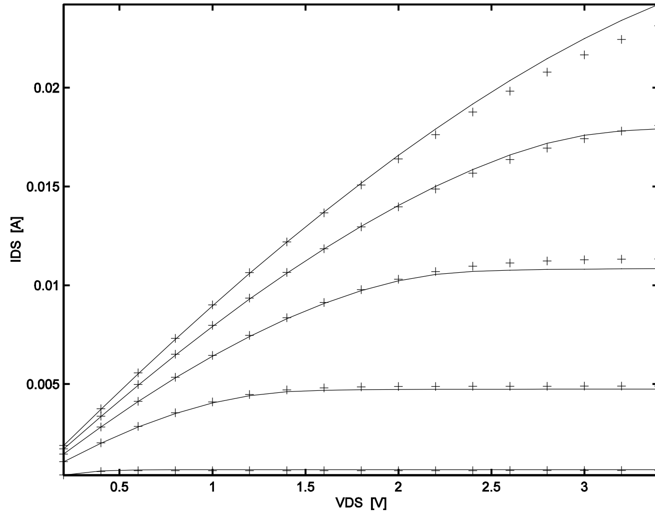


Fig. 3.188 **NMOSHL** output characteristic of a typical wafer. W/L = 100/3,
VGS = 1.0,2.0,3.0,4.0,5.0 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

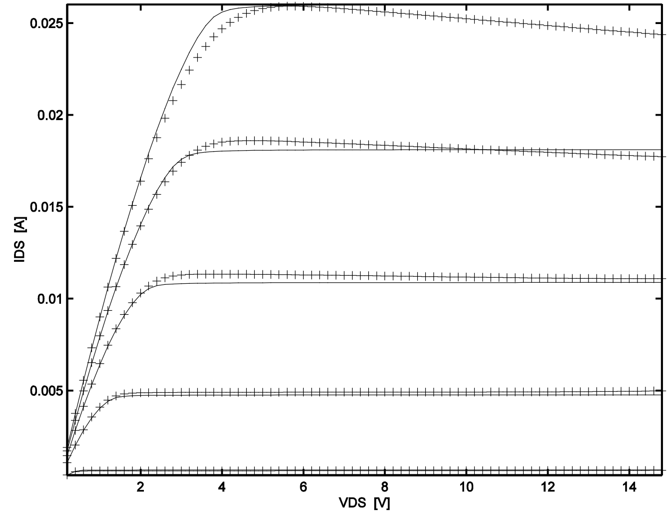


Fig. 3.189 **NMOSHL** output characteristic of a typical wafer. W/L = 100/3,
VGS = 1.0,2.0,3.0,4.0,5.0 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

3.3 Bipolar Transistor Characteristics

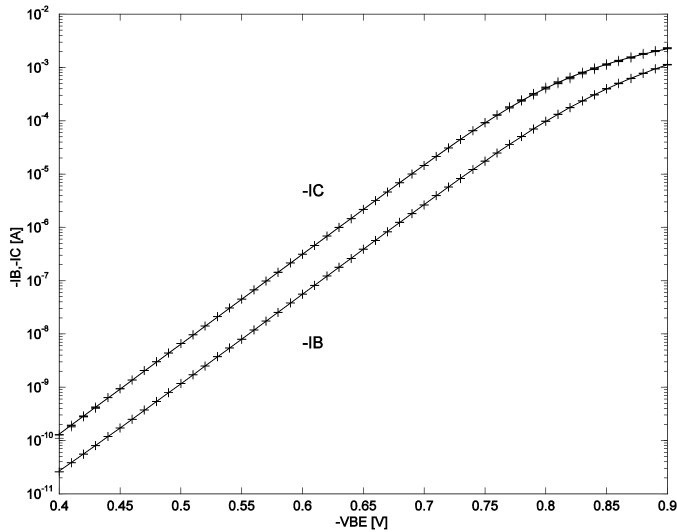


Fig. 3.190 Gummel plot of vertical PNP bipolar transistor (**VERT10**) for a typical wafer.
VBC = 0,0.5,1,1.5,2 V, + = measured, — = SPICE model

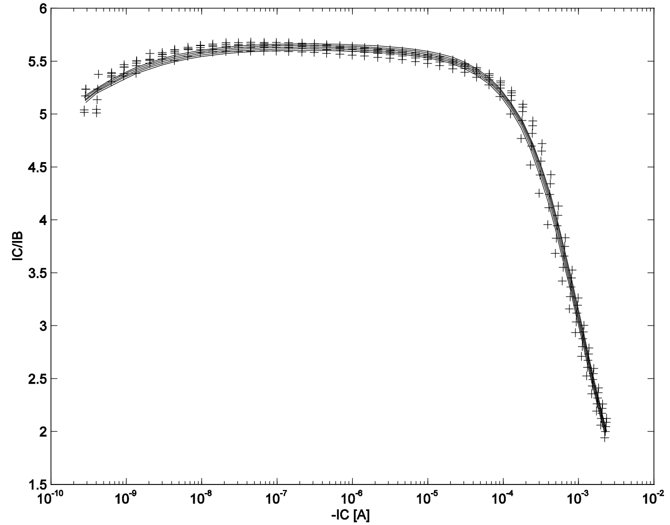


Fig. 3.191 Current gain of vertical PNP bipolar transistor (**VERT10**) for a typical wafer.
VBC = 0,0.5,1,1.5,2 V, + = measured, — = SPICE model

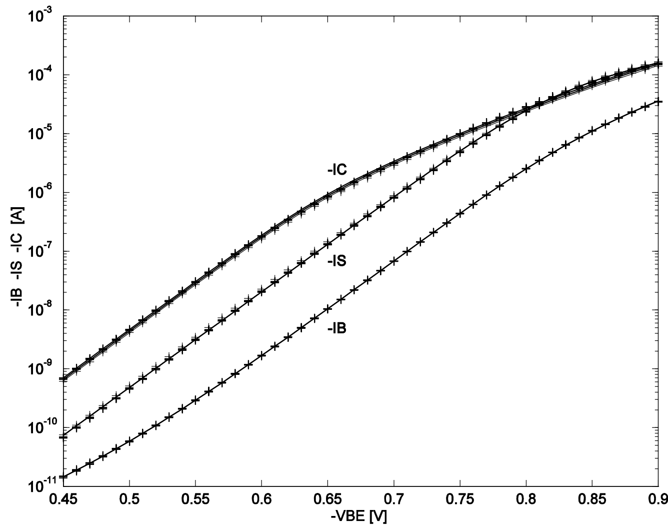


Fig. 3.192 Gummel plot of lateral PNP bipolar transistor (**LAT2**) for a typical wafer.
VBC = 0,1.2,2.4 V, + = measured, — = SPICE model

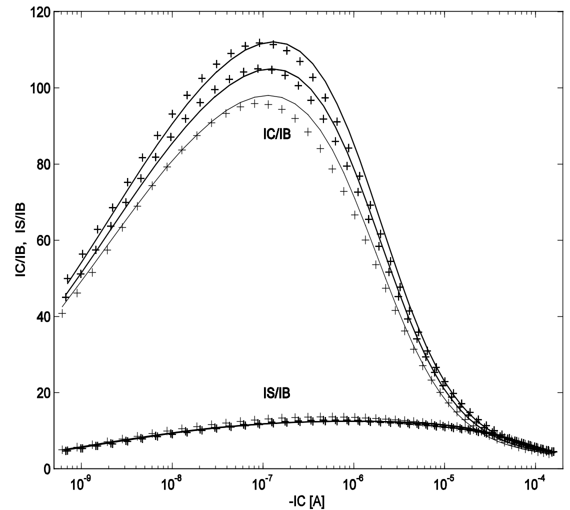


Fig. 3.193 Current gain of lateral PNP bipolar transistor (**LAT2**) for a typical wafer.
VBC = 0,1.2,2.4 V, + = measured, — = SPICE model

3.4 Well Resistor Characteristics

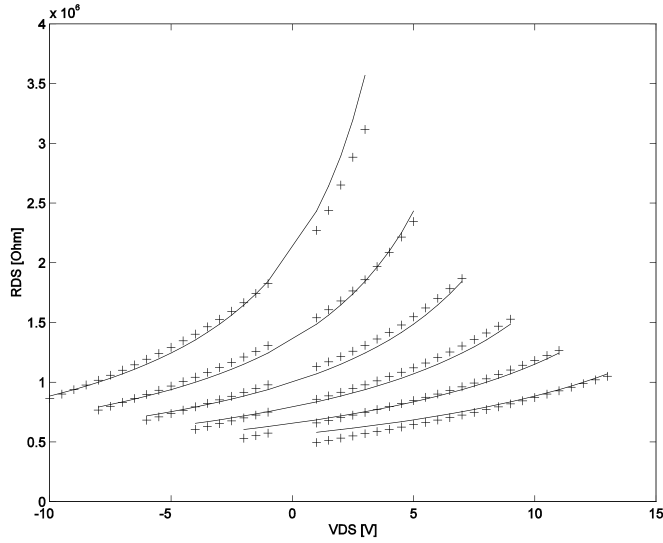


Fig. 3.194 N-well resistor characteristic of a typical wafer. W/L = 1.7/200, -VBS = 0,2,4,6,8,10 V, + = measured, — = SPICE JFET model

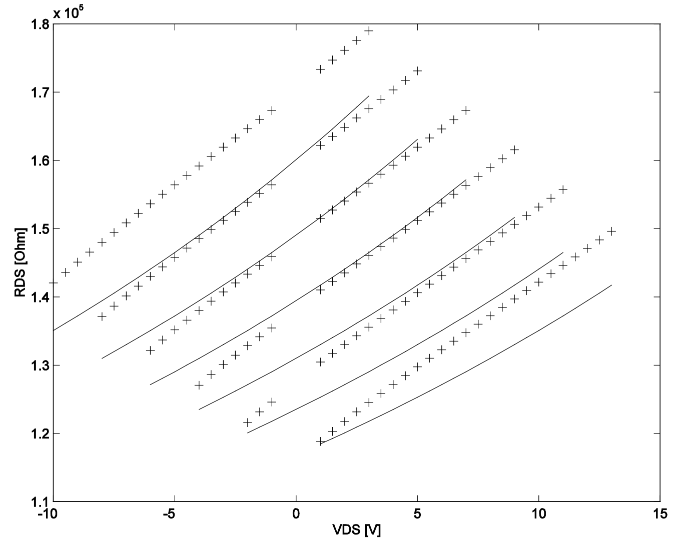


Fig. 3.195 N-well resistor characteristic of a typical wafer. W/L = 3/200 -VBS = 0,2,4,6,8,10 V, + = measured, — = SPICE JFET model

3.5 Poly Resistor Temperature Characteristics

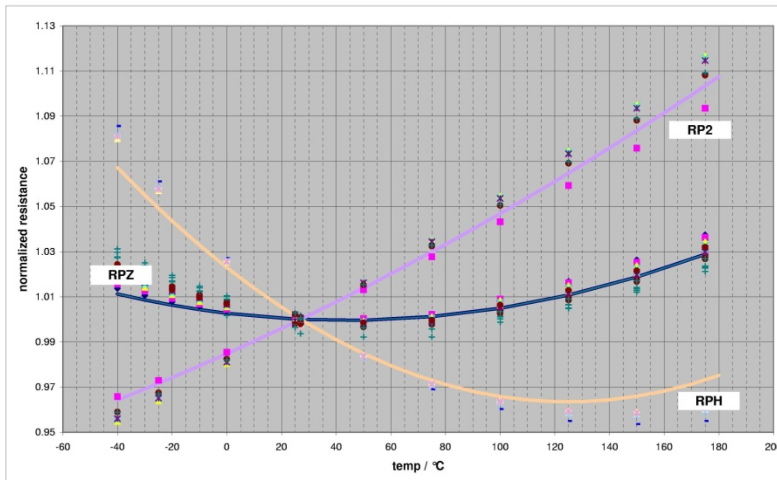


Fig. 3.196 **Poly resistor temperatuer** characteristic for RPOLY2 (RP2) , RPOLYH (RPH) and RPOLYZ (RPZ).
Symbols = measured, — = SPICE Resistor model for different geometries

3.6 Capacitor Characteristics

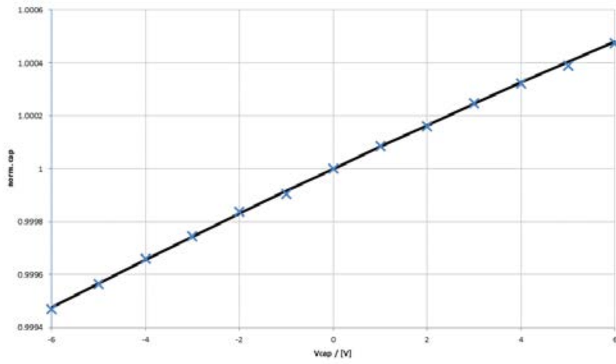


Fig. 3.197 **CPOLY** characteristic of a typical wafer.

+ = measured, — = SPICE Cap model

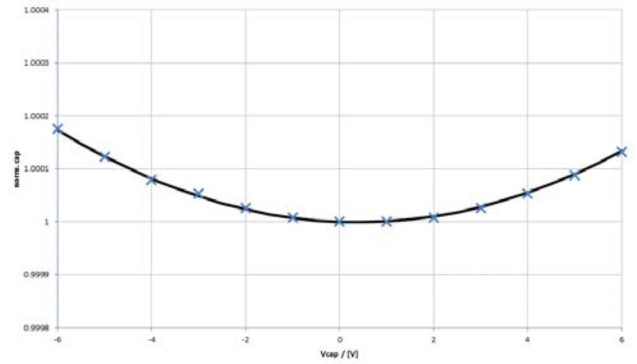


Fig. 3.198 **CMIM** characteristic of a typical wafer.

+ = measured, — = SPICE Cap model

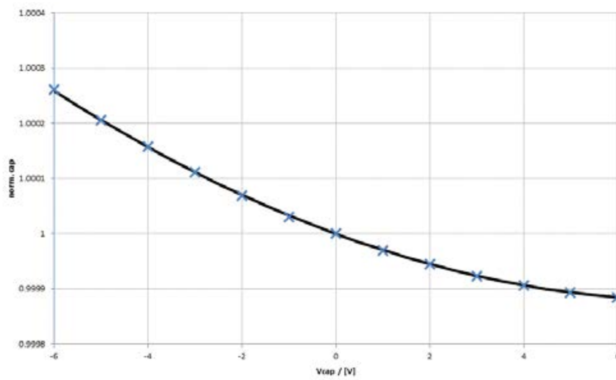


Fig. 3.199 **CPMIM** characteristic of a typical wafer.

+ = measured, — = SPICE Cap model

3.7 Schottky Barrier Diode Characteristics

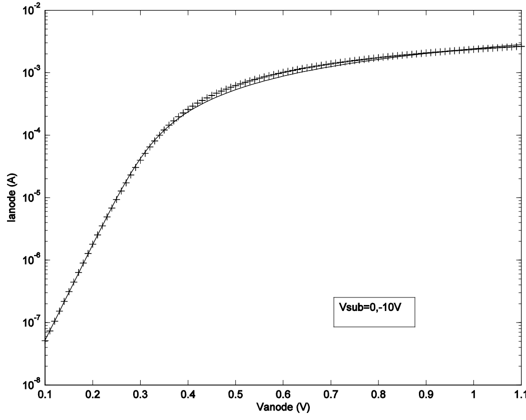


Fig.3.167 **SBD5** anode current vs. anode voltage for Vsub=0, -10V. W/L=0.4/12, + = measured, — = Schottky subcircuit model

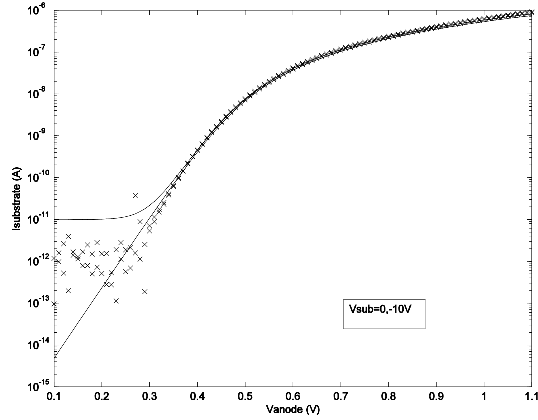


Fig.3.168 **SBD5** Substrate current vs. anode voltage for Vsub=0, -10V. W/L=0.4/12, + = measured, — = Schottky subcircuit model

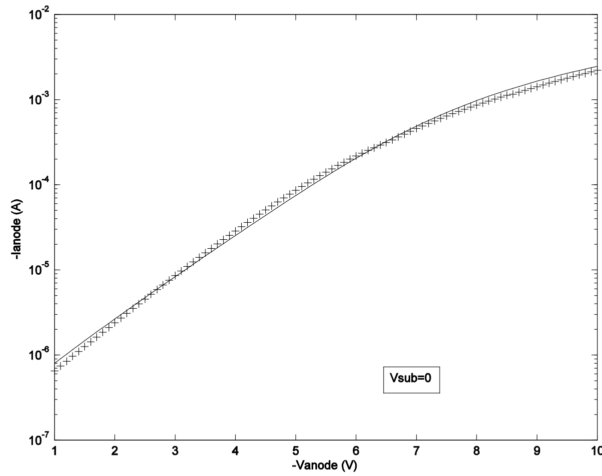


Fig.3.169 **SBD5** reverse anode current vs. anode voltage for Vsub=0V, . W/L=0.4/12

4 Support

For questions on process parameters please refer to:

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