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0.35 um CMOS C35 Design Rules

Seven Digit Document: ENG-183

Revision #: 9.0

Company Confidential

Table of Contents

1 Introduction

1.1 Revision

Revision	Date	Changes	Affected pages
1	2002-03	First version of design rule specification	1 to 44
2	2003-02	Add thick metal module and process C35B4M3	1 to 51
3	2003-07	Add ZD2SM24 Add G01P1, G01P2, R01CT, R01V1, R01V2, R01V3, R01PA, PMOSM_G2 Change CB.E.1, CB.E.2, CB.E.3, CB.E.4, NMOS_G2, A.R.1-5 Delete CB.E.6, CB.E.8, CB.E.10, CB.E.12	1 to 54
4	2004-11	Add RDIFFN Add R01M4 Change OD.C.2, OD.C.3, CB.R.1, ZD2SM24 note, A.R.5 Delete S1M2MC	1 to 54

5	2005-6	Add low VT module
		Add C35A3B0, C35B3C3, C35B3L3, C35B4C0, C35B4M6
		Add LVTDEF, LVTA, LVPTUB
		Add NMOSL, PMOSL, NMOSML, PMOSML, NMOSHL, NMOSMHL
		Add NMOSML_R1, PMOSML_R1
			1 to 61

6	2007-02	Add width/spacing for derived process layers, IPDEF, KEPOUT, NMOSL_G2, NMOSML_G2, electromigration Change number of reticles	1 to 66
7	2008-08	Add low TC poly module Add C35B4Z1, C35B4T1 Add INDDEF, METRES, PROBE, RFDEF Add RPOLYZ Change CB.W.1	1 to 68
8	2008-12	Add RPOLY2P, RPOLY2PH	1 to 71

9	2011-04	Add DEVDEF_pfuse, PCOAT
		Add CPMIM, RPOLY1, PFUSE
		Add L2R001, LDR001, PFR001, PWR001, PYR001
		Change RPOLYH, RPOLYZ
			2-5, 8-10, 12-14, 16, 18, 21, 28, 31, 46, 50, 54, 56, 58

1.2 Process Family

This document is valid for the following 0.35um CMOS processes:

Process name	No. of reticles	Core module	PIP capacitor module	5V gate module	high resistive poly module	low TC poly module	Metal 4 module	Thick metal module	MIM capacitor module	Low VT module
C35A3B0	13	x								
C35B3C0	14	x	x							
C35B3C1	17	x	x	x						
C35B3C3	18	x	x	x	x					
C35B3L3	20	x	x	x	x					x
C35B4C0	16	x	x				x			
C35B4C3	20	x	x	x	x		x			
C35B4T1	20	x	x	x				x		
C35B4M3	22	x	x	x	x			x	x	
C35B4M6	18	x	x		x		x		x	
C35B4Z1	20	x	x	x		x	x			

Core module: p-substrate, 1-poly, 3-metal, 3.3 Volt CMOS process.

PIP capacitor module: poly1-poly2 capacitor, RPOLY2 resistor, RPOLY2P resistor

5V gate module: 5V mid-oxide for MOSFETs

High resistive poly module: High resistive poly resistor RPOLYH, RPOLY2PH resistor

Low TC poly module: Low TC poly resistor RPOLYZ (HRES mask with low TC implant)

Metal 4 module: Thin metal 4

Thick metal module: Thick metal 4

MIM capacitor module: MET2-METCAP capacitor

Low VT module: Low threshold 3.3V and 5V MOSFETs

1.3 Related Documents

Description	Document Number
0.35 um CMOS C35 Process Parameters	ENG-182
0.35 um CMOS C35 RF Spice Models	ENG-188
0.35 um CMOS C35 Noise Parameters	ENG-189
0.35 um CMOS C35 Matching Parameters	ENG-228
C35 ESD Design Rules	ENG-236
Standard Family Cells	ENG-42
Assembly Related Design Rules	ASSY-15

Note

All data represent drawn dimensions. Graphical illustrations are not to scale.

2 General

2.1 Definitions

Process Layers

CONT (CO): contact layer (connects MET1 to DIFF, POLY1, POLY2)
DIFF (OD): diffusion layer
FIMP (PW): p-tub / n-field implant layer
HRES (HR): high resistive layer
LVTA (LV): low threshold adjust layer
LVPTUB (LF): low threshold p-tub layer
LVTDEF (LV): low threshold definition layer
MET1 (M1): metal1 layer
MET2 (M2): metal2 layer
MET3 (M3): metal3 layer, top metal for 3-metal processes
MET4 (M4): standard or thick metal4 layer, top metal for 4-metal processes
METCAP (MC): metal capacitor layer
MIDOX (OD2): mid gate oxide layer (V(GATE)>3.3 Volt)
NLDD (LD): n-LDD implant
NLDD50 (L2): 5 Volt n-LDD implant
NPLUS (NP): n+implant layer
NTUB (NW): n-tub layer
PAD (CB): pad layer
PCOAT (PY): polyimide coating layer
POLY1 (PO): poly1 layer
POLY2 (PO2): poly2 layer
PPLUS (PP): p+implant layer
SFCDEF: excludes SFC from checks and automatic layer generation
VIA1: via1 layer (connects MET2 to MET1)
VIA2: via2 layer (connects MET3 to MET2)
VIA3: via3 layer (connects MET4 to MET3)

Definition Layers

Note: These layers are not used in chip production.
They are necessary for design tools, e.g. design rule check.

CAPDEF: sandwich capacitors
DEVDEF_pfuse (PF): poly fuse definition
DIODE: marks protection diodes for device extraction
HOTTUB: marks HOT_NTUB
INDDEF: inductor definition layer
IPDEF (IP): Intellectual Property definition layer (used in full layout of IP-blocks)
KEPOUT (KO): IP keep out definition layer (reserves free space for IP-blocks)
M1HOLE (M1): metal1 slot (MET1 = MET1 and not M1HOLE)
M2HOLE (M2): metal2 slot (MET2 = MET2 and not M2HOLE)
M3HOLE (M3): metal3 slot (MET3 = MET3 and not M3HOLE)
M4HOLE (M4): metal4 slot (MET4 = MET4 and not M4HOLE)
METRES: metal resistor definition layer (splits nets for LVS)
NOFILL: Avoids automatic generation of fill patterns
PROBE: probe pad
RESDEF: resistor definition layer
RESTRM: resistor definition cut layer (RESDEF = RESDEF and not RESTRM)
RFDEF: RF definition layer (RF model)
SUBDEF: Substrate definition
TUBDEF: n-tub resistor definition layer
ZENER: defines Zener diodes for checks and automatic layer generation

Structures

Note: "and" is a logical intersection. "sizing" is applied per side.

DIFFCON: diffusion contact (CONT and DIFF and not POLY2 and not POLY1)
GATE: DIFF and POLY1
HOT_NDIFF: NDIFF outside NTUB not connected to PSUB
HOT_NTUB: NTUB not connected to highest potential
MTOP: Top Metal (MET3 or MET4)
NDIFF: n+diffusion (DIFF and NPLUS)
NDIFFCON: n+diffusion contact (DIFFCON and NPLUS)
NGATE: NDIFF and POLY1
NTAP: NDIFF and NTUB
PADVIA1: VIA1 and (PAD sizing 5 um)
PADVIA2: VIA2 and (PAD sizing 5 um)
PADVIA3: VIA3 and (PAD sizing 5 um)
PDIFF: p+diffusion (DIFF and PPLUS)
PDIFFCON: p+diffusion contact (DIFFCON and PPLUS)
PGATE: PDIFF and POLY1
POLY1CON: poly1 contact (CONT and POLY1 and not POLY2)
POLY2CON: poly2 contact (CONT and POLY2)
PSUB: p-substrate

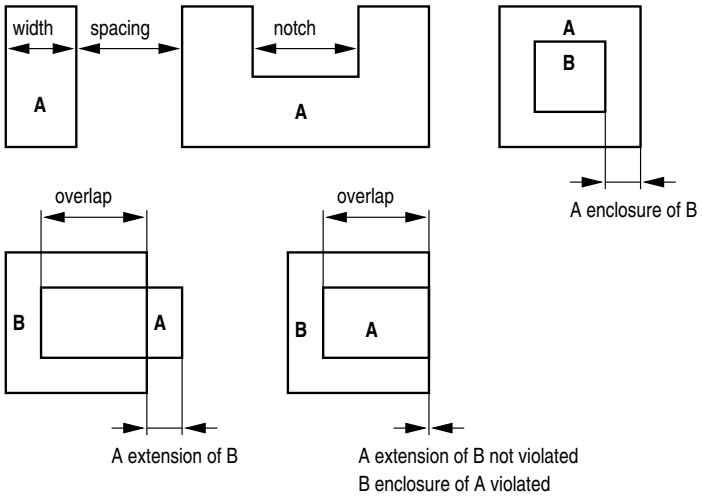
PTAP: PDIFF and not NTUB
SCRIBE: scribe line border
SFC: standard family cells, they contain all process layers
WIDE_METx: METx width and length > 10 um, any METx within 1 um is included

Elements

CMIM: metal2 to metalC capacitor (MET2 and METCAP and not POLY2)
CORNER: corner cell with slotted metal busses
CPMIM: stacked CPOLY / CMIM capacitor (MET2 and METCAP and POLY1 and POLY2)
CPOLY: poly1-poly2 capacitor (POLY1 and POLY2)
CVAR: Varactor - NMOS capacitor in NTUB
LAT2: lateral PNP transistor (2 um x 2 um emitter)
ND: parasitic n+p- diode (NDIFF and PSUB and DIODE)
NMOS: n-channel MOSFET (NGATE and PSUB)
NMOSH: high voltage n-channel MOSFET
NMOSHL: low threshold high voltage n-channel MOSFET
NMOSL: low threshold n-channel MOSFET (NGATE and PSUB and LVTDEF)
NMOSM: n-channel MOSFET with mid gate oxide (NGATE and PSUB and MIDOX)
NMOSMH: high voltage n-channel MOSFET with mid-oxide
NMOSMHL: low threshold high voltage n-channel MOSFET with mid-oxide
NMOSML: low threshold n-channel MOSFET with mid gate oxide (NGATE and PSUB and MIDOX and LVTDEF)
NWD: parasitic n-p- diode (NTUB and PSUB and DIODE)
PD: parasitic p+n- diode (PDIFF and NTUB and DIODE)
PFUSE: poly fuse for programmable elements (POLY1 and DEVDEF_pfuse)
PMOS: p-channel MOSFET (PGATE and NTUB)
PMOSL: low threshold p-channel MOSFET (PGATE and NTUB and LVTDEF)
PMOSM: p-channel MOSFET with mid gate oxide (PGATE and NTUB and MIDOX)
PMOSML: low threshold p-channel MOSFET with mid gate oxide (PGATE and NTUB and MIDOX and LVTDEF)
RDIFFN: n+diffusion resistor (NDIFF and RESDEF and not RESTRM)
RDIFFP: p+diffusion resistor (PDIFF and RESDEF and not RESTRM)
RNWELL: n-tub resistor (NTUB and TUBDEF and not RESTRM)
RPOLY1: poly1 resistor (POLY1 and RESDEF and not DEVDEF_pfuse and not RESTRM)
RPOLY2P: high precision poly2 resistor (POLY2 and RESDEF and not RESTRM, RESDEF label "RPOLY2P")
RPOLY2PH: high precision poly2 resistor (POLY2 and RESDEF and not RESTRM, RESDEF label "RPOLY2PH")
RPOLY2: poly2 resistor (POLY2 and RESDEF and not RESTRM, no RESDEF label)
RPOLYH: high resistive poly2 resistor (POLY2 and HRES and RESDEF and not PPLUS, no HRES label)
RPOLYZ: low TC poly2 resistor (POLY2 and HRES and RESDEF and not PPLUS, HRES label "RPOLYZ")
VERT10: vertical PNP transistor (10 um x 10 um emitter)
ZD2SM24: zener diode for programmable elements (ZENER and DIFF and NTUB)

Geometric Relations

A and B: logical intersection.
A sizing X um: A sized X um per side.
A width: distance inside_A - inside_A
A spacing to B: distance outside_A - outside_B (different polygons)
A notch: distance outside_A - outside_A (same polygon)
A enclosure of B: distance inside_A - outside_B (A contains B)
A extension of B: distance inside_A - outside_B (A may intersect B)
A overlap of B: distance inside_A - inside_B



2.2 Layout Requirements

Guideline	Description	Value
REC001	Grid	integral multiple of 0.025 um
REC002	Corners	90 deg,135 deg
REC003	Data extrema including SCRIBE	integral multiple of 5 um

3 Layer Overview

3.1 Core Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
NTUB	5 / 0	1.7	1.0
FIMP	8 / 0	1.7	1.0
DIFF	10 / 0	0.3	0.6
POLY1	20 / 0	0.35	0.45
NLDD	21 / 0	0.6	0.6
NPLUS	23 / 0	0.6	0.6
PPLUS	24 / 0	0.6	0.6
CONT	34 / 0	0.4	0.4
MET1	35 / 0	0.5	0.45
VIA1	36 / 0	0.5	0.45
MET2	37 / 0	0.6	0.5
VIA2	38 / 0	0.5	0.45
MET3	39 / 0	0.6	0.6
PAD	40 / 0	15	15
PCOAT	59 / 0	15	15
SFCDEF	62 / 2		

Definition Layers

Name_ Purpose	GDS2 Layer / Datatype	Comments
M1HOLE	35 / 1	MET1 slots
M2HOLE	37 / 1	MET2 slots
M3HOLE	39 / 1	MET3 slots
SUBDEF	62 / 3	substrate definition
HOTTUB	62 / 4	HOT_NTUB
IPDEF	62 / 6	IP definition
KEPOUT	62 / 7	free space for IP blocks
NOFILL	62 / 5	no fill patterns allowed
ZENER	62 / 10	zener diode
DIODE	62 / 11	parasitic diodes in schematic
TUBDEF	62 / 12	tub resistor
RESDEF	62 / 13	diffusion and poly resistors
RESTRM	62 / 14	removes RESDEF and TUBDEF
METRES	62 / 15	splits nets for LVS
CAPDEF	62 / 20	sandwich capacitor
INDDEF	62 / 22	inductor
RFDEF	62 / 26	RF definition
PROBE	62 / 27	probe pad
DEVDEF_pfuse	62 / 39	poly fuse

3.2 PIP Capacitor Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
POLY2	30 / 0	0.65	0.5

3.3 5V Gate Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
MIDOX	14 / 0	0.6	0.6
NLDD50	53 / 0	0.6	0.6

3.4 Metal 4 Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
VIA3	41 / 0	0.5	0.45
MET4	42 / 0	0.6	0.6

Definition Layers

Name	GDS2 Number / Datatype	Comments
M4HOLE	42 / 1	MET4 slots

3.5 Thick Metal Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
VIA3	41 / 0	0.5	0.45
MET4	42 / 0	2.5	2

Definition Layers

Name	GDS2 Number / Datatype	Comments
M4HOLE	42 / 1	MET4 slots

3.6 High Resistive Poly Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
HRES	29 / 0	0.6	0.6

3.7 Low TC Poly Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
HRES	29 / 0	0.6	0.6

3.8 MIM Capacitor Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
METCAP	55 / 0	4	0.8

3.9 Low VT Module

Drawn Process Layers

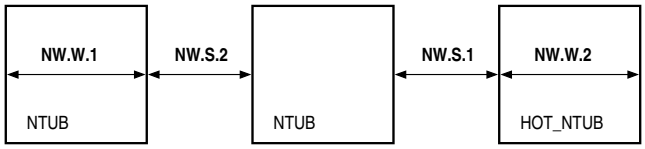
Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
LVTA	46 / 0		
LVPTUB	47 / 0		
LVTDEF	62 / 28	0.6	0.6

4 Layer Rules

4.1 Core Module

4.1.1 NTUB

Rule	Description	Value [um]
NW.W.1	Minimum NTUB width	1.7
NW.W.2	Minimum HOT_NTUB width	3
NW.S.1	Minimum spacing of NTUB with different potential	3
NW.S.2	Minimum spacing of NTUB with same potential	1
NWR001	NTUB overlapping KEPOUT is not allowed	
S1KONW	Minimum NTUB spacing to KEPOUT or SFCDEF (not shown)	3

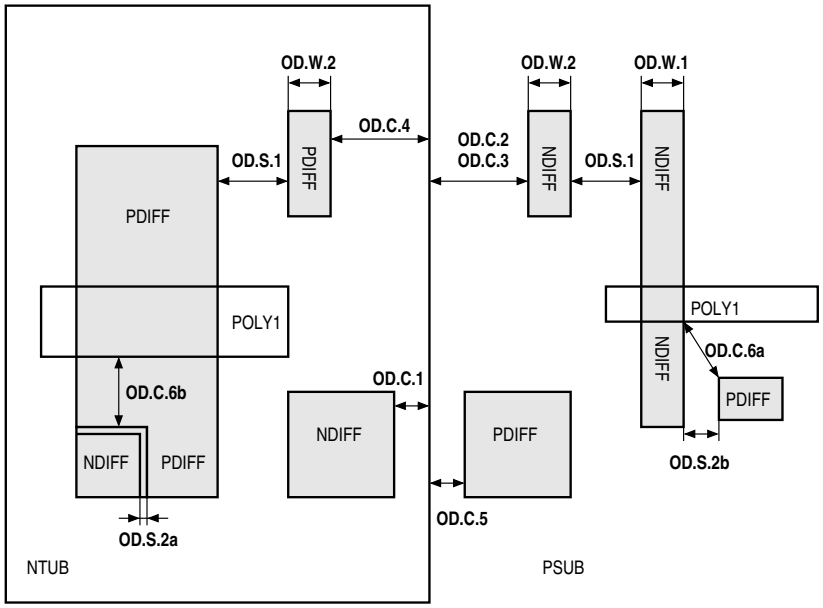


4.1.2 FIMP

Info	Description
PWR001	FIMP outside SFCDEF will be removed and regenerated

4.1.3 DIFF

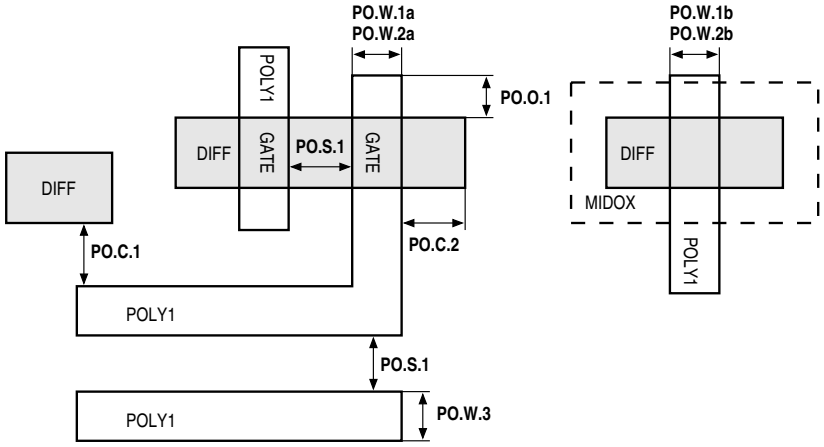
Rule	Description	Value [um]
OD.W.1	Minimum DIFF width to define the width of NMOS / PMOS	0.4
OD.W.2	Minimum DIFF width for interconnection (NDIFF or PDIFF)	0.3
OD.S.1	Minimum DIFF spacing	0.6
OD.C.1	Minimum NTUB enclosure of NDIFF	0.2
OD.C.2	Minimum NDIFF to NTUB spacing	1.2
OD.C.3	Minimum NDIFF to HOT_NTUB spacing (without PTAP in between)	2.6
OD.C.4	Minimum NTUB enclosure of PDIFF	1.2
OD.C.5	Minimum PDIFF to NTUB spacing	0.2
OD.C.6a	Minimum PDIFF to NGATE spacing	0.45
OD.C.6b	Minimum NDIFF to PGATE spacing	0.45
OD.S.2a	Minimum NDIFF to butting PDIFF spacing	0
OD.S.2b	Minimum NDIFF to non-butting PDIFF spacing	0.6
AAR001	DIFF overlapping KEPOUT is not allowed	
S1AAKO	Minimum DIFF spacing to KEPOUT or SFCDEF (not shown)	0.6



4.1.4 POLY1

Rule	Description	Value [um]
PO.W.1a	Minimum GATE length of PMOS	0.35
PO.W.1b	Minimum GATE length of PMOSM	0.5
PO.W.2a	Minimum GATE length of NMOS	0.35
PO.W.2b	Minimum GATE length of NMOSM	0.5
PO.W.3	Minimum POLY1 width for interconnect	0.35
PO.S.1	Minimum POLY1 spacing	0.45
PO.C.1	Minimum POLY1 to DIFF spacing	0.2
PO.C.2	Minimum DIFF extension of GATE	0.5
PO.O.1	Minimum POLY1 extension of GATE	0.4
PO.R.1	Minimum density of POLY1 area [%] Density = total poly layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing. They should not be placed on active devices.	14
P1R002	POLY1 overlapping KEPOUT is not allowed	
S1KOP1	Minimum POLY1 spacing to KEPOUT or SFCDEF (not shown)	0.45

Guideline	Description	Value
G01P1	Maximum ratio of POLY1 area to connected CONT area	18000

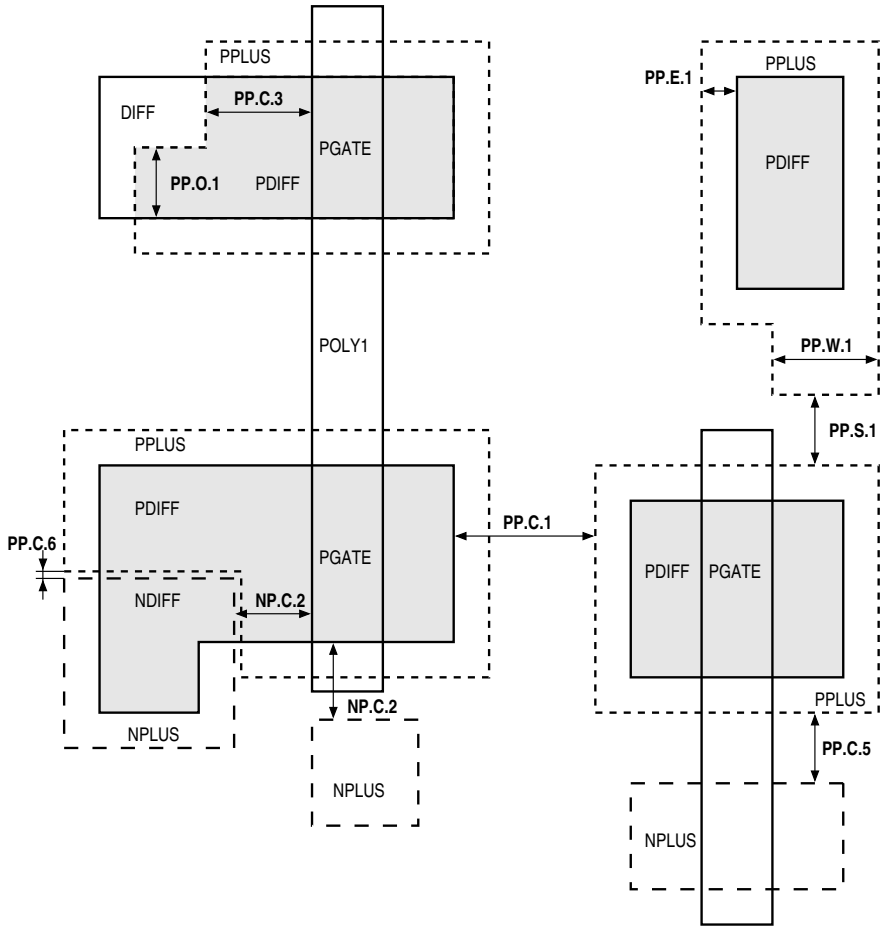


4.1.5 DEVDEF_pfuse

Info	Description
PFR001	DEVDEF_pfuse outside IPDEF is not allowed

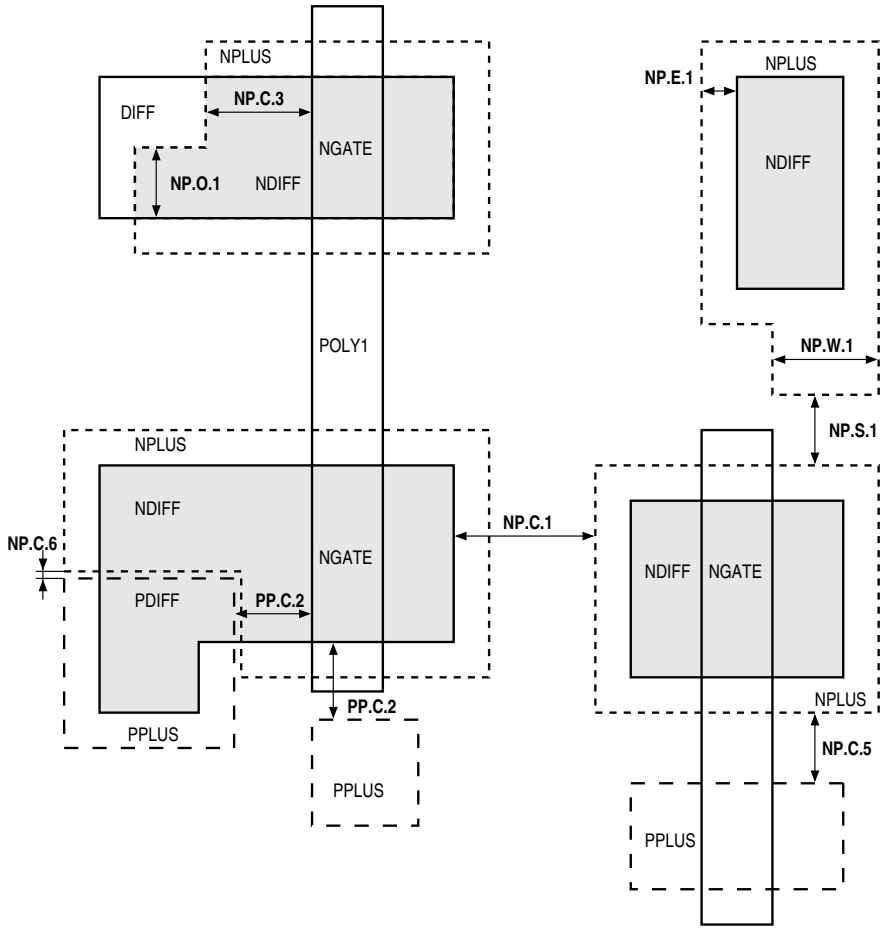
4.1.6 PPLUS

Rule	Description	Value [um]
PP.W.1	Minimum PPLUS width	0.6
PP.S.1	Minimum PPLUS spacing	0.6
PP.C.1	Minimum PPLUS to DIFF spacing	0.35
PP.C.2	Minimum PPLUS to NGATE spacing (shown in NPLUS section)	0.45
PP.C.3	Minimum PPLUS extension of PGATE	0.45
PP.O.1	Minimum overlap of PPLUS and DIFF	0.45
PP.E.1	Minimum PPLUS extension of DIFF	0.25
PP.C.5	Minimum PPLUS to NPLUS spacing on POLY1 Overlap of NPLUS and PPLUS on the same POLY1 region is not allowed	0.25
PP.C.6	Minimum PPLUS to NPLUS spacing on DIFF with same potential	0
PSR001	PPLUS overlapping KEPOUT is not allowed	
S1KOPS	Minimum PPLUS spacing to KEPOUT or SFCDEF (not shown)	0.6



4.1.7 NPLUS

Rule	Description	Value [um]
NP.W.1	Minimum NPLUS width	0.6
NP.S.1	Minimum NPLUS spacing	0.6
NP.C.1	Minimum NPLUS to DIFF spacing	0.35
NP.C.2	Minimum NPLUS to PGATE spacing (shown in PPLUS section)	0.45
NP.C.3	Minimum NPLUS extension of NGATE	0.45
NP.O.1	Minimum overlap of NPLUS and DIFF	0.45
NP.E.1	Minimum NPLUS extension of DIFF	0.25
NP.C.5	Minimum PPLUS to NPLUS spacing on POLY1 Overlap of NPLUS and PPLUS on the same POLY1 region is not allowed	0.25
NP.C.6	Minimum NPLUS to PPLUS spacing on DIFF with same potential	0
NSR001	NPLUS overlapping KEPOUT is not allowed	
S1KONS	Minimum NPLUS spacing to KEPOUT or SFCDEF (not shown)	0.6

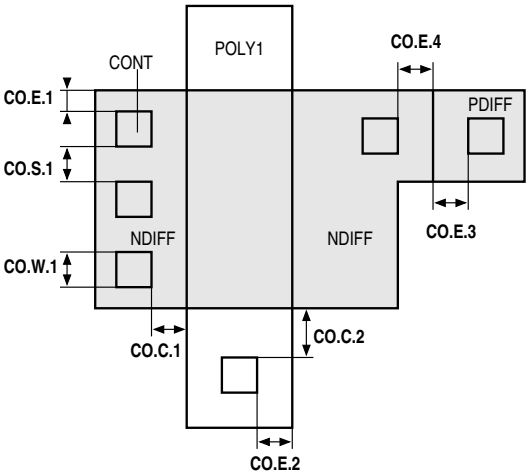


4.1.8 NLDD

Info	Description
LDR001	NLDD outside SFCDEF will be removed and regenerated

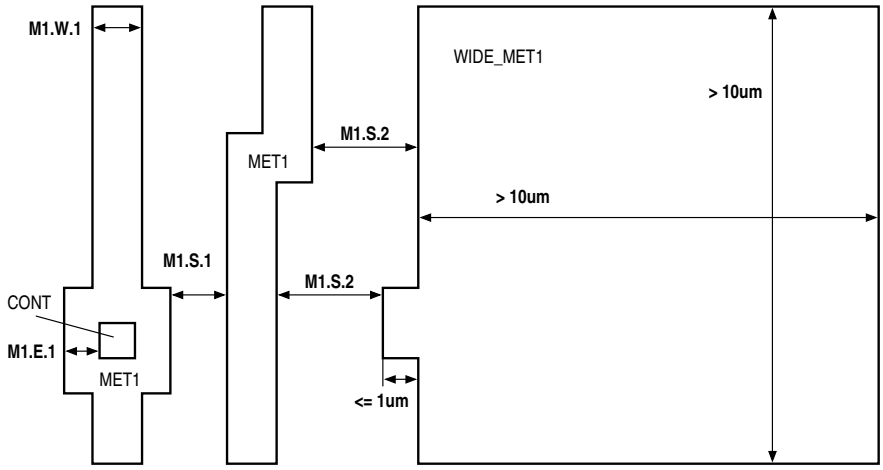
4.1.9 CONT

Rule	Description	Value [um]
CO.W.1	Fixed CONT width	0.4
CO.S.1	Minimum CONT spacing	0.4
CO.C.1	Minimum DIFFCON to GATE spacing	0.3
CO.C.2	Minimum POLY1CON to DIFF spacing	0.4
CO.E.1	Minimum DIFF enclosure of DIFFCON Use as many CONTs as possible.	0.15
CO.E.2	Minimum POLY1 enclosure of POLY1CON	0.2
CO.E.3	Minimum PPLUS enclosure of PDIFFCON	0.25
CO.E.4	Minimum NPLUS enclosure of NDIFFCON	0.25
CO.R.1	POLY1CON on DIFF is not allowed	
CO.R.2	Butted CONT is not allowed	
R01CT	CONT without DIFF or POLY1 or POLY2 is not allowed	
COR002	CONT overlapping KEPOUT is not allowed	
S1COKO	Minimum CONT spacing to KEPOUT or SFCDEF (not shown)	0.4



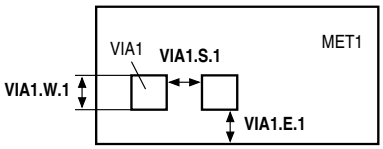
4.1.10 MET1

Rule	Description	Value [um]
M1.W.1	Minimum MET1 width	0.5
M1.S.1	Minimum MET1 spacing	0.45
M1.S.2	Minimum MET1 to WIDE_MET1 spacing	0.8
M1.E.1	Minimum MET1 enclosure of CONT	0.15
M1.R.1	Minimum density of MET1 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing. They should not be placed on active devices.	30
M1R002	MET1 overlapping KEPOUT is not allowed	
S1KOM1	Minimum MET1 spacing to KEPOUT or SFCDEF (not shown)	0.45



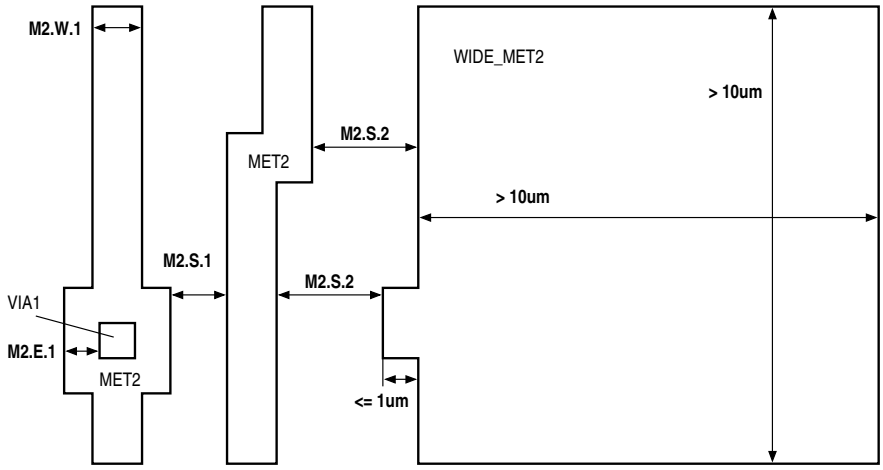
4.1.11 VIA1

Rule	Description	Value [um]
VIA1.0	VIA1 can be located at any region	
VIA1.W.1	Fixed VIA1 width	0.5
VIA1.S.1	Minimum VIA1 spacing	0.45
VIA1.E.1	Minimum MET1 enclosure of VIA1	0.2
VIA1.C.1	VIA1 can be fully or partially stacked on CONT	
R01V1	VIA1 without MET1 is not allowed	
V1R002	VIA1 overlapping KEPOUT is not allowed	
S1KOV1	Minimum VIA1 spacing to KEPOUT or SFCDEF (not shown)	0.45



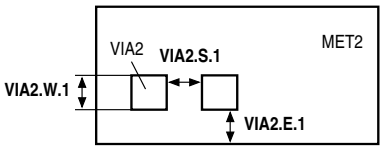
4.1.12 MET2

Rule	Description	Value [um]
M2.W.1	Minimum MET2 width	0.6
M2.S.1	Minimum MET2 spacing	0.5
M2.E.1	Minimum MET2 enclosure of VIA1	0.15
M2.S.2	Minimum MET2 to WIDE_MET2 spacing	0.8
M2.R.1	Minimum density of MET2 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing. They should not be placed on active devices.	30
M2R002	MET2 overlapping KEPOUT is not allowed	
S1KOM2	Minimum MET2 spacing to KEPOUT or SFCDEF (not shown)	0.6



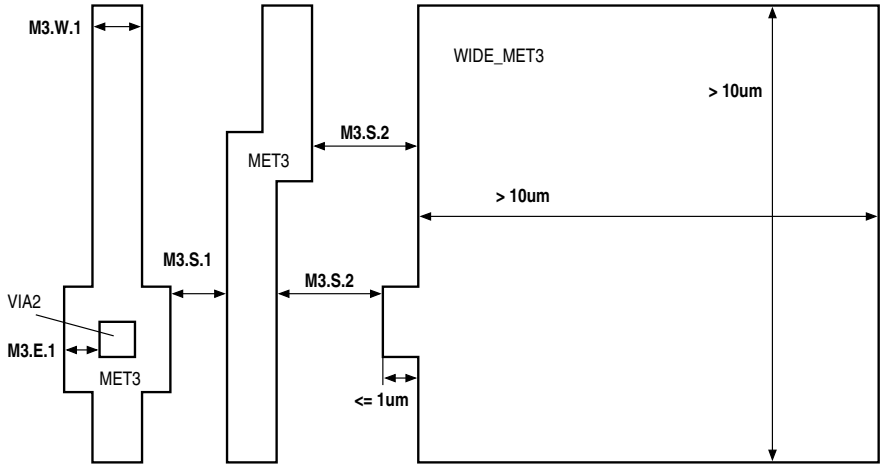
4.1.13 VIA2

Rule	Description	Value [um]
VIA2.0	VIA2 can be located at any region	
VIA2.W.1	Fixed VIA2 width	0.5
VIA2.S.1	Minimum VIA2 spacing	0.45
VIA2.E.1	Minimum MET2 enclosure of VIA2	0.2
VIA2.C.1	VIA2 can be fully or partially stacked on VIA1, CONT	
R01V2	VIA2 without MET2 is not allowed	
V2R002	VIA2 overlapping KEPOUT is not allowed	
S1KOV2	Minimum VIA2 spacing to KEPOUT or SFCDEF (not shown)	0.45



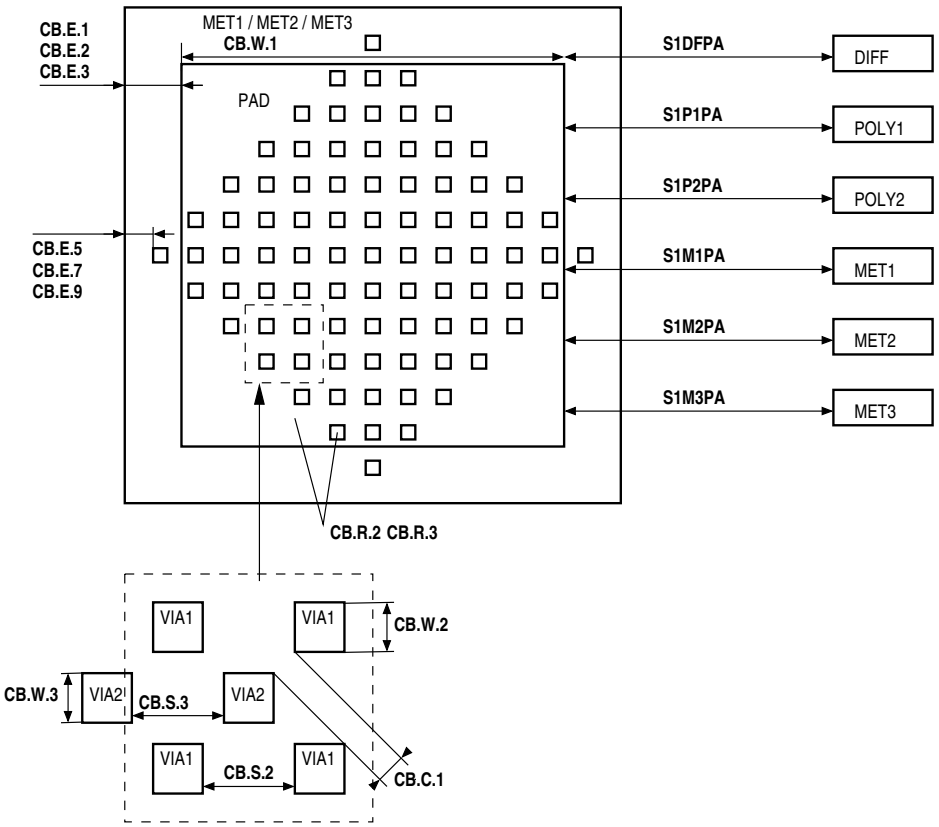
4.1.14 MET3

Rule	Description	Value [um]
M3.W.1	Minimum MET3 width	0.6
M3.S.1	Minimum MET3 spacing	0.6
M3.E.1	Minimum MET3 enclosure of VIA2	0.15
M3.S.2	Minimum MET3 to WIDE_MET3 spacing	0.8
M3.R.1	Minimum density of MET3 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing.	30
M3R002	MET3 overlapping KEPOUT is not allowed	
S1KOM3	Minimum MET3 spacing to KEPOUT or SFCDEF (not shown)	0.6



4.1.15 PAD

Rule	Description	Value [um]
CB.R.1	Bond stack: MET3 / VIA2 / MET2 / VIA1 / MET1 Note: All METx layers must be connected together Note: Different bond stacks need to be cleared by the assembly house	
W1PA	Minimum PAD width	15
CB.W.1	Minimum bonding PAD width (85um preferred, 60um on request)	70
CB.S.1	Minimum PAD spacing	15
CB.E.1	Minimum MET1 enclosure of PAD	5
CB.E.2	Minimum MET2 enclosure of PAD	5
CB.E.3	Minimum MET3 enclosure of PAD	5
CB.E.5	Minimum MET1 enclosure of the nearest PADVIA1	3
CB.E.7	Minimum MET2 enclosure of the nearest PADVIA2 and PADVIA1	3
CB.E.9	Minimum MET3 enclosure of the nearest PADVIA2	3
CB.W.2	Fixed PADVIA1 width	0.5
CB.W.3	Fixed PADVIA2 width	0.5
CB.S.2	Minimum PADVIA1 spacing	0.8
CB.S.3	Minimum PADVIA2 spacing	0.8
CB.C.1	Minimum PADVIA2 to PADVIA1 spacing	0.3
CB.R.2	Minimum ratio of PADVIA1 area to PAD area [%]	5
CB.R.3	Minimum ratio of PADVIA2 area to PAD area [%]	5
S1DFPA	Minimum PAD to DIFF spacing	9
S1P1PA	Minimum PAD to POLY1 spacing	9
S1P2PA	Minimum PAD to POLY2 spacing	9
S1M1PA	Minimum PAD to MET1 spacing (different net)	9
S1M2PA	Minimum PAD to MET2 spacing (different net)	9
S1M3PA	Minimum PAD to MET3 spacing (different net)	9
R01PA	PAD without MET3 is not allowed	
PAR002	PAD overlapping KEPOUT is not allowed	
S1KOPA	Minimum PAD spacing to KEPOUT or SFCDEF (not shown)	9



4.1.16 PCOAT

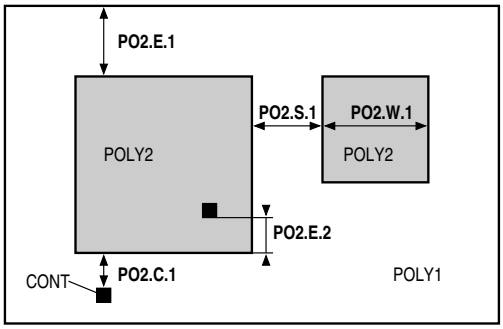
Info	Description
PYR001	PCOAT outside SFCDEF will be removed and regenerated

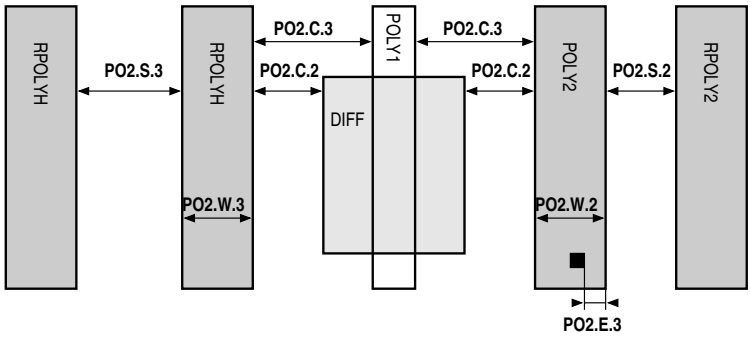
4.2 PIP Capacitor Module

4.2.1 POLY2

Rule	Description	Value [um]
PO2.W.1	Minimum CPOLY width	0.8
PO2.W.2	Minimum POLY2 width	0.65
PO2.W.3	Minimum RPOLYH width	0.8
PO2.S.1	Minimum CPOLY spacing	0.65
PO2.S.2	Minimum POLY2 spacing	0.5
PO2.S.3	Minimum RPOLYH spacing	0.75
PO2.C.1	Minimum POLY1CON to CPOLY spacing	1.2
PO2.C.2	Minimum DIFF to POLY2 spacing	0.2
PO2.C.3	Minimum POLY1 to POLY2 spacing	0.65
PO2.E.1	Minimum POLY1 enclosure of CPOLY	1
PO2.E.2	Minimum CPOLY enclosure of POLY2CON	0.6
PO2.E.3	Minimum POLY2 enclosure of POLY2CON	0.25
PO2.R.1	POLY2 on DIFF is not allowed	
P2R002	POLY2 overlapping KEPOUT is not allowed	
S1KOP2	Minimum POLY2 spacing to KEPOUT or SFCDEF (not shown)	0.6

Guideline	Description	Value
G01P2	Maximum ratio of POLY2 area to connected CONT area	22000

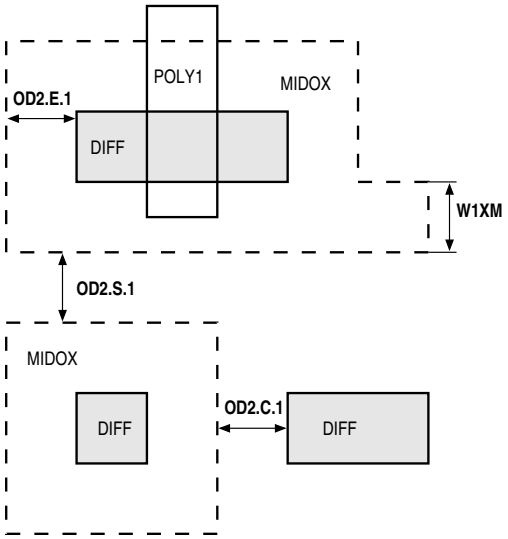

PO2.E.1
POLY2
PO2.S.1
PO2.W.1
POLY2
PO2.E.2
CONT
PO2.C.1
POLY1


RPOLYH
PO2.S.3
RPOLYH
PO2.C.3
PO2.C.2
POLY1
DIFF
PO2.C.3
PO2.C.2
POLY2
PO2.S.2
RPOLY2
PO2.W.3
PO2.W.2
PO2.E.3

4.3 5V Gate Module

4.3.1 MIDOX

Rule	Description	Value [um]
W1XM	Minimum MIDOX width	0.6
OD2.E.1	Minimum MIDOX enclosure of DIFF	0.6
OD2.S.1	Minimum MIDOX spacing	0.6
OD2.C.1	Minimum MIDOX to DIFF spacing	0.6
BAD1XM	MIDOX outside GATE is not allowed	
XMR002	MIDOX overlapping KEPOUT is not allowed	
S1KOXM	Minimum MIDOX spacing to KEPOUT or SFCDEF (not shown)	0.6



4.3.2 NLDD50

Info	Description
L2R001	NLDD50 outside SFCDEF will be removed and regenerated

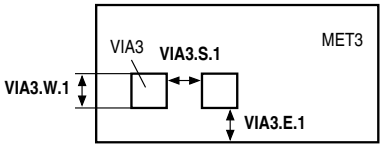
4.4 Metal 4 Module

4.4.1 MET3

Rule	Description	Value [um]
M3.S.1	Minimum MET3 spacing	0.5

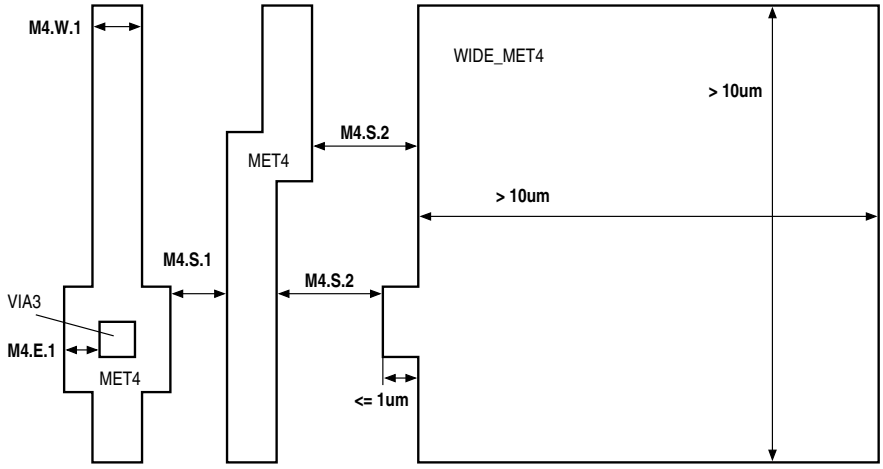
4.4.2 VIA3

Rule	Description	Value [um]
VIA3.0	VIA3 can be located at any region	
VIA3.W.1	Fixed VIA3 width	0.5
VIA3.S.1	Minimum VIA3 spacing	0.45
VIA3.E.1	Minimum MET3 enclosure of VIA3	0.2
VIA3.C.1	VIA3 can be fully or partially stacked on VIA2, VIA1, CONT	
R01V3	VIA3 without MET3 is not allowed	
V3R002	VIA3 overlapping KEPOUT is not allowed	
S1KOV3	Minimum VIA3 spacing to KEPOUT or SFCDEF (not shown)	0.45



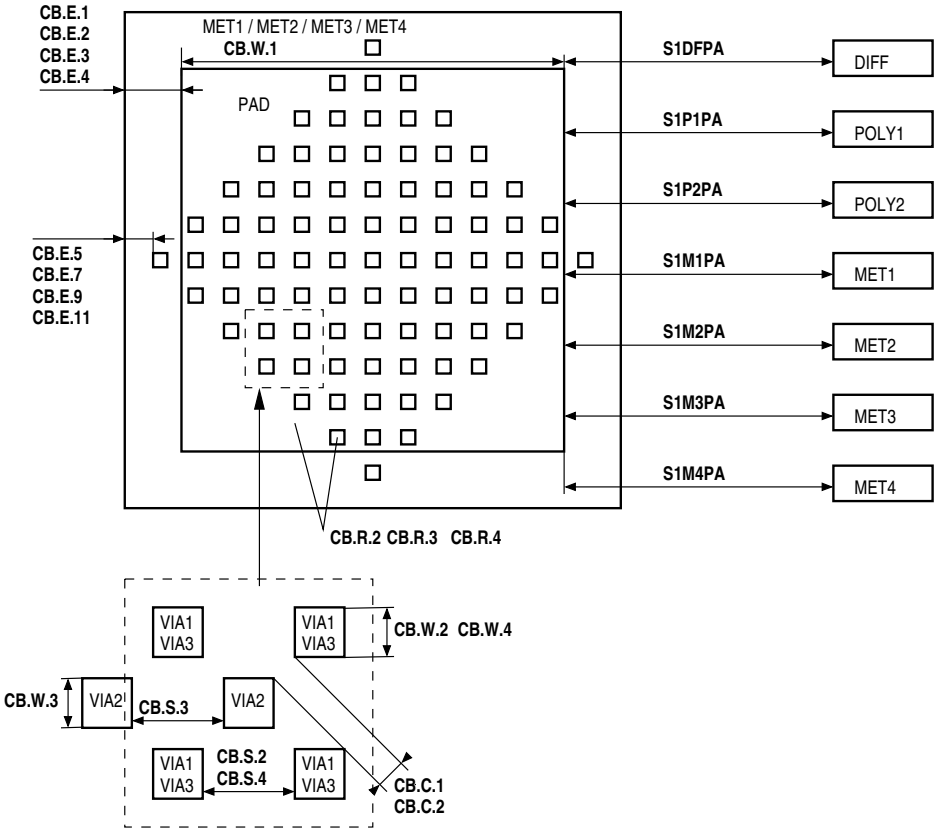
4.4.3 MET4

Rule	Description	Value [um]
M4.W.1	Minimum MET4 width	0.6
M4.S.1	Minimum MET4 spacing	0.6
M4.E.1	Minimum MET4 enclosure of VIA3	0.15
M4.S.2	Minimum MET4 to WIDE_MET4 spacing	0.8
M4.R.1	Minimum density of MET4 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing.	30
M4R002	MET4 overlapping KEPOUT is not allowed	
S1KOM4	Minimum MET4 spacing to KEPOUT or SFCDEF (not shown)	0.6



4.4.4 PAD

Rule	Description	Value [um]
CB.R.1	Bond stack: MET4 / MET3 / VIA2 / MET2 / VIA1 / MET1 Note: All METx layers must be connected together Note: Different bond stacks need to be cleared by the assembly house	
CB.E.4	Minimum MET4 enclosure of PAD	5
CB.E.9	Minimum MET3 enclosure of the nearest PADVIA3 and PADVIA2	3
CB.E.11	Minimum MET4 enclosure of the nearest PADVIA3	3
CB.W.4	Fixed PADVIA3 width	0.5
CB.S.4	Minimum PADVIA3 spacing	0.8
CB.C.2	Minimum PADVIA3 to PADVIA2 spacing	0.3
CB.R.4	Minimum ratio of PADVIA3 area to PAD area [%]	5
S1M4PA	Minimum PAD to MET4 spacing (different net)	9
R01PA	PAD without MET4 is not allowed	



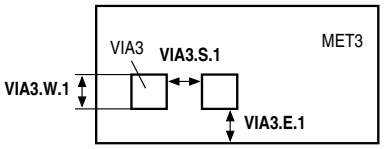
4.5 Thick Metal Module

4.5.1 MET3

Rule	Description	Value [um]
M3.S.1	Minimum MET3 spacing	0.5

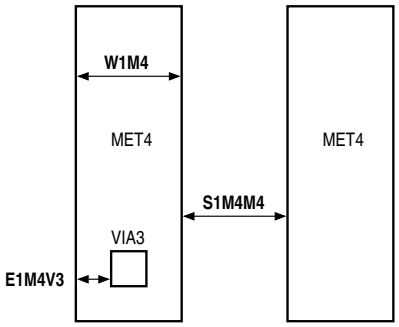
4.5.2 VIA3

Rule	Description	Value [um]
VIA3.0	VIA3 can be located at any region	
VIA3.W.1	Fixed VIA3 width	0.5
VIA3.S.1	Minimum VIA3 spacing	0.45
VIA3.E.1	Minimum MET3 enclosure of VIA3	0.2
VIA3.C.1	VIA3 can be fully or partially stacked on VIA2, VIA1, CONT	
R01V3	VIA3 without MET3 is not allowed	
V3R002	VIA3 overlapping KEPOUT is not allowed	
S1KOV3	Minimum VIA3 spacing to KEPOUT or SFCDEF (not shown)	0.45



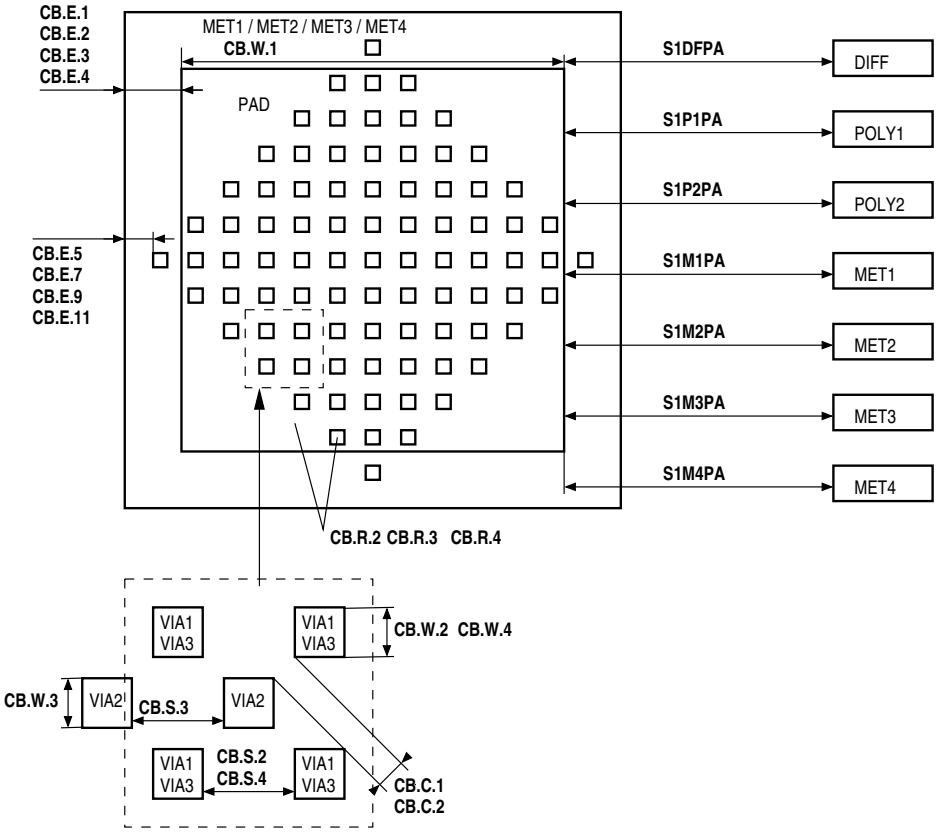
4.5.3 MET4

Rule	Description	Value [um]
W1M4	Minimum MET4 width	2.5
S1M4M4	Minimum MET4 spacing	2
E1M4V3	Minimum MET4 enclosure of VIA3	0.5
R01M4	Minimum density of MET4 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2.5um rectangles with 4um spacing.	30
M4R002	MET4 overlapping KEPOUT is not allowed	
S1KOM4	Minimum MET4 spacing to KEPOUT or SFCDEF (not shown)	2



4.5.4 PAD

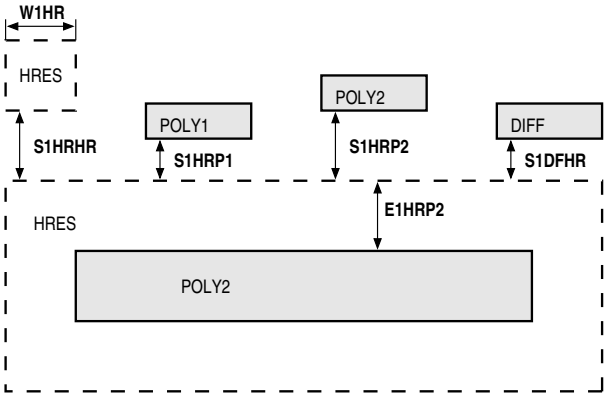
Rule	Description	Value [um]
CB.R.1	Bond stack: MET4 / MET3 / VIA2 / MET2 / VIA1 / MET1 Note: All METx layers must be connected together Note: Different bond stacks need to be cleared by the assembly house	
CB.E.4	Minimum MET4 enclosure of PAD	5
CB.E.9	Minimum MET3 enclosure of the nearest PADVIA3 and PADVIA2	3
CB.E.11	Minimum MET4 enclosure of the nearest PADVIA3	3
CB.W.4	Fixed PADVIA3 width	0.5
CB.S.4	Minimum PADVIA3 spacing	0.8
CB.C.2	Minimum PADVIA3 to PADVIA2 spacing	0.3
CB.R.4	Minimum ratio of PADVIA3 area to PAD area [%]	5
S1M4PA	Minimum PAD to MET4 spacing (different net)	9
R01PA	PAD without MET4 is not allowed	



4.6 High Resistive Poly Module

4.6.1 HRES

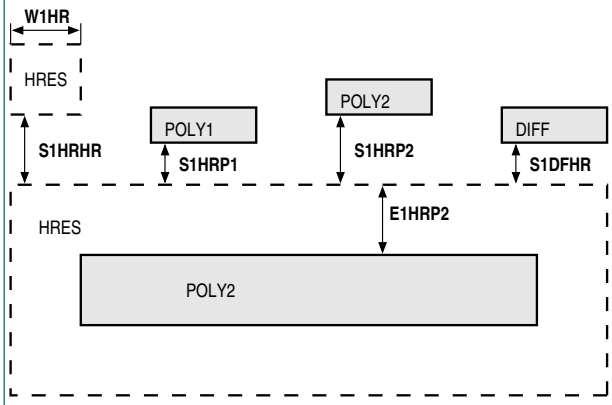
Rule	Description	Value [um]
W1HR	Minimum HRES width	0.6
S1HRHR	Minimum HRES spacing	0.6
BAD1HR	HRES is not allowed over DIFF	
BAD2HR	HRES is not allowed over NPLUS	
BAD3HR	HRES is not allowed over POLY1	
E1HRP2	Minimum HRES enclosure of POLY2	3
S1HRP1	Minimum HRES to POLY1 spacing	0.35
S1HRP2	Minimum HRES to POLY2 spacing	3
S1DFHR	Minimum HRES to DIFF spacing	0.35
HRR004	HRES overlapping KEPOUT is not allowed	
S1HRKO	Minimum HRES spacing to KEPOUT or SFCDEF (not shown)	0.6



4.7 Low TC Poly Module

4.7.1 HRES

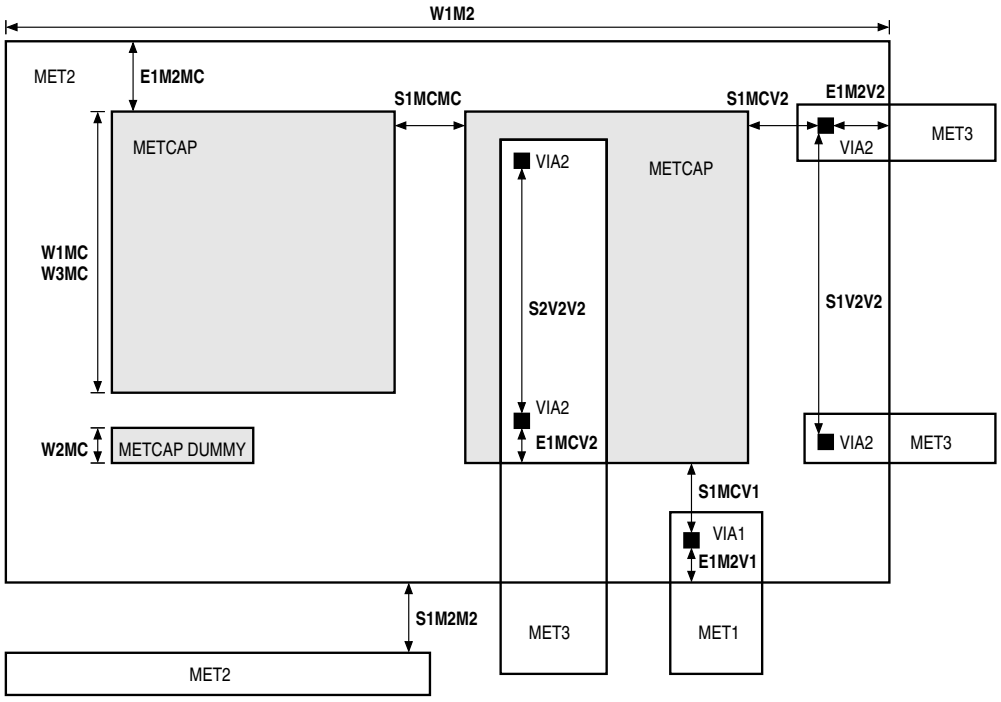
Rule	Description	Value [um]
W1HR	Minimum HRES width	0.6
S1HRHR	Minimum HRES spacing	0.6
BAD1HR	HRES is not allowed over DIFF	
BAD2HR	HRES is not allowed over NPLUS	
BAD3HR	HRES is not allowed over POLY1	
E1HRP2	Minimum HRES enclosure of POLY2	3
S1HRP1	Minimum HRES to POLY1 spacing	0.35
S1HRP2	Minimum HRES to POLY2 spacing	3
S1DFHR	Minimum HRES to DIFF spacing	0.35
HRR004	HRES overlapping KEPOUT is not allowed	
S1HRKO	Minimum HRES spacing to KEPOUT or SFCDEF (not shown)	0.6



4.8 MIM Capacitor Module

4.8.1 METCAP

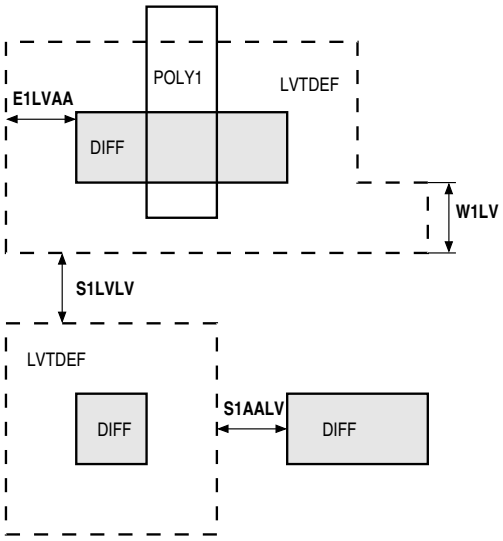
Rule	Description	Value [um]
W1MC	Minimum METCAP width	4
W2MC	Minimum dummy METCAP width	0.5
W3MC	Maximum METCAP size	30
W1M2	Maximum MET2 width (capacitor bottom plate)	35
S1MCMC	Minimum METCAP spacing	0.8
S1M2M2	Minimum MET2 spacing (capacitor bottom plate)	0.8
S1MCV1	Minimum spacing between VIA1 and METCAP	0.5
S1MCV2	Minimum spacing between VIA2 and METCAP	0.5
S1V2V2	Minimum VIA2 spacing on MET2 bottom plate outside METCAP	4
S2V2V2	Minimum VIA2 spacing on METCAP	3.5
E1M2MC	Minimum MET2 enclosure of METCAP	1
E1M2V1	Minimum MET2 enclosure of VIA1 (capacitor bottom plate)	0.2
E1M2V2	Minimum MET2 enclosure of VIA2 (capacitor bottom plate)	0.2
E1MCV2	Minimum METCAP enclosure of VIA2	0.5
R1MC	Minimum METCAP density [%]	3
R1V2	Minimum VIA2 density inside METCAP [%]	1
BAD1M1	MET1 under METCAP region is not allowed	
MCR002	METCAP overlapping KEPOUT is not allowed	
S1MCKO	Minimum METCAP spacing to KEPOUT or SFCDEF (not shown)	0.8


W1M2
MET2
E1M2MC
S1MCMC
S1MCV2
E1M2V2
MET3
VIA2
METCAP
VIA2
METCAP
W1MC
W3MC
S2V2V2
S1V2V2
VIA2
W2MC
METCAP DUMMY
E1MCV2
VIA2
MET3
S1MCV1
VIA1
E1M2V1
S1M2M2
MET3
MET1
MET2

4.9 Low VT Module

4.9.1 LVTDEF

Rule	Description	Value [um]
W1LV	Minimum LVTDEF width	0.6
S1LVLV	Minimum LVTDEF spacing	0.6
E1LVAA	Minimum LVTDEF enclosure of DIFF	0.25
S1AALV	Minimum LVTDEF to DIFF spacing	0.35
LVR001	LVTDEF over ZENER is not allowed	
LVR002	LVTDEF outside GATE is not allowed	
LVR004	LVTDEF overlapping KEPOUT is not allowed	
S1KOLV	Minimum LVTDEF spacing to KEPOUT or SFCDEF (not shown)	0.6



4.9.2 LVTA

Rule	Description
LVR003	LVTA outside SFCDEF will be removed and regenerated

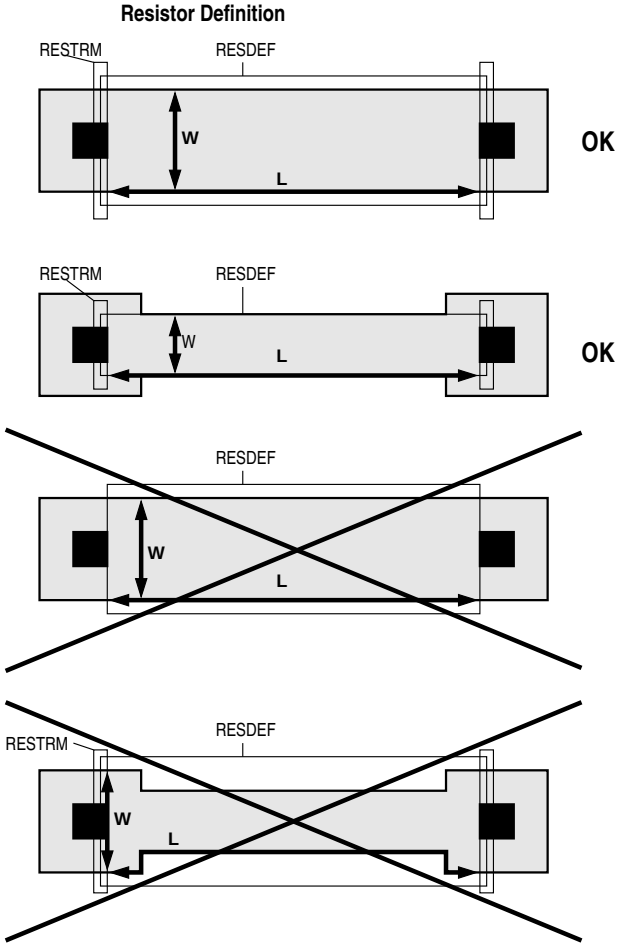
4.9.3 LVPTUB

Rule	Description
LFR001	LVPTUB outside SFCDEF will be removed and regenerated

5 Element Rules

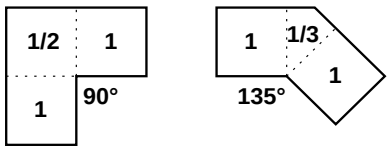
5.1 Layout Conventions

5.1.1 Resistor Definition



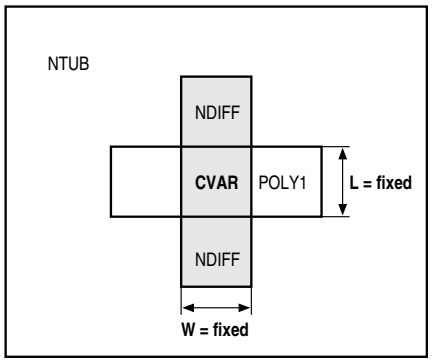
5.1.2 Resistor Corner Correction

Use the following effective number of squares to calculate the resistance of corners:



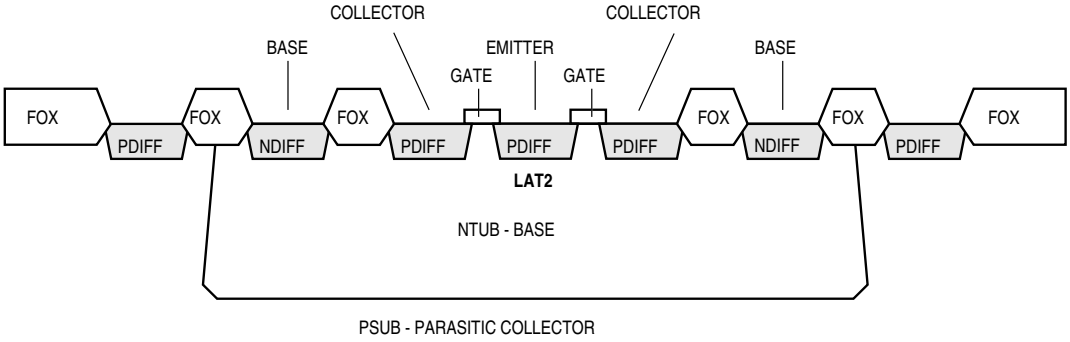
5.2 Core Module

5.2.1 CVAR



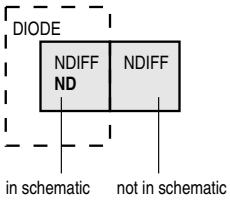
Note: The layout of CVAR units are predefined and available on request.

5.2.2 LAT2



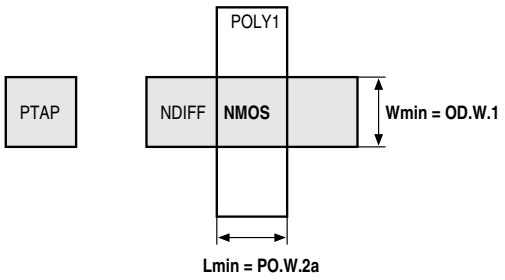
Note: The layout of LAT2 is predefined and available on request. It must not be changed.

5.2.3 ND



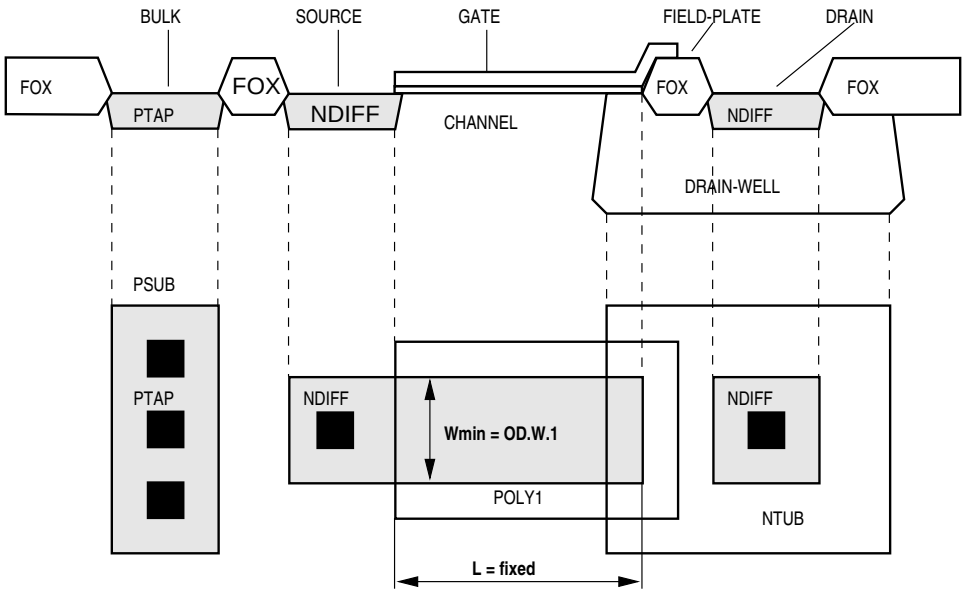
Note: ND is only intended for simulation of reverse leakage currents and junction capacitances. It is not recommended to use this diode as an active circuit element.

5.2.4 NMOS



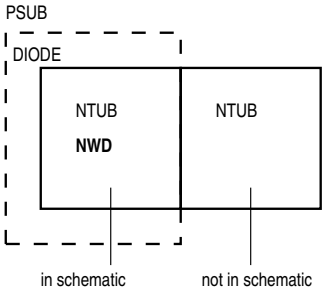
Guideline	Description	Value [um]
NMOS_G1	Precision analog NMOS should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.	
NMOS_G2	Minimum channel length for critical analog NMOS transistors Critical analog NMOS transistors are: 1. Transistors biased at (Vth < VGS < VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	0.7

5.2.5 NMOSH



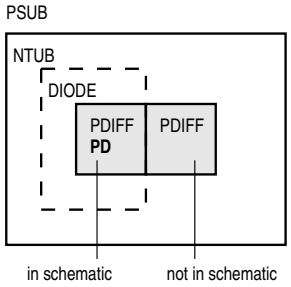
Note: The layout of NMOSH is predefined and available on request. Only W may be changed.

5.2.6 NWD



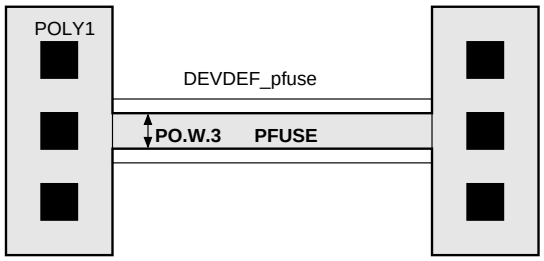
Note: NWD is only intended for simulation of reverse leakage currents and junction capacitances. It is not recommended to use this diode as an active circuit element.

5.2.7 PD



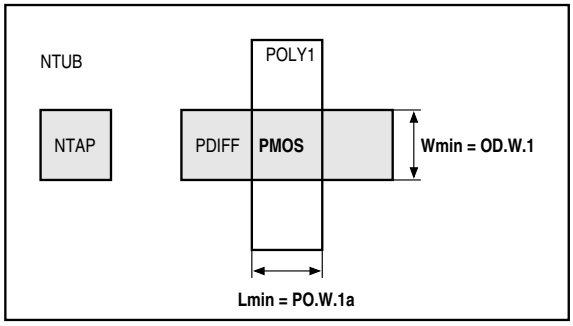
Note: PD is only intended for simulation of reverse leakage currents and junction capacitances. It is not recommended to use this diode as an active circuit element.

5.2.8 PFUSE



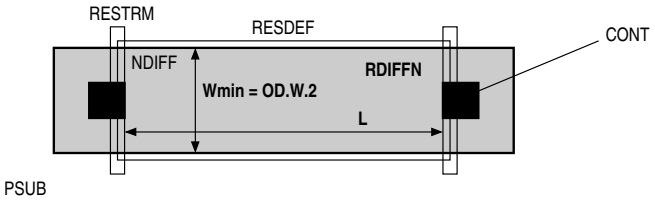
Note: The layout of the poly fuse PFUSE is fixed.
PFUSE can only be used for programming in qualified programmable blocks.

5.2.9 PMOS

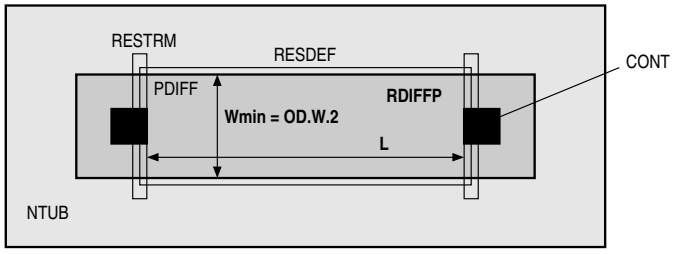


Guideline	Description
PMOS_G1	Precision analog PMOS should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.

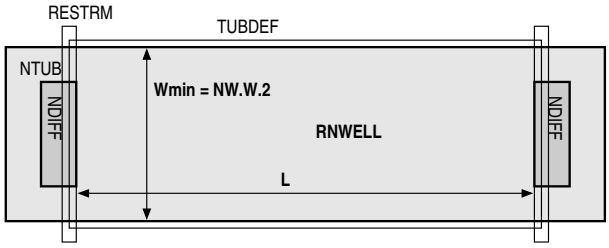
5.2.10 RDIFFN



5.2.11 RDIFFP

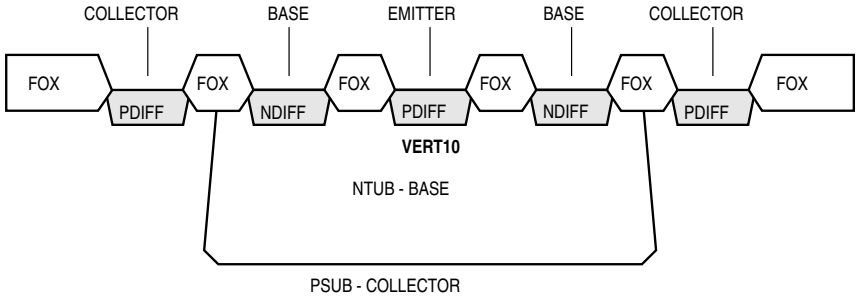


5.2.12 RNWELL



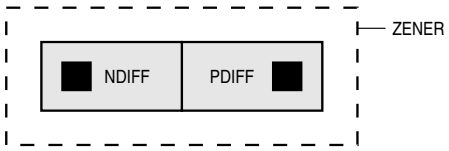
Guideline	Description	Value
RNWELL_G1	Minimum number of RNWELL squares	5

5.2.13 VERT10



Note: The layout of VERT10 is predefined and available on request. It must not be changed.

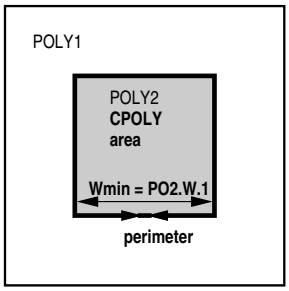
5.2.14 ZD2SM24



Note: The layout of the zener diode ZD2SM24 is fixed.
ZD2SM24 can only be used for programming in qualified zap blocks.

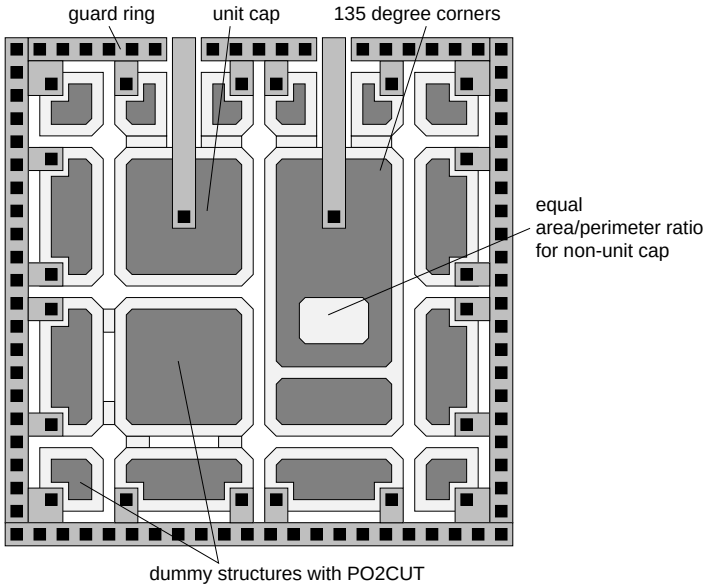
5.3 PIP Capacitor Module

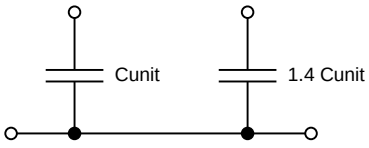
5.3.1 CPOLY



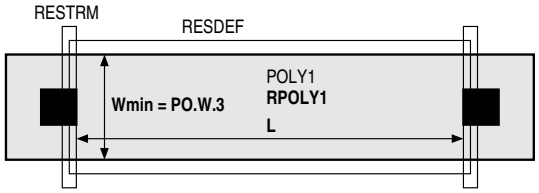
Guideline	Description
CPOLY_G1	PPLUS on CPOLY is not allowed
CPOLY_G2	NPLUS on CPOLY is not allowed

CPOLY Example





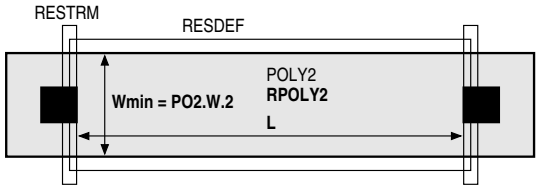
5.3.2 RPOLY1



Rule	Description
RPOLY1_R1	PPLUS on RPOLY1 is not allowed
RPOLY1_R2	NPLUS on RPOLY1 is not allowed

Guideline	Description	Value
RPOLY1_G1	Minimum number of RPOLY1 squares	5

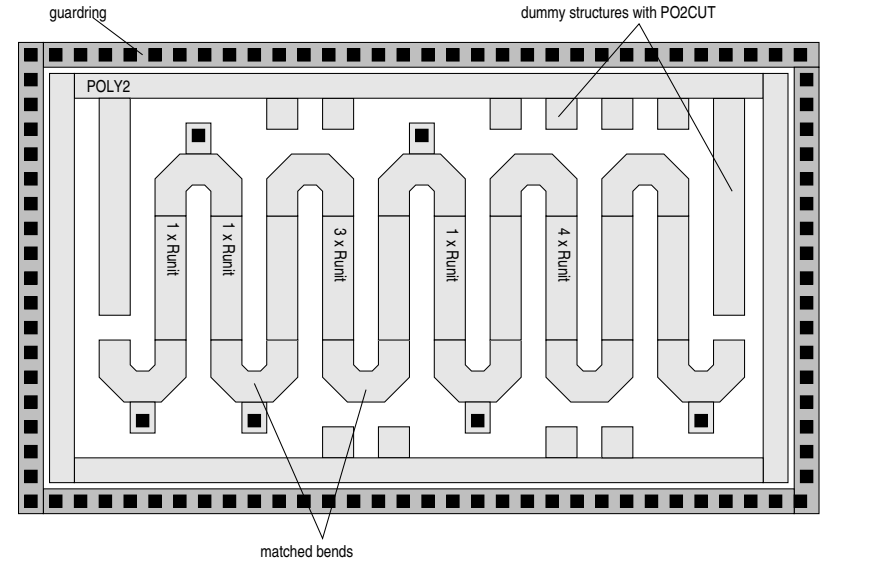
5.3.3 RPOLY2



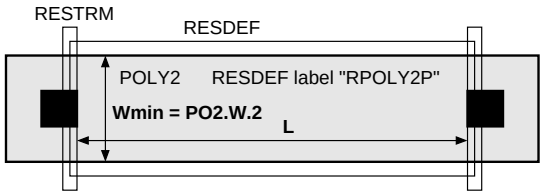
Rule	Description
RPOLY2_R1	PPLUS on RPOLY2 is not allowed
RPOLY2_R2	NPLUS on RPOLY2 is not allowed

Guideline	Description	Value
RPOLY2_G1	Minimum number of RPOLY2 squares	5

RPOLY2 Example



5.3.4 RPOLY2P

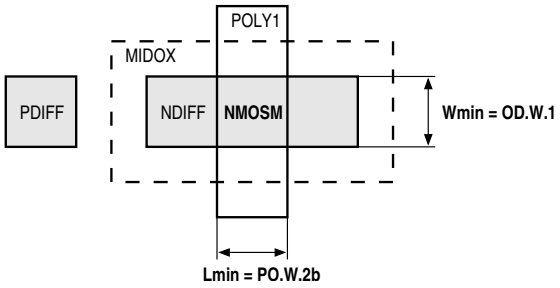


Rule	Description
RPOLY2P_R1	PPLUS on RPOLY2P is not allowed
RPOLY2P_R2	NPLUS on RPOLY2P is not allowed

Guideline	Description	Value
RPOLY2P_G1	Minimum number of RPOLY2P squares	5

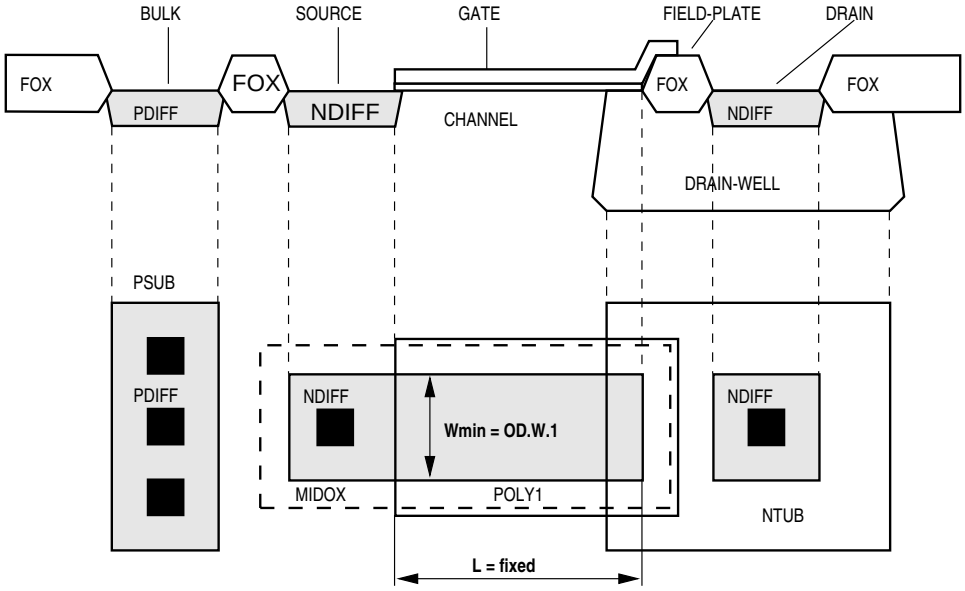
5.4 5-Volt Module

5.4.1 NMOSM



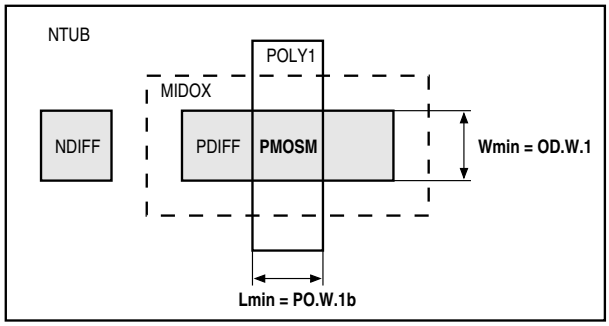
Guideline	Description	Value [um]
NMOSM_G1	Precision analog NMOSM should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.	
NMOSM_G2	Minimum channel length for critical analog NMOSM transistors Critical analog NMOSM transistors are: 1. Transistors biased at (Vth < VGS < VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	1

5.4.2 NMOSMH



Note: The layout of NMOSMH is predefined and available on request. Only W may be changed.

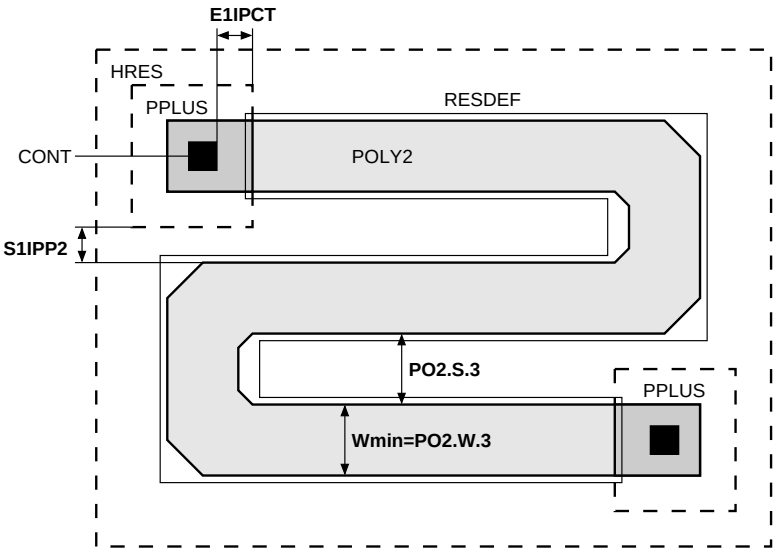
5.4.3 PMOSM



Guideline	Description	Value
PMOSM_G1	Precision analog PMOSM should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.	
PMOSM_G2	Minimum channel length for critical analog PMOSM transistors Critical analog PMOSM transistors are: 1. Transistors biased at (-Vth < -VGS < -VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	0.75

5.5 High Resistive Poly Module

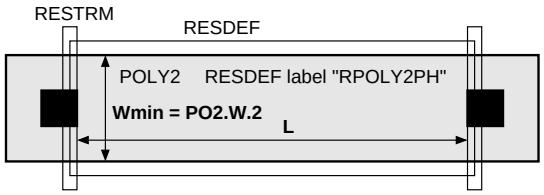
5.5.1 RPOLYH



Rule	Description	Value [um]
PO2.W.3	Minimum RPOLYH width	0.8
PO2.S.3	Minimum RPOLYH spacing	0.75
E1IPCT	Minimum PPLUS enclosure of POLY2CON	0.6
S1IPP2	Minimum PPLUS to RPOLYH spacing	0.35

Guideline	Description	Value [um]
RPOLYH_G1	Minimum number of RPOLYH squares	5
RPOLYH_G2	Minimum high precision RPOLYH width	2

5.5.2 RPOLY2PH

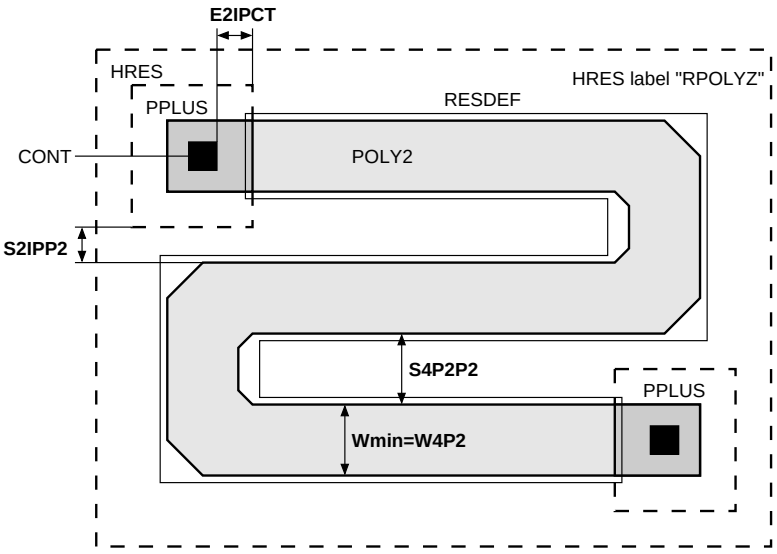


Rule	Description
RPOLY2PH_R1	PPLUS on RPOLY2PH is not allowed
RPOLY2PH_R2	NPLUS on RPOLY2PH is not allowed

Guideline	Description	Value
RPOLY2PH_G1	Minimum number of RPOLY2PH squares	5

5.6 Low TC Poly Module

5.6.1 RPOLYZ

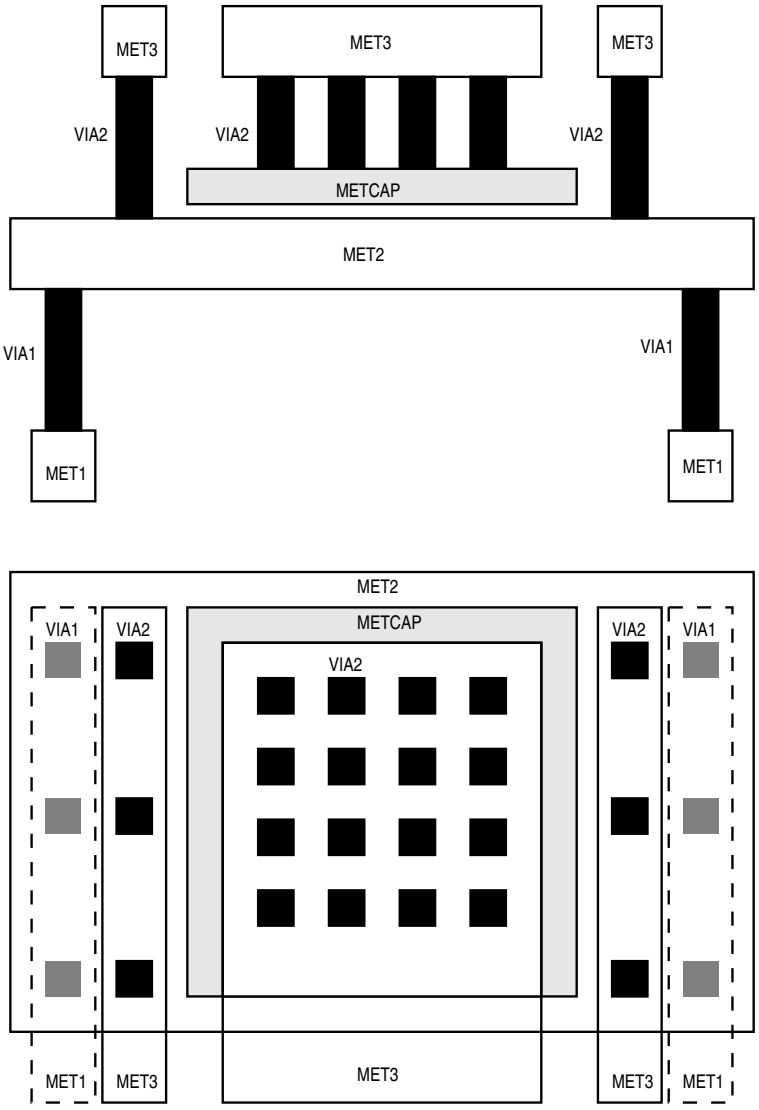


Rule	Description	Value [um]
W4P2	Minimum RPOLYZ width	0.8
S4P2P2	Minimum RPOLYZ spacing	0.75
E2IPCT	Minimum PPLUS enclosure of POLY2CON	0.6
S2IPP2	Minimum PPLUS to RPOLYZ spacing	0.35

Guideline	Description	Value [um]
RPOLYZ_G1	Minimum number of RPOLYZ squares	3.75
RPOLYZ_G2	Minimum high precision RPOLYZ width	2

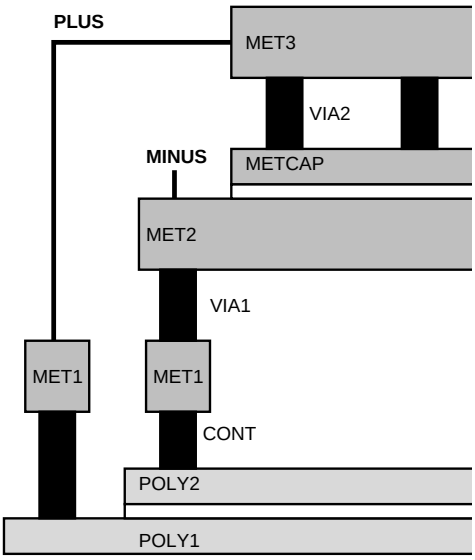
5.7 MIM Capacitor Module

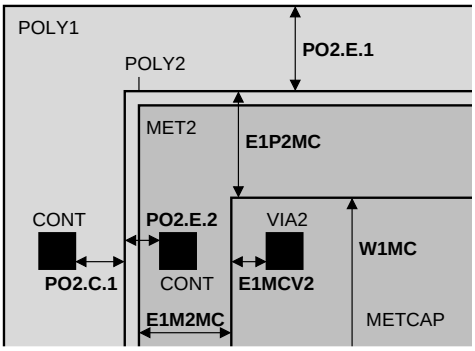
5.7.1 CMIM



Note: Active and passive circuit elements under METCAP are not recommended to avoid noise coupling or deviated MIM capacitance.
Put as many VIA2 as possible on METCAP to achieve a high Q factor.

5.7.2 CPMIM



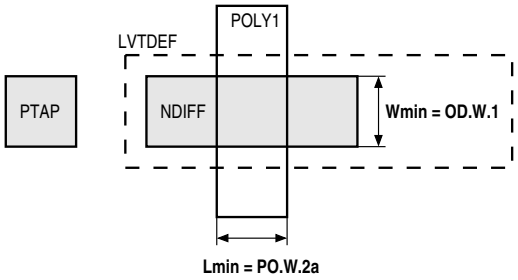


Note: Put as many VIA2 as possible on METCAP to achieve a high Q factor.

Rule	Description	Value [um]
E1P2MC	Fixed POLY2 enclosure of METCAP	1.15
CPMIM_R1	CPMIM overlapping MET1 is not allowed	
CPMIM_R2	METCAP and POLY1 plates must be connected	
CPMIM_R3	MET2 and POLY2 plates must be connected	

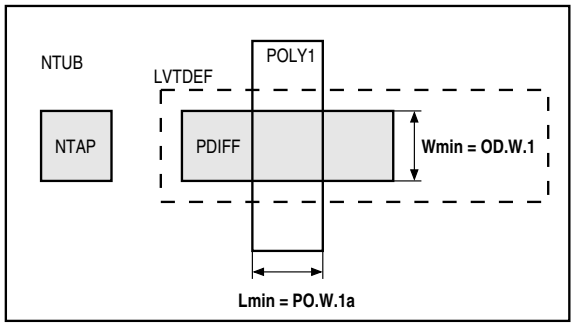
5.8 Low VT Module

5.8.1 NMOSL



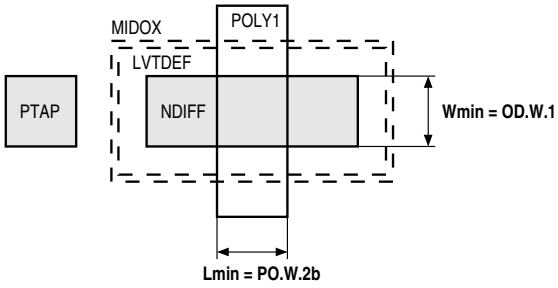
Guideline	Description	Value [um]
NMOSL_G1	Precision analog NMOSL should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.	
NMOSL_G2	Minimum channel length for critical analog NMOSL transistors Critical analog NMOSL transistors are: 1. Transistors biased at (Vth < VGS < VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	0.7

5.8.2 PMOSL



Guideline	Description
PMOSL_G1	Precision analog PMOSL should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.

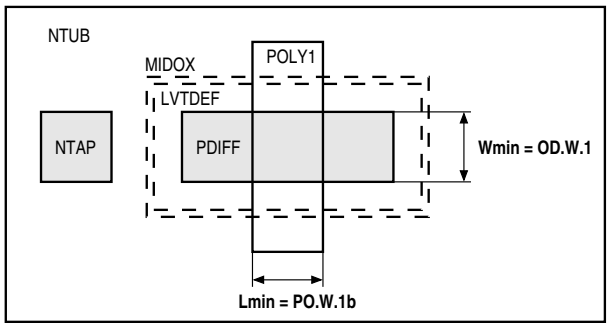
5.8.3 NMOSML



Rule	Description	Value [um]
NMOSML_R1	Minimum GATE length of NMOSML	0.5

Guideline	Description	Value [um]
NMOSML_G1	Precision analog NMOSML should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.	
NMOSML_G2	Minimum channel length for critical analog NMOSML transistors Critical analog NMOSML transistors are: 1. Transistors biased at (Vth < VGS < VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	1

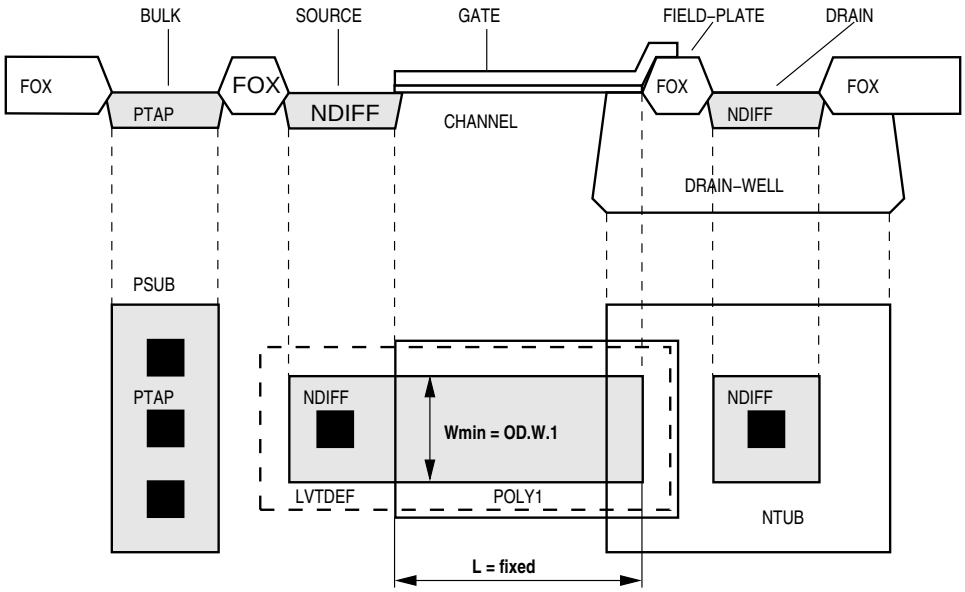
5.8.4 PMOSML



Rule	Description	Value [um]
PMOSML_R1	Minimum GATE length of PMOSML	0.5

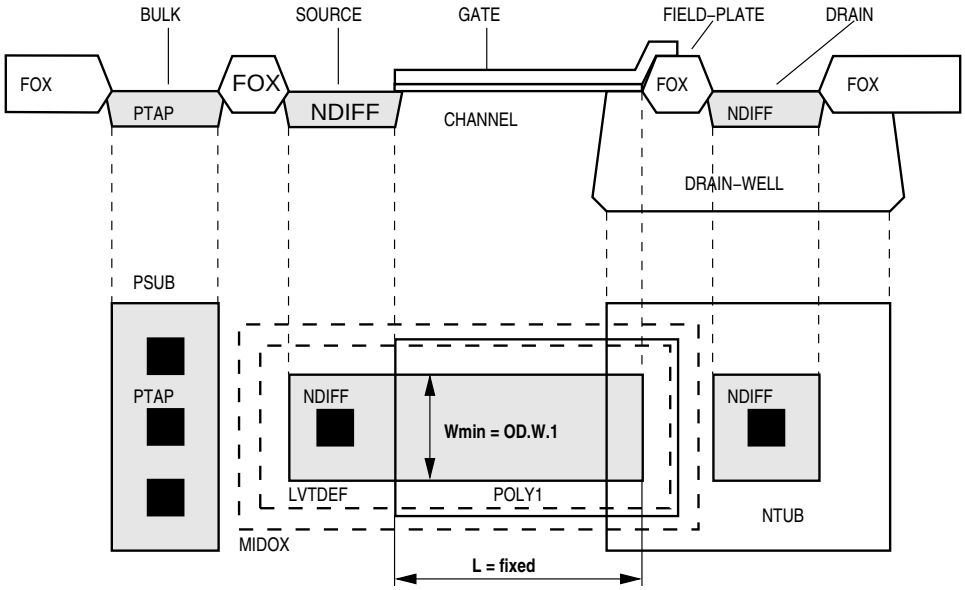
Guideline	Description
PMOSML_G1	Precision analog PMOSML should not be covered with METx. If this is not possible METx covering of matching transistors should be identical.

5.8.5 NMOSHL



Note: The layout of NMOSHL is predefined and available on request. Only W may be changed.

5.8.6 NMOSMHL



Note: The layout of NMOSMHL is predefined and available on request. Only W may be changed.

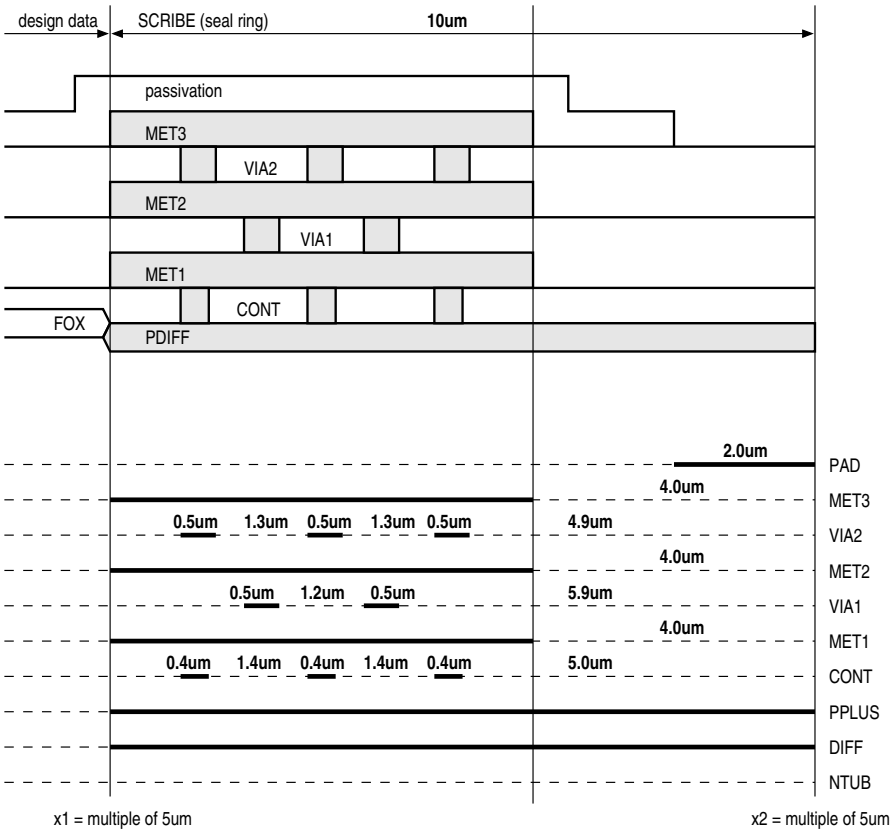
6 Scribe Border

A scribe border seals the chip against humidity and other external influences. This guard ring is connected to substrate.

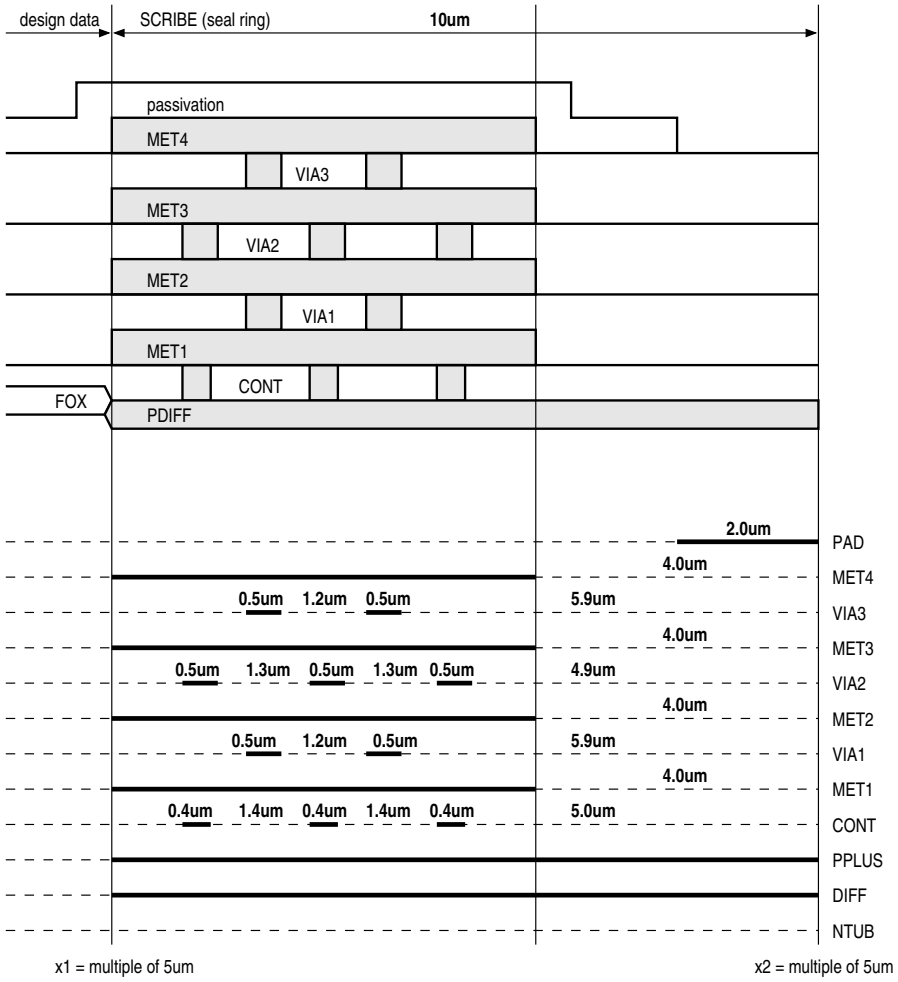
SCRIBE is a predefined layout and must completely enclose the design data. The inner edge of SCRIBE is butted to the data extrema of the design.

Only minimum sized vias according to the standard design rules are allowed.

6.1 Core Module



6.2 Metal 4 Module



6.3 Thick Metal Module

Identical to Metal 4 Module.

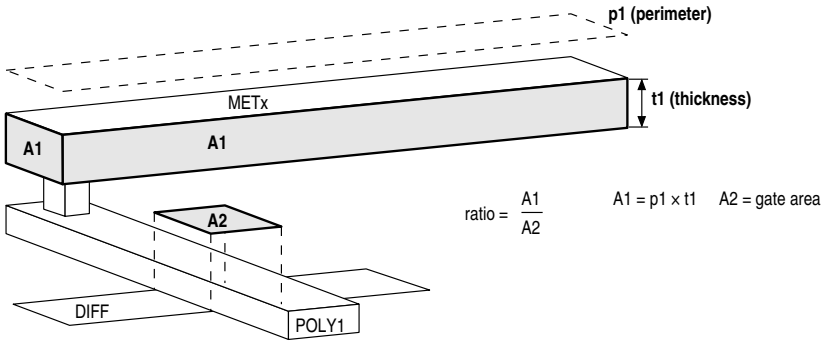
7 Ion Etch Antennas

7.1 Core Module

Structures collect electric charge during ion-etching which can be a hazard for associated GATE oxide.

Rule	Description	Value
A.R.1	Maximum ratio of floating POLY1 edge area to connected GATE area t1(POLY1)=0.282um	200
A.R.2	Maximum ratio of floating MET1 edge area to connected GATE area t1(MET1)=0.665um	400
A.R.3	Maximum ratio of floating MET2 edge area to connected GATE area t1(MET2)=0.64um	400
A.R.4	Maximum ratio of floating MET3 edge area to connected GATE area t1(MET3)=0.925um	400

Note: “floating” are shapes connected to active GATE area but not to DIFF.
Only layers which have been formed before etching have to be considered



7.2 Metal 4 Module

Rule	Description	Value
A.R.4	Maximum ratio of floating MET3 edge area to connected GATE area t1(MET3)=0.64um	400
A.R.5	Maximum ratio of floating MET4 edge area to connected GATE area t1(MET4)=0.925um	400

7.3 Thick Metal Module

Rule	Description	Value
A.R.4	Maximum ratio of floating MET3 edge area to connected GATE area t1(MET3)=0.64um	400
A.R.5	Maximum ratio of floating MET4 edge area to connected GATE area t1(MET4)=2.8um	400

8 Stress Release and CMP Rules

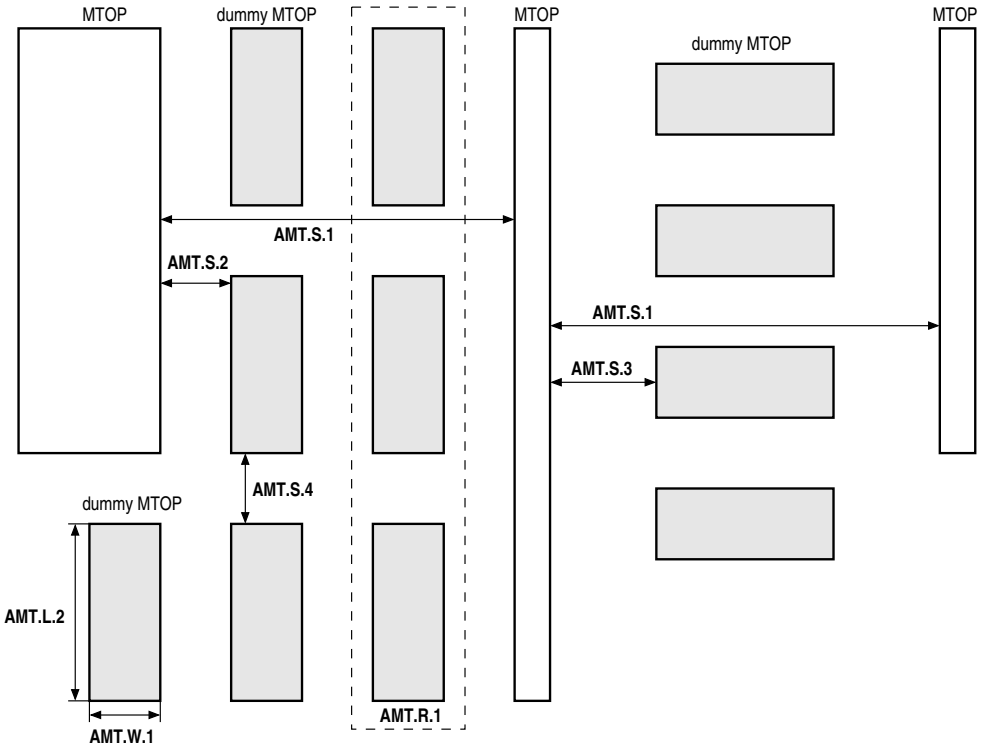
8.1 Top Metal Dummy Structures

Rule	Description	Value [um]
AMT.S.1	Maximum MTOP spacing when the width of one or both MTOP shapes is less than 10um.	10

To meet AMT.S.1 the following dummy structures must be added in the top metal layer as an assembly stress buffer:

Guideline	Description	Value [um]
AMT.W.1	Fixed width of dummy MTOP block	2
AMT.L.1	Fixed length of dummy MTOP block	5
AMT.S.2	Minimum MTOP feature to dummy MTOP block spacing	2
AMT.S.3	Maximum MTOP feature to dummy MTOP block spacing	6
AMT.S.4	Fixed dummy MTOP block spacing	2
AMT.R.1	Minimum number of dummy MTOP blocks in a region	3

Note: Automatic filling with dummy MTOP blocks can be suppressed with layer NOFILL.

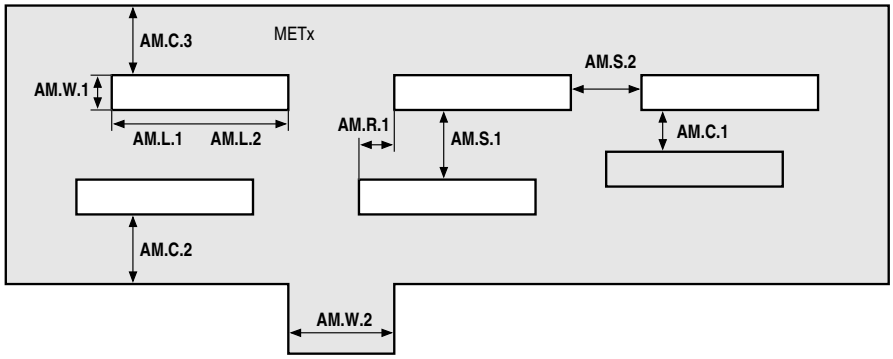


8.2 Metal Slots

Slots must be inserted to release stress in wide metal (> 35um):

Rule	Description	Value [um]
AM.W.0	Maximum METx width	35
AM.W.1	Fixed slot width	3
AM.L.1	Minimum slot length	30
AM.L.2	Maximum slot length	300
AM.S.1	Minimum spacing between two parallel slots	10
AM.S.2	Minimum spacing between two slots in a sequence	10

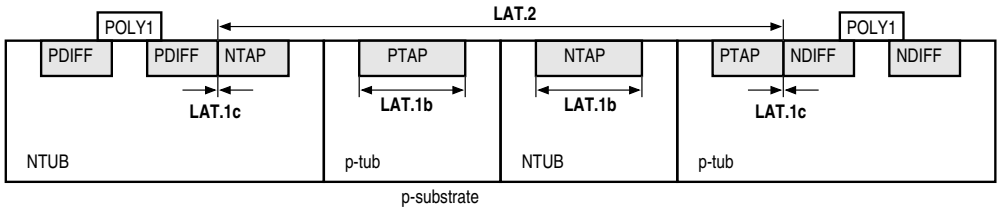
Guideline	Description	Value [um]
AM.C.1	Minimum slots spacing between neighbor layers (i.e.: MET1 / MET2, MET2 / MET3, MET3 / MET4)	2
AM.C.2	Minimum slot to inner metal edge spacing	10
AM.C.3	Minimum slot to outer metal edge spacing	10
AM.W.2	Minimum width of METx connected to wide METx with slots No slot is allowed opposite this metal	10
AM.R.1	Starting position of parallel slots should be staggered.	
AM.R.2	Slot must be parallel to the current direction.	

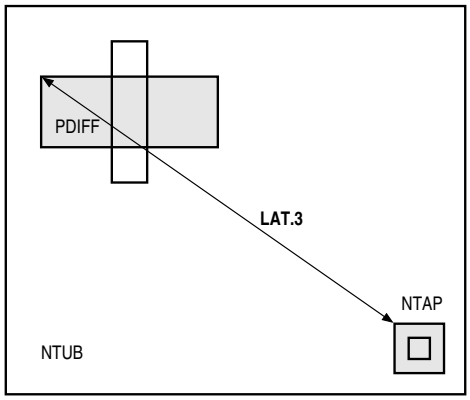


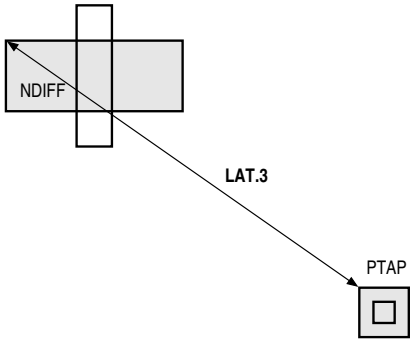
Note: The cell CORNER is available to insert slots in buses at die corners.

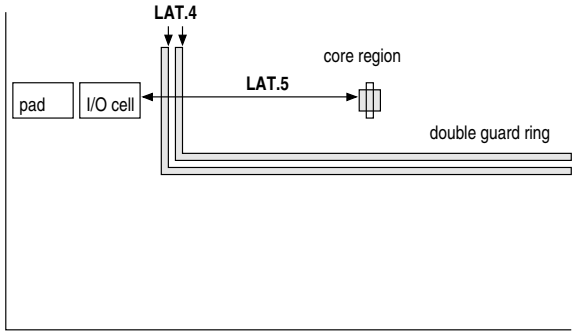
9 Latch-up Prevention

Guideline	Description	Value [um]
LAT.1a	A double guard ring structure should be inserted in between NMOS and PMOS of I / O buffers	
LAT.1b	Minimum PTAP and NTAP guard ring width for I / O buffers	3
LAT.1c	Maximum distance from PTAP or NTAP guard ring to source DIFF for I / O buffers	2
LAT.2	Minimum NMOS to PMOS spacing for I / O buffers and ESD devices Active DIFF area in this spacing is not allowed.	40
LAT.3	Maximum distance from any point inside source / drain DIFF to the nearest TAP DIFF of the same NTUB or PSUB.	20
LAT.4	A guard ring structure with NTUB pseudo-collector and PTAP should be inserted between I / O buffers and internal circuit area	
LAT.5	Minimum I / O buffer to internal circuit spacing	50
LAT.6	Any HOT_NDIFF area connecting to I / O pads should be surrounded by double guard ring.	
LAT.7	Any NTUB without direct connection to VDD and with HOT_NDIFF inside it should be surrounded by double guard ring.	
LAT.8	For special devices such as bipolar transistor, diode, resistor, or special circuits such as charge pump, power regulator, high noise or high power circuitry, a double guard ring should be inserted surrounding and between them.	
LAT.9	All the guard rings and pickups should be connected to VDD / VSS with very low series resistance. That is, NTUB should be tied together with NTAP, and DIFF should be tied together with contacts and metal to VDD / VSS. As many as possible CONT should be used.	


LAT.2
POLY1
POLY1
PDIFF
PDIFF
NTAP
PTAP
NTAP
PTAP
NDIFF
NDIFF
LAT.1c
LAT.1b
LAT.1b
LAT.1c
NTUB
p-tub
NTUB
p-tub
p-substrate


PDIFF
LAT.3
NTAP
NTUB

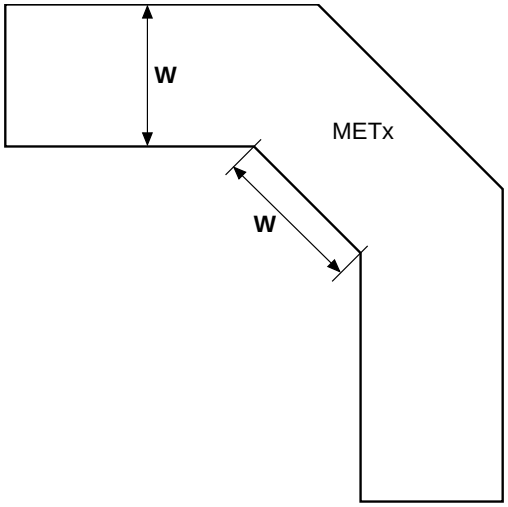

NDIFF
LAT.3
PTAP

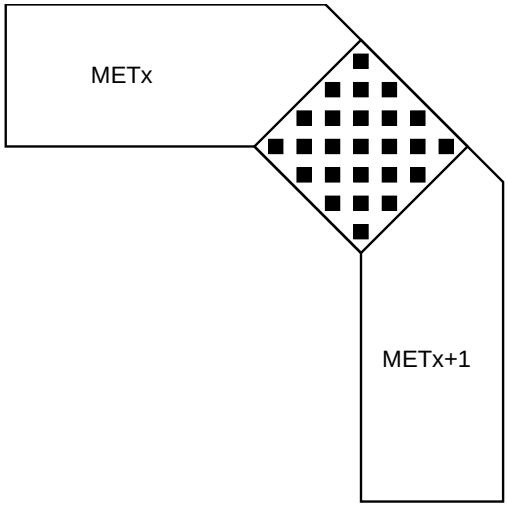

LAT.4
core region
LAT.5
pad
I/O cell
double guard ring

10 Electromigration Guidelines

For current densities refer to document 0.35 um 50V CMOS Process Parameters ENG-238

Guideline	Description
EMG001	Metal lines operated at I >= 90% Imax should have shamfered corners. Minimum length of inner chamfered edge = metal line width
EMG002	Via arrays connecting metal lines operated at I >= 90% Imax should be placed in a 45deg section.





11 Support

For questions on process parameters please refer to:

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