ENG - 182

0.35µm CMOS C35 Process Parameters

Revision #: 8.0

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Table of Contents

1 Introduction

1.1 Revision

Change Status of Pages (including short description of change)

Revision	Date	Changes	Affected pages
1.0	March 2002	first version of process parameter specification	1-63
2.0	February 2003	Changed: Parameters throughout the document due to parameter adjustments Chapter “Matching Parameter” taken out. All information about matching is included in the 0.35µm CMOS Matching Parameters document Eng – 228. SPICE Modeling: Added: Thick metal module, MIM capacitor module, Poly fuses. MOS transistor threshold voltage measured in linear region. MIM capacitor in Wafer Cross Section.	1-62
3.0	August 2004	Changed: Parameters throughout the document due to parameter adjustments Narrower specification for: RNWELL, RDIFFN, RDIFFP, RMET, RMET2, RMET3, CMIM (TMIM), RPOLY, RPOLYH Corrected:XJNW, Zener diode and poly fuse parameter withdrawn, TPROT1 for all metal modules, TMET and the corresponding metal capacitances. Accommodation of all influenced SPICE models. New SPICE models: RPOLY2, RDIFFN, RDIFFP, RPOLYH, CMIM, RNWELL. Added: JMETT, JPOLYH, TCMET, TCPOLY2W	1-62

Revision	Date	Changes	Affected pages
4.0	November 2005	TMP2FOXP1 (metal1-poly2 oxide thickness (field region, with poly1)), TP2FOX (poly2-well oxide thickness (field region)), TPOX, TMIM calculated from measured CPOX and CMIM Pass/Fail Parameters with reduced specification limits: RMETT Added: Schematic Description of Geometrical Parameters, Low VT Module Add processes C35A3B0, C35B3C3, C35B3L3, C35B4C0, C35B4M6 RPOLY1 resistor, junction current temperature exponent coefficient for all diodes (XTI) Changed: Diode leakage parameter for all diodes (JS, JSW), Temperature & voltage coefficients RPOLY2, RPOLYH	1-79
5.0	January 2007	Corrected: WPOLY1, VERT10 SPICE model temperature coefficient. Added: Poly Fuse and Zener diode electrical parameter specification, Descriptions of features and limitations of all SPICE models. Listing of worst case SPICE parameter Model feature overview table. Changed: VERT10, RPOLY1, RPOLY2 and RPOLYH SPICE model, SPICE models NMOSL, PMOSL, NMOSML, PMOSML	1-89
6.0	November 2008	Added: Low TC Poly Module, electrical Parameters and SPICE model, Note for thick metal module (Polyimide is mandatory for processes with thick top metal) Add process C35B4Z1, C35B4T1 Add high precision poly resistors: RPOLY2P and RPOLY2PH	1-95

Revision	Date	Changes	Affected pages
7.0	March 2013	Added: Schottky barrier diode Current Density AC operation guideline Changed: CMIM improved VC1 and VC2 behaviour Narrower specification for: RMET, RMET2, RMET3, RMET3T, RMET4, RMETT New: CMIM voltage ratio pass/fail parameter CPMIM GDS parameters for all MOS transistors Split into “0.35µm CMOS C35 Process Parameters” and ”0.35µm CMOS C35 SPICE Models” documents	1-68
8.0	November 2013	Added: Electromigration document ENG-487 in section 1.3 with note in section 2.3 Changed: IS12SBD5	p.8, p.13 p. 51

1.2 Process Family

This document is valid for the following 0.35um CMOS processes:

Process name	No. of masks	Core module	PIP capacitor module	5V gate module	High resistive poly module	Low TC poly module	Metal 4 module	Thick metal module	MIM capacitor module	Low VT module	Schottky diode module
C35A3B0	13	x									
C35B3C0	14	x	x								
C35B3C1	17	x	x	x							
C35B3C3	18	x	x	x	x						
C35B3L3	20	x	x	x	x					x	
C35B3S3	21	x	x	x	x					x	x
C35B3GH	28	x	x	x		x				x	x
C35B4C0	16	x	x				x				
C35B4C3	20	x	x	x	x		x				
C35B4T1	20	x	x	x				x			
C35B4M3	22	x	x	x	x			x**	x		
C35B4M6	18	x	x		x		x		x		
C35B4O1*	19	x	x	x			x				
C35B4Z1	20	x	x	x		x	x				

Core module: p-substrate, 1-poly, 3-metal, 3.3 Volt CMOS process.

PIP capacitor module: poly1-poly2 capacitor, RPOLY2 resistor, RPOLY2P resistor

5V gate module: 5V mid-oxide for MOSFETs

High resistive poly module: High resistive poly resistor RPOLYH, RPOLY2PH resistor

Low TC Poly Module Parameters: Low TC poly resistor RPOLYZ

Metal 4 module: Thin metal 4

Thick metal module: Thick metal 4

MIM capacitor module: MET2-METCAP capacitor

Low VT module: Low threshold 3.3V and 5V MOSFETs

*) C35B4O1: opto process with ARC layer.

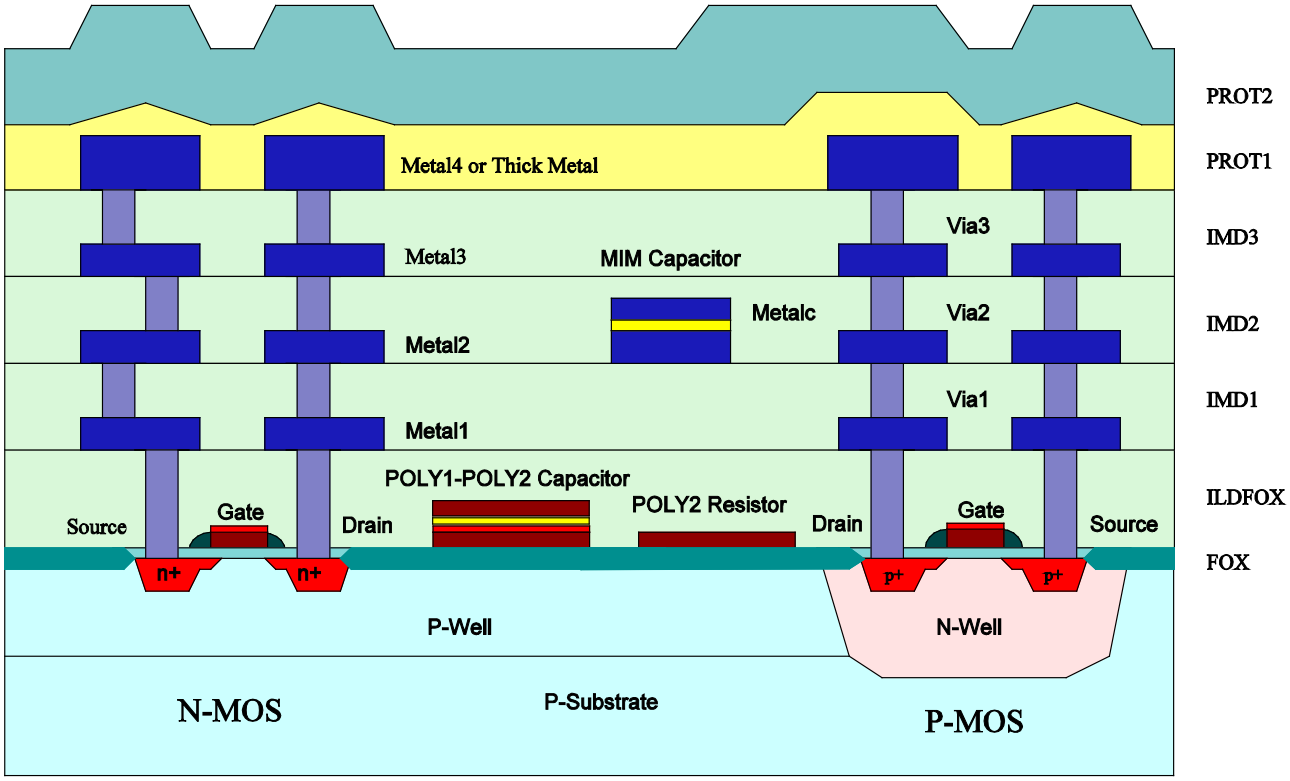
**) Polyimide is mandatory for processes with thick top metal

1.3 Related Documents

Description	Document Number
0.35µm CMOS C35 SPICE Models	ENG - 472
0.35µm CMOS C35 Design Rules	ENG - 183
0.35µm CMOS C35 Noise Parameters	ENG - 189
0.35µm CMOS C35 RF SPICE Models	ENG - 188
0.35µm CMOS Matching Parameters	ENG - 228
0.35µm CMOS C35O Process Parameters	ENG - 248
C35 ESD Design Rules	ENG - 236
Electromigration: Current Multiplication Factors	ENG - 487
Standard Family Cells	ENG - 42
Assembly Related Design Rules	ASSY - 15

2 General

2.1 Wafer Cross – Section



2.2 Operating Conditions

2.2.1 Temperature Range

The process described in this document is qualified for the temperature range -40°C <=Tj<=125°C.

Temperature dependent parameters are extracted in the temperature range 25°C< Tj <125°C.

SPICE models are valid for the temperature range -40°C< Tj <180°C.

(Tj specified as junction temperature)

2.2.2 Operating Voltage Range

The maximum operating voltages are specified in absolute values.

Note: The values in brackets denote absolute maximum ratings. These ratings are stress ratings only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown).

MOS Transistors	Device-name	max. VGS [V]	max. VDS [V]	max. VGB [V]	max. VDB [V]	max. VSB [V]	max. VBpsub [V]
3.3 Volt NMOS	NMOS	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	-
3.3 Volt PMOS	PMOS	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	5.5 (7)
5 Volt NMOS	NMOSM	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	-
5 Volt PMOS	PMOSM	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)
high voltage NMOS (gate oxide)	NMOSH	3.6 (5)	15 (17)	3.6 (5)	15 (17)	3.6 (5)	-
high voltage NMOS (mid-oxide)	NMOSMH	5.5 (7)	15 (17)	5.5 (7)	15 (17)	5.5 (7)	-

MOS Transistors	Device-name	max. VGS [V]	max. VDS [V]	max. VGB [V]	max. VDB [V]	max. VSB [V]	max. VBpsub [V]
Low VT 3.3 V NMOS	NMOSL	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	-
Low VT 3.3 V PMOS	PMOSL	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	5.5 (7)
Low VT 5 V NMOS	NMOSML	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	-

MOS Transistors	Device-name	max. VGS [V]	max. VDS [V]	max. VGB [V]	max. VDB [V]	max. VSB [V]	max. VBpsub [V]
Low VT 5 V PMOS	PMOSML	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)
Low VT 3.3 V high voltage NMOS (gate oxide)	NMOSHL	3.6 (5)	15 (17)	3.6 (5)	15 (17)	3.6 (5)	-
Low VT 5 V high voltage NMOS (mid-oxide)	NMOSMHL	5.5 (7)	15 (17)	5.5 (7)	15 (17)	5.5 (7)	-

Operating Voltage Range (continued)

PNP Bipolar Transistors	Device-name	max. VCE [V]	max. VEC [V]	max. VEB [V]	max. VBS [V]
vertical PNP (C = S)	VERT10	3.6 (5)	-	3.6 (5)	-
lateral PNP	LAT2	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)

Schottky Barrier Diode	Device- name	max. VAC reverse [V]	Max. VAC forward [V]	max. VCS [V]
Schottky barrier diode	SBD5	-5.5 (-7)	0.6(0.66)	-5.5(-7)

Capacitors	Device-name	max.Vterm-bulk [V]	max. Vterm1-term2 [V]
poly1-poly2	CPOLY	20 (30)*	5.5 (7)
MOS-Varactor	CVAR	3.6 (5)	3.6 (5)
metal2-metalC	CMIM	20 (30)*	5.5 (7)
poly2/metal2-metalC	CPMIM	20 (30)*	5.5 (7)

Resistors	Device-name	max. Vterm-bulk [V]
poly1	RPOLY1	20 (30)*
poly2	RPOLY2	20 (30)*
poly2	RPOLY2P RPOLY2PH	20 (30)*
high resistive poly2	RPOLYH	20 (30)*
low TC poly2	RPOLYZ	20 (30)*
p+ diffusion	RDIFFP, RDIFFP3	5.5 (7)
n+ diffusion	RDIFFN, RDIFFN3	5.5 (7)
Low voltage n-well	RNWELL	13 (15)

*) An inversion layer is formed in the bulk underneath the poly if the poly-to-bulk voltage exceeds the field threshold

voltage. The field threshold voltages are specified in section "3 Process Control Parameters".

Parasitics have the same maximum operating voltage as the primitive device they exist within. Please refer to section “2.3 Current Densities” as well.

2.3 Current Densities

Important application note:
The maximum allowed DC-current densities at 110°C are derived from reliability experiments. In addition, the effective AC-current densities (RMS-values) and the peak AC-current densities are specified in Note Q1.

Note: Additional electromigration information can be found in ENG - 487

Parameter	Symbol	Min	Typ	Max	Unit
POLY1 current density	JPOLY			0.5	mA/µm
POLY2 current density	JPOLY2			0.3	mA/µm
high resistive poly current density	JPOLYH			0.1	mA/µm
low TC POLY2 current density	JPOLYZ			0.2	mA/µm
MET1 current density	JMET			1.0	mA/µm
MET2 current density	JMET2			1.0	mA/µm
MET3 current density valid for triple metal process	JMET3T			1.6	mA/µm
MET3 current density valid for quadruple metal process	JMET3			1.0	mA/µm
MET4 current density	JMET4			1.6	mA/µm
METT thick metal current density	JMETT			5.0	mA/µm
CNT current density 0.4x0.4µm²	JCNT			0.94	mA/cnt
VIA current density 0.5x0.5µm²	JVIA			0.6	mA/via
VIA2 current density 0.5x0.5µm² valid for triple metal process	JVIA2T			0.9	mA/via
VIA2 current density 0.5x0.5µm² valid for quadruple metal process	JVIA2			0.6	mA/via
VIA3 current density 0.5x0.5µm²	JVIA3			0.96	mA/via
stack CNT/VIA current density 0.4x0.4µm² / 0.5x0.5µm²	JSTCNTVIA			0.6	mA/via
stack VIA1/2 current density 0.5x0.5µm²	JSTVIA12			0.4	mA/via
stack VIA2/3 current density 0.5x0.5µm²	JSTVIA23			0.64	mA/via
stack VIA1/2/3 current density 0.5x0.5µm²	JSTVIA123			0.64	mA/via

3 Process Control Parameters

3.1 Introduction

This section contains geometrical and electrical parameters, which are measured for process control purposes. All the other measurements are done at T_0 = 27°C.

Process parameters are assigned to one of the following categories:

1. **PASS/FAIL PARAMETERS**

   Pass/fail parameters are used for wafer selection during or after the wafer fabrication process, respectively. These parameters are extracted either from measurements within the fabrication process or from special process monitor test chips placed along the scribe line.

2. **INFORMATION PARAMETERS**

   Information parameters are provided in order to increase the knowledge about the process behaviour. These parameters do not lead to wafer reject in case of failure.

   CHARACTERIZATION PARAMETERS are a special group of information parameters. They are not under 100% statistical control because they require huge test structures (e.g. parasitic capacitors) or time consuming measurement procedures (e.g. temperature coefficients). These data are extracted from special process control monitor (PCM) test structures.

Note: A design shall rely on pass/fail parameters only.

The electrical parameters are regularly extracted from the scribe line monitor (SLM) test structures on every wafer. This so-called **MAP (Manufacturing Acceptance Parameters) data** can be obtained from the Foundry Engineering group of ams AG in order to estimate if the fab run is more or less close to the typical mean process condition.

Important Note: The process control transistor parameters must not be used for circuit simulation purposes. They are extracted from simplified model equations in order to increase the speed of the measurements. Special circuit-simulation transistor parameters are related to the document ”0.35µm CMOS C35 SPICE Models” (ENG – 472). Those are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. Therefore, process control transistor parameters may differ from their corresponding circuit simulation transistor parameters.

3.2 CMOS Core Module Parameters

3.2.1 Structural and Geometrical Parameters

Please refer to chapter ”3.13 Schematic Description” for a general overview of the backend of the 0.35um process.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
field oxide thickness	TFOX	260	290	320	nm	1
gate oxide thickness	TGOX	7.1	7.6	8.1	nm	2
poly1 thickness	TPOLY1	264	282	300	nm	1
metal1-poly oxide thickness (field region)	TILDFOX	395	645	895	nm	1
metal2-metal1 oxide thickness	TIMD1	620	1000	1380	nm	1
metal3-metal2 oxide thickness	TIMD2	620	1000	1380	nm	1
metal1 thickness	TMET1	565	665	765	nm	3
metal2 thickness	TMET2	540	640	740	nm	3
metal3 thickness (top metal)	TMET3T	775	925	1075	nm	3
passivation thickness 1	TPROT1	930	1030	1130	nm	1
passivation thickness 2	TPROT2	800	1000	1200	nm	1

Information parameters	Symbol	Min	Typ	Max	Unit	Note
metal1-poly oxide thickness (active region)	TILDDIFF	791	918	1045	nm	1
n+ junction depth	XJN		0.2		µm	4
p+ junction depth	XJP		0.2		µm	4
n-well junction depth	XJNW		3.5		µm	4
wafer substrate resistivity (non epi)	RSWAF	14	19	24	Ω cm	5
wafer thickness	TWAF	710		740	µm	5

3.2.2 MOS Electrical Parameters

3.2.2.1 MOS 3.3V N-Channel Electrical Parameters : NMOS

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10N	0.36	0.46	0.56	V	6
threshold voltage short channel 10x0.35	VTO10X035N	0.40	0.50	0.60	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_N3	0.49	0.59	0.69	V	6
threshold voltage poly on field 0.75µm	VTFPN	15	> 20		V	9
effective channel length 0.35µm	LEFF035N	0.30	0.38	0.46	µm	10
effective channel width 0.4µm	WEFF04N	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAN	0.48	0.58	0.68	$V^{½}$	12
gain factor	KPN	150	170	190	µA/V²	7
drain-source breakdown 0.35µm	BVDS035N	7	> 8		V	14
saturation current 0.35µm	IDS035N	450	540	630	µA/µm	15
substrate current 0.35µm	ISUB035N		1.5	3	µA/µm	16
subthreshold leakage current 0.35µm	SLEAK035N		0.5	2	pA/µm	17
gate oxide breakdown	BVGOXN	7	> 8		V	19
Output conductance 10/1.2	GDS10X12N	0.54	1.32	2.10	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.35µm	LACT035N		0.29		µm	27
threshold voltage narrow channel 0.4x10	VTO04X10N		0.46		V	6
threshold voltage small channel 0.4x0.35	VTO04X035N		0.48		V	6
threshold voltage temperature coefficient	TCVTON		-1.1		mV/K	13
effective substrate doping	NSUBN		212		$10^{15}/cm^3$	12

Information parameters	Symbol	Min	Typ	Max	Unit	Note
effective mobility	UON		370		cm²/Vs	8
mobility exponent	BEXN		-1.8		-	13

3.2.2.2 MOS 3.3V P-Channel Electrical Parameters : PMOS

Negative values are considered as absolute values for their Min/Max limits.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10P	-0.58	-0.68	-0.78	V	6
threshold voltage short channel 10x0.35	VTO10X035P	-0.55	-0.65	-0.75	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_P3	-0.62	-0.72	-0.82	V	6
threshold voltage poly on field 0.75µm	VTFPP	-15	< -20		V	9
effective channel length 0.35µm	LEFF035P	0.42	0.50	0.58	µm	10
effective channel width 0.4µm	WEFF04P	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAP	-0.32	-0.40	-0.48	$V^{½}$	12
gain factor	KPP	48	58	68	µA/V²	7
drain-source breakdown 0.35µm	BVDS035P	-7	< -8		V	14
saturation current 0.35µm	IDS035P	-180	-240	-300	µA/µm	15
subthreshold leakage current 0.35µm	SLEAK035P		-0.5	-2	pA/µm	17
gate oxide breakdown	BVGOXP	-7	< -8		V	19
Output conductance 10/1.2	GDS10X12P	0.32	0.87	1.41	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.35µm	LACT035P		0.31		µm	27
threshold voltage narrow channel 0.4x10	VTO04X10P		-0.90		V	6
threshold voltage small channel 0.4x0.35	VTO04X035P		-0.68		V	6

Information parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage temperature coefficient	TCVTOP		1.8		mV/K	13
effective substrate doping	NSUBP		101		$10^{15}/cm^3$	12
effective mobility	UOP		126		cm^2/Vs	8
mobility exponent	BEXP		-1.30		-	13

3.2.2.3 MOS N-Channel High Voltage Electrical Parameters : NMOSH

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage 3µm	VTO3NH	0.34	0.44	0.54	V	6
drain-source breakdown 3µm	BVDS3NH	15	19		V	14
on-resistance 3µm	RON3NH	9	13	17	kΩ µm	20

Information parameters	Symbol	Min	Typ	Max	Unit	Note
saturation current 3µm	IDS3NH	160	200	240	µA/µm	15
substrate current 3µm	ISUB3NH		1.5	3	µA/µm	16

3.2.3 Sheet Resistances

3.2.3.1 NWELL - Resistor: RNWELL

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
NWELL field sheet resistance	RNWELL	0.9	1.0	1.1	kΩ/□	21
NWELL field eff. width 1.7 µm	WNWELL	0.35	0.55	0.75	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
NWELL field temp. coefficient	TCNWELL		6.2		$10^{-3}/K$	23

3.2.3.2 RPOLY1 Sheet resistor: RPOLY1

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 sheet resistance	RPOLY	5	8	11	Ω/□	21
POLY1 effective width 0.35 µm	WPOLY	0.20	0.30	0.40	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 temperature coefficient	TCPOLY		0.9		10^{-3}/K	23
POLY1 gate sheet resistance (NMOS)	RGATEN		7		Ω/□	21
POLY1 gate sheet resistance (PMOS)	RGATEP		11		Ω/□	21
POLY1 gate effective width 0.35 µm (NMOS)	WGATEN		0.35		µm	21
POLY1 gate effective width 0.35 µm (PMOS)	WGATEP		0.35		µm	21

3.2.3.3 Diffusion Resistor: RDIFFN

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
NDIFF sheet resistance	RDIFFN	65	75	85	Ω/□	21
NDIFF effective width 0.3 µm	WDIFFN	0.25	0.40	0.55	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
NDIFF temperature coefficient	TCDIFFN		1.5		10^{-3}/K	23

3.2.3.4 Diffusion Resistor: RDIFFP

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
PDIFF sheet resistance	RDIFFP	115	140	165	Ω/□	21
PDIFF effective width 0.3 µm	WDIFFP	0.25	0.40	0.55	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
PDIFF temperature coefficient	TCDIFFP		1.5		10^{-3}/K	23

3.2.3.5 Metal Resistors

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET1 sheet resistance	RMET		70	100	mΩ/□	22

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET1 effective width 0.5 µm	WMET		0.5		µm	21
MET1 temperature coefficient	TCMET		3.3		10^{-3}/K	23

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET2 sheet resistance	RMET2		70	100	mΩ/□	22

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET2 effective width 0.6 µm	WMET2		0.5		µm	21
MET2 temperature coefficient	TCMET2		3.4		10^{-3}/K	23

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 sheet resistance (top metal)	RMET3T		40	80	mΩ/□	22

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 effective width 0.6 µm (top metal)	WMET3T		0.6		µm	21
MET3 temperature coefficient (top metal)	TCMET3T		3.5		10^{-3}/K	23

Please refer to section ”2.3 Current Densities” as well.

3.2.4 Contact Resistances

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET1-NDIFF cont. resistance 0.4x0.4µm²	RCNTMDN		30	100	Ω/cnt	24
MET1-PDIFF cont. resistance 0.4x0.4µm²	RCNTMDP		60	150	Ω/cnt	24
MET1-POLY1 cont. resistance 0.4x0.4µm²	RCNTMP		2	10	Ω/cnt	24
VIA resistance 0.5x0.5µm²	RVIA		1.2	3	Ω/via	24
VIA2 resistance 0.5x0.5µm²	RVIA2		1.2	3	Ω/via	24

Please refer to section ”2.3 Current Densities” as well.

3.2.5 Capacitances

Capacitance values except CGOX are characterization parameters (refer to section "3.1Introduction").

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 - DIFF (gate oxide)						
POLY1 - DIFF area	CGOX	4.26	4.54	4.86	fF/µm²	2

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 - DIFF (gate oxide)						
GATE – NDIFF overlap	CGSDON	0.105	0.120	0.134	fF/µm	27
GATE - PDIFF overlap	CGSDOP	0.075	0.086	0.096	fF/µm	27
GATE - BULK overlap	CGBO	0.10	0.11	0.12	fF/µm	28
POLY1 – LDD (gate oxide)						
GATE – LDD overlap	CGSDLN	0.115	0.131	0.147	fF/µm	27
GATE – LDD overlap	CGSDLP	0.095	0.108	0.121	fF/µm	27
POLY1 – WELL (field oxide)						
POLY1 – WELL (field oxide) area	CPFOX	0.108	0.119	0.133	fF/µm²	25
POLY1 – WELL (field oxide) perimeter	CPFOXF	0.051	0.053	0.055	fF/µm	26

Capacitances (continued)

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET1 – WELL (field region)						
MET1 - WELL (active region) area	CMDIFF	0.026	0.030	0.034	fF/µm²	25
MET1 - WELL (active region) perimeter	CMDIFFF	0.042	0.044	0.047	fF/µm	26
MET1 – WELL (field region)						
MET1 – WELL (field region) area	CMFOX	0.023	0.029	0.038	fF/µm²	25
MET1 – WELL (field region) perimeter	CMFOXF	0.040	0.044	0.049	fF/µm	26
MET1 - POLY1 (active region), MET1 - POLY2 (active region, without POLY1)						
MET1 - POLY1 (active region) area	CMPDIFF	0.034	0.039	0.045	fF/µm²	25
MET1 - POLY1 (active region) perimeter	CMPDIFFF	0.045	0.048	0.052	fF/µm	26
MET1 - POLY1 (field region), MET1 - POLY2 (field region, without POLY1)						
MET1 - POLY1 (field region) area	CMPFOX	0.040	0.055	0.090	fF/µm²	25
MET1 - POLY1 (field region) perimeter	CMPFOXF	0.047	0.053	0.063	fF/µm	26
MET2 – WELL						
MET2 – WELL area	CM2FOX	0.010	0.012	0.017	fF/µm²	25
MET2 – WELL perimeter	CM2FOXF	0.032	0.035	0.039	fF/µm	26
MET2 - POLY1, MET2 – POLY2 (without POLY1)						
MET2 - POLY1 area	CM2P	0.012	0.016	0.023	fF/µm²	25
MET2 - POLY1 perimeter	CM2PF	0.034	0.037	0.042	fF/µm	26
MET2 - MET1						
MET2 - MET1 area	CM2M	0.026	0.036	0.059	fF/µm²	25
MET2 - MET1 perimeter	CM2MF	0.042	0.048	0.056	fF/µm	26
MET3T – WELL						
MET3T – WELL area	CM3TFOX	0.006	0.008	0.011	fF/µm²	25
MET3T – WELL perimeter	CM3TFOXF	0.029	0.032	0.036	fF/µm	26
MET3T – POLY1, MET3 – POLY2 (without POLY1)						
MET3T – POLY1 area	CM3TP	0.007	0.009	0.013	fF/µm²	25
MET3T – POLY1 perimeter	CM3TPF	0.030	0.034	0.038	fF/µm	26

Capacitances (continued)

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET3T - MET1						
MET3T - MET1 area	CM3TM	0.010	0.014	0.020	fF/µm²	25
MET3T - MET1 perimeter	CM3TMF	0.034	0.039	0.044	fF/µm	26
MET3T - MET2						
MET3T - MET2 area	CM3TM2	0.026	0.036	0.059	fF/µm²	25
MET3T - MET2 perimeter	CM3TM2F	0.046	0.053	0.062	fF/µm	26
COUPLING CAPACITANCES						
POLY1 - POLY1 coupling	CP1P1		0.039		fF/µm	29
MET1 - MET1 coupling	CM1M1		0.087		fF/µm	29
MET2 - MET2 coupling	CM2M2		0.084		fF/µm	29
MET3T - MET3T coupling (top metal)	CM3TM3T		0.096		fF/µm	29

3.2.5.1 MOS Varactor: CVAR

Information parameters	Symbol	Min	Typ	Max	Unit	Note
Capacitance at –1.0V	CVARM	1.06	1.33	1.59	fF/µm²	44
Capacitance at 0.0V	CVAR0	2.40	3.00	3.61	fF/µm²	44
Capacitance at +1.0V	CVARP	3.90	4.88	5.86	fF/µm²	44
quality factor W/L=317/0.65, 2.4 GHz	QMIN		43		-	41
tuning range	gamma		57		%	42

3.2.6 Diode Parameters

Diode parameters except breakdown voltage parameters are characterisation parameters (refer to section "Introduction").

NDIFF-PWELL

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
breakdown voltage	BVN	7	9		V	31

Information parameters	Symbol	Min	Typ	Max	Unit	Note
area junction capacitance	CJN		0.84		fF/µm²	30
area grading coefficient	MJN		0.34		-	30
junction potential	PBN		0.69		V	30
sidewall junction capacitance	CJSWN		0.25		fF/µm	30
sidewall grading coefficient	MJSWN		0.23		-	30
area leakage current	JSN		0.51		aA/µm²	32
junction current temperature exponent coefficient	XTIND_NL		2.03		-	32
sidewall leakage current	JSSWN		0.61		aA/µm	32

PDIFF-NWELL

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
breakdown voltage	BVP	-7	-9		V	31

Information parameters	Symbol	Min	Typ	Max	Unit	Note
area junction capacitance	CJP		1.36		fF/µm²	30
area grading coefficient	MJP		0.54		-	30
junction potential	PBP		1.02		V	30
sidewall junction capacitance	CJSWP		0.35		fF/µm	30
sidewall grading coefficient	MJSWP		0.46		-	30
area leakage current	JSP		0.28		aA/µm²	32
junction current temperature exponent coefficient	XTIND_PL		1.97		-	32
sidewall leakage current	JSSWP		0.37		aA/µm	32

Diode Parameters (continued)

NWELL-PWELL/PSUB

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
breakdown voltage	BVNW	25	34		V	31

Information parameters	Symbol	Min	Typ	Max	Unit	Note
area junction capacitance	CJNW		0.08		fF/µm²	30
area grading coefficient	MJNW		0.39		-	30
junction potential	PBNW		0.53		V	30
sidewall junction capacitance	CJSWNW		0.51		fF/µm	30
sidewall grading coefficient	MJSWNW		0.27		-	30
area leakage current	JSNW		2.8		aA/µm²	32
junction current temperature exponent coefficient	XTIND_NWL		1.47		-	32
sidewall leakage current	JSSWNW		7.6		aA/µm	32

3.2.7 Bipolar Parameters

3.2.7.1 Lateral PNP Bipolar Transistor: LAT2

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
lateral PNP base-emitter voltage 2x2µm²@1µA	VBEL	600	650	700	mV	34
lateral PNP current gain 2x2µm²@1µA	BETAL1	30	140	380	-	34

Information parameters	Symbol	Min	Typ	Max	Unit	Note
lateral PNP current gain 2x2µm²@10µA	BETAL10		30		-	34
lateral PNP Early voltage 2x2µm²	VAFL	8	15		V	35
lateral PNP - parasitic vertical current gain 2x2µm²	BETAVL		14		-	34

3.2.7.2 Vertical PNP Bipolar Transistor: VERT10

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
vertical PNP base-emitter voltage 10x10µm²	VBEV	650	680	710	mV	33
vertical PNP current gain 10x10µm²@10µA	BETAV	2.0	5.0	8.0	-	33

Information parameters	Symbol	Min	Typ	Max	Unit	Note
vertical PNP Early voltage 10x10µm²	VAFV		>80		V	35
vertical PNP half gain current 10x10µm²	ICHBV		120		µA	33

3.2.8 OTP Electrical Parameter

The aim of the Poly Fuse and Zener diode electrical parameters is to provide information about the poly1 resistor fuse, the burn transistor parameters and the Zener diode parameter only. The poly fuse is intended to be used in qualified cells only. It is not allowed to use it in any other application.

3.2.8.1 Poly Fuses Parameters

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
poly1 resistance fuse (1.8x0.35µm)	RPFUSE0	25	45	65	Ω	45
poly1 resistance fuse after burn (1.8x0.35µm)	RPFUSE1	0.1	20		MΩ	46
Idsat of burn transistor (150x0.35µm)	IDSMOS_PF	47	67	87	mA	47

Information parameters	Symbol	Min	Typ	Max	Unit	Note
Vt of burn transistor (150x0.35)	VTMOS_PF	0.38	0.48	0.58	V	6

3.2.8.2 Zener Diode Parameters: ZD2SM24

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
Zener breakdown voltage 2µA	VZENER2	0.7	1.6	2.5	V	48

Information parameters	Symbol	Min	Typ	Max	Unit	Note
Zener breakdown voltage 50µA	VZENER50	2.0	3.0	4.0	V	48
Zener diode leakage current	LZENER		0.2		µA	49
zapped Zener diode voltage	VZAP			100	mV	50
Zener breakdown voltage 50µA temperature coefficient	TCVZENER50		-2.4		mV/K	51

3.3 Poly1-Poly2 Capacitor Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

3.3.1 Structural and Geometrical Parameters

Please refer to chapter "3.13 Schematic Description" for a general overview of the backend of the 0.35um process.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
CPOLY equivalent oxide thickness	TPOX	36.88	41.16	45.39	nm	2
poly2 thickness	TPOLY2	185	200	215	nm	1

Information parameters	Symbol	Min	Typ	Max	Unit	Note
m1-p2 oxide thickness	TP2FOX	480	727	974	nm	1
metal1-poly2 oxide thickness (field region, with poly1)	TMP2FOXP1	135	404	673	nm	1

3.3.2 Poly2 Sheet Resistance: RPOLY2

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 sheet resistance	RPOLY2	40	50	60	Ω/□	21
POLY2 effective width 0.65 µm	WPOLY2	0.30	0.40	0.50	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 sheet resistance temp. coefficient linear term W > 4 µm	TC1POLY2		0.59		10^{-3}/K	23
POLY2 sheet resistance temp. coefficient quadratic term	TC2POLY2		7.7		$10^{-7}/K^2$	23

3.3.3 Contact Resistance

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET1-POLY2 cont. resistance 0.4x0.4µm²	RCNTMP2		20	40	Ω/cnt	24

3.3.4 High Precision Poly2 Sheet Resistance: RPOLY2P

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 sheet resistance	RPOLY2P	42	47	52	Ω/□	21
POLY2 effective width 0.65 µm	WPOLY2P	0.30	0.40	0.50	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 sheet resistance temp. coefficient linear term W > 4 µm	TC1POLY2P		0.59		10^{-3}/K	23
POLY2 sheet resistance temp. coefficient quadratic term	TC2POLY2P		7.7		$10^{-7}/K^2$	23

The values specified for RPOLY2P are only valid for the poly1-poly2 module.

3.3.5 POLY1-POLY2 Capacitor: CPOLY

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
CPOLY area capacitance	CPOX	0.78	0.86	0.96	fF/µm²	2
CPOLY breakdown voltage high voltage on POLY2	BVPOX	15	30		V	36
CPOLY breakdown voltage high voltage on POLY1	BVPOXH	15	30		V	36

Information parameters	Symbol	Min	Typ	Max	Unit	Note
CPOLY perimeter capacitance	CPOXF	0.083	0.086	0.089	fF/µm	26
CPOLY linearity	VCPOX		85		ppm/V	37
CPOLY leakage current	LKCPOX			1	aA/µm²	**39**
CPOLY temperature coefficient	TCPOX		0.03		10^{-3}/K	38

The values specified above are only valid for the poly1-poly2 module.

3.3.6 Capacitances

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 - WELL (field region)						
POLY2 - WELL (field region) area	CP2FOX	0.095	0.105	0.117	fF/µm²	25
POLY2 - WELL (field region) perimeter	CP2FOXF	0.049	0.050	0.052	fF/µm	26
MET1 - POLY2 (field region, with POLY1)						
MET1 - POLY2 area	CMP2FOXP1	0.053	0.088	0.262	fF/µm²	25
MET1 - POLY2 perimeter	CMP2FOXP1F	0.050	0.060	0.082	fF/µm	26
MET2 - POLY2 (field region, with POLY1)						
MET2 - POLY2 area	CM2P2FOXP1	0.013	0.017	0.027	fF/µm²	25
MET2 - POLY2 perimeter	CM2P2FOXP1F	0.036	0.040	0.045	fF/µm	26
MET3T – POLY2 (field region, with POLY1)						
MET3T(top metal) – POLY2 area	CM3TP2FOXP1	0.007	0.010	0.014	fF/µm²	25
MET3T(top metal) – POLY2 perimeter	CM3TP2FOXP1F	0.031	0.035	0.036	fF/µm	26
COUPLING CAPACITANCES						
POLY2 - POLY2 coupling	CP2P2		0.016		fF/µm	29

3.4 Metal2-MetalC Capacitor Module Parameters

Please refer to "1.2 Process Family " for information on the processes where this module is implemented.

3.4.1 Structural and Geometrical Parameters

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
CMIM equivalent oxide thickness	TMIM	23.80	27.61	32.87	nm	2

Information parameters	Symbol	Min	Typ	Max	Unit	Note
METC thickness	TMETC		150		nm	3

3.4.2 METC Sheet Resistance

Information parameters	Symbol	Min	Typ	Max	Unit	Note
METC sheet resistance	RMETC		8.0		Ω/□	22
METC effective width 4µm	WMETC		4.0		µm	21

3.4.3 Contact Resistance

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET3-METC via resistance 0.5x0.5µm²	RVIA2C		1.75	6	Ω/via	24

3.4.4 Metal2-MetalC Capacitor: CMIM

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
CMIM area capacitance	CMIM	1.05	1.25	1.45	fF/µm²	2
CMIM breakdown voltage high voltage on MET2	BVM2	10	40		V	19
CMIM breakdown voltage high voltage on METC	BVMC	10	40		V	19

Information parameters	Symbol	Min	Typ	Max	Unit	Note
CMIM perimeter capacitance	CMIMF		0.17		fF/µm	26
CMIM linearity, 1st order	VC1MIM		-6.6	-15	ppm/V	37
CMIM linearity, 2nd order	VC2MIM		3.6	6	ppm/V²	37

Information parameters	Symbol	Min	Typ	Max	Unit	Note
CMIM temperature coefficient	TCMIM		22.3		ppm/K	38
CMIM leakage current	LKCMIM		10		aA/µm²	39
CMIM voltage ratio of C(+-5V) / C(0V)	CMIM_C5C0		125	250	ppm	40

3.4.1 Poly-MIM stack capacitor: CPMIM

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
CPMIM area capacitance	CPMIM	1.95	2.2	2.45	fF/µm²	2
CPMIM breakdown voltage high voltage on MET2	BVPM2	10	40		V	19
CPMIM breakdown voltage high voltage on METC	BVPMC	10	40		V	19

Information parameters	Symbol	Min	Typ	Max	Unit	Note
CPMIM perimeter capacitance	CPMIMF		1.4		fF/µm	26
CPMIM linearity, 1st order	VC1PMIM		31		ppm/V	37
CPMIM linearity, 2nd order	VC2PMIM		2		ppm/V²	37
CPMIM leakage current	LKCPMIM		10		aA/µm²	39
CPMIM temperature coefficient	TCPMIM		23.6		ppm/K	38

3.5 5 Volt Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

The transistors NMOSM, PMOSM and NMOSMH use mid-oxide as gate insulator.

3.5.1 Structural and Geometrical Parameters

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
Mid-oxide thickness	TMOX	14	15	16	nm	2

3.5.2 MOS Electrical Parameters

3.5.2.1 MOS 5V N-Channel Electrical Parameters : NMOSM

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10NM	0.60	0.70	0.80	V	6
threshold voltage short channel 10x0.5	VTO10X05NM	0.60	0.70	0.80	V	6
threshold voltage short channel 10x0.5 (measured in linear region)	VT_5N3	0.69	0.79	0.89	V	6
effective channel length 0.5µm	LEFF05NM	0.35	0.45	0.55	µm	10
effective channel width 0.4µm	WEFF04NM	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMANM	0.90	1.05	1.20	$V^{½}$	12
gain factor	KPNM	80	100	120	µA/V²	7
drain-source breakdown 0.5µm	BVDS05NM	7	> 9		V	14
saturation current 0.5µm	IDS05NM	400	470	540	µA/µm	15
substrate current 0.5µm	ISUB05NM		2	5	µA/µm	16
subthreshold leakage current 0.5µm	SLEAK05NM		0.1	1	pA/µm	17
gate oxide breakdown	BVGOXNM	12	> 15		V	19
Output conductance 10/1.2	GDS10X12NM	0.005	0.64	1.27	µA/V	18

MOS 5V N-Channel Electrical Parameters: NMOSM (continued)

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.5µm	LACT05NM		0.30		µm	27
threshold voltage narrow channel 0.4x10	VTO04X10NM		0.63		V	6
threshold voltage small channel 0.4x0.5	VTO04X05NM		0.63		V	6
threshold voltage temperature coefficient	TCVTONM		-1.5		mV/K	13
effective substrate doping	NSUBNM		173		$10^{15}/cm^3$	12
effective mobility	UONM		435		cm^2/Vs	8
mobility exponent	BEXNM		-1.76		-	13

3.5.2.2 MOS 5V P-Channel Electrical Parameters: PMOSM

Negative values are considered as absolute values for their Min/Max limits.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10PM	-0.85	-0.97	-1.09	V	6
threshold voltage short channel 10x0.5	VTO10X05PM	-0.85	-0.97	-1.09	V	6
threshold voltage short channel 10x0.5 (measured in linear region)	VT_5P3	-0.88	-1.03	-1.18	V	6
effective channel length 0.5µm	LEFF05PM	0.58	0.68	0.78	µm	10
effective channel width 0.4µm	WEFF04PM	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAPM	-0.53	-0.63	-0.73	$V^{½}$	12
gain factor	KPPM	25	31	37	$µA/V^2$	7
drain-source breakdown 0.5µm	BVDS05PM	-7	< -8		V	14
saturation current 0.5µm	IDS05PM	-150	-200	-250	µA/µm	15
subthreshold leakage current 0.5µm	SLEAK05PM		-0.01	-0.1	pA/µm	17
gate oxide breakdown	BVGOXPM	-12	< -15		V	19

MOS 5V P-Channel Electrical Parameters: PMOSM (continued)

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
Output conductance 10/1.2	GDS10X12PM	0.04	0.36	0.69	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.5µm	LACT05PM		0.45		µm	27
threshold voltage narrow channel 0.4x10	VTO04X10PM		-1.25		V	6
threshold voltage small channel 0.4x0.5	VTO04X05PM		-0.90		V	6
threshold voltage temperature coefficient	TCVTOPM		2.0		mV/K	13
effective substrate doping	NSUBPM		63		$10^{15}/cm^3$	12
effective mobility	UOPM		135		cm^2/Vs	8
mobility exponent	BEXPM		-1.3		-	13

3.5.2.3 MOS N-Channel High Voltage Electrical Parameters : NMOSMH

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage 3µm	VTO3NMH	0.55	0.67	0.79	V	6
drain-source breakdown 3µm	BVDS3NMH	17	22		V	14
on-resistance 3µm	RON3NMH	7	11	15	kΩ µm	20

Information parameters	Symbol	Min	Typ	Max	Unit	Note
saturation current 3µm	IDS3NMH	180	220	260	µA/µm	15
substrate current 3µm	ISUB3NMH		1	5	µA/µm	16

3.5.3 Capacitances

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 - DIFF (mid-oxide) area	CMOX	2.16	2.30	2.46	$fF/µm^2$	2

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 - DIFF (mid-oxide)						
GATE – NDIFF overlap	CGSDOMN	0.095	0.108	0.121	fF/µm	27
GATE - PDIFF overlap	CGSDOMP	0.080	0.091	0.102	fF/µm	27
GATE - BULK overlap	CGBOM	0.10	0.11	0.12	fF/µm	28
POLY1 – LDD (mid oxide)						
GATE – LDD overlap	CGSDLMN	0.200	0.227	0.254	fF/µm	27
GATE – LDD overlap	CGSDLMP	0.052	0.060	0.068	fF/µm	27

3.6 Low VTH Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

3.6.1 Low VT MOS 3.3V N-Channel Electrical Parameters : NMOSL

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10NL	0.33	0.41	0.49	V	6
threshold voltage short channel 10x0.35	VTO10X035NL	0.32	0.40	0.48	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_N3L	0.37	0.45	0.53	V	6
threshold voltage poly on field 0.75µm	VTFPNL	15	> 20		V	
effective channel length 0.35µm	LEFF035NL	0.30	0.38	0.46	µm	10
effective channel width 0.4µm	WEFF04NL	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMANL	0.42	0.52	0.62	$V^{½}$	12
gain factor	KPNL	156	176	196	µA/V²	7
drain-source breakdown 0.35µm	BVDS035NL	7	> 8		V	14
saturation current 0.35µm	IDS035NL	480	580	680	µA/µm	15
substrate current 0.35µm	ISUB035NL		1.2	3	µA/µm	16
subthreshold leakage current 0.35µm	SLEAK035NL		4	160	pA/µm	17
gate oxide breakdown	BVGOXNL	7	> 8		V	19
Output conductance 10/1.2	GDS10X12NL	0.66	1.43	2.2	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.35µm	LACT035NL		0.27		µm	27
subthreshold leakage current 0.35µm @ 125 C	SLNL125		1.7	10.0	nA/µm	17
threshold voltage narrow channel 0.4x10	VTO04X10NL		0.42		V	6

Information parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage small channel 0.4x0.35	VTO04X035NL		0.42		V	6
threshold voltage temperature coefficient	TCVTONL		-1.0		mV/K	13
effective substrate doping	NSUBNL		166		$10^{15}/cm^3$	12
effective mobility	UONL		387		cm^2/Vs	8
mobility exponent	BEXNL		-1.7		-	13

3.6.2 Low VT MOS 3.3V P-Channel Electrical Parameters : PMOSL

Negative values are considered as absolute values for their Min/Max limits.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10PL	-0.37	-0.45	-0.53	V	6
threshold voltage short channel 10x0.35	VTO10X035PL	-0.37	-0.45	-0.53	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_P3L	-0.50	-0.58	-0.66	V	6
threshold voltage poly on field 0.75µm	VTFPPL	-15	< -20		V	
effective channel length 0.35µm	LEFF035PL	0.42	0.50	0.58	µm	10
effective channel width 0.4µm	WEFF04PL	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAPL	-0.39	-0.47	-0.55	$V^{½}$	12
gain factor	KPPL	48	58	68	$µA/V^2$	7
drain-source breakdown 0.35µm	BVDS035PL	-6	< -7		V	14
saturation current 0.35µm	IDS035PL	-200	-270	-350	µA/µm	15
subthreshold leakage current 0.35µm	SLEAK035PL		-250	-4500	pA/µm	17
gate oxide breakdown	BVGOXPL	-7	< -8		V	19
Output conductance 10/1.2	GDS10X12PL	0.5	1.18	1.85	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.35µm	LACT035PL		0.28		µm	27
subthreshold leakage current 0.35µm @ 125 C	SLPL125		-50	-250	nA/µm	17
threshold voltage narrow channel 0.4x10	VTO04X10PL		-0.47		V	6
threshold voltage small channel 0.4x0.35	VTO04X035PL		-0.50		V	6
threshold voltage temperature coefficient	TCVTOPL		1.86		mV/K	13
effective substrate doping	NSUBPL		136		$10^{15}/cm^3$	12
effective mobility	UOPL		126		cm^2/Vs	8
mobility exponent	BEXPL		-1.28		-	13

3.6.3 Low VTH MOS N-Channel High Voltage Electrical Parameters : NMOSHL

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage 3µm	VTO3NHL	0.29	0.39	0.49	V	6
drain-source breakdown 3µm	BVDS3NHL	15	19		V	14
on-resistance 3µm	RON3NHL	8	12	16	kΩ µm	20

Information parameters	Symbol	Min	Typ	Max	Unit	Note
saturation current 3µm	IDS3NHL	170	210	250	µA/µm	15
substrate current 3µm	ISUB3NHL		1.2	3	µA/µm	16

3.6.4 Capacitances

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 - DIFF (gate oxide)						
NMOS GATE – NDIFF overlap	CGSDONL	0.011	0.012	0.013	fF/µm	27
PMOS GATE - PDIFF overlap	CGSDOPL	0.050	0.056	0.062	fF/µm	27
NMOS GATE - BULK overlap	CGBONL	0.10	0.11	0.12	fF/µm	28
PMOS GATE - BULK overlap	CGBOPL	0.10	0.11	0.12	fF/µm	28
POLY1 – LDD (gate oxide)						
GATE – LDD overlap	CGSDLNL	0.30	0.35	0.40	fF/µm	26
GATE – LDD overlap	CGSDLPL	0.21	0.24	0.27	fF/µm	26

3.7 5 Volt low VTH Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

The transistors NMOSML and PMOSML use mid-oxide as gate insulator.

3.7.1 Low Voltage MOS 5V N-Channel Electrical Parameters : NMOSML

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10NML	0.47	0.57	0.67	V	6
threshold voltage short channel 10x0.5	VTO10X05NML	0.41	0.51	0.61	V	6
threshold voltage short channel 10x0.5 (measured in linear region)	VT_5N3L	0.52	0.62	0.72	V	6
effective channel length 0.5µm	LEFF05NML	0.35	0.45	0.55	µm	10
effective channel width 0.4µm	WEFF04NML	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMANML	0.79	0.94	1.09	$V^{½}$	12
gain factor	KPNML	85	105	125	µA/V²	7
drain-source breakdown 0.5µm	BVDS05NML	7	> 9		V	14
saturation current 0.5µm	IDS05NML	440	520	600	µA/µm	15
substrate current 0.5µm	ISUB05NML		2	5	µA/µm	16
subthreshold leakage current 0.5µm	SLEAK05NML		4	75	pA/µm	17
gate oxide breakdown	BVGOXNML	12	> 15		V	19
gate oxide breakdown	BVGOXNML	12	15		V	19
Output conductance 10/1.2	GDS10X12NML	0.26	0.80	1.34	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.5µm	LACT05NML		0.25		µm	27
subthreshold leakage current 0.5µm @ 125 C	SLNML125		1.5	14.0	nA/µm	17
threshold voltage narrow channel 0.4x10	VTO04X10NML		0.51		V	6
threshold voltage small channel 0.4x0.5	VTO04X05NML		0.48		V	6
threshold voltage temperature coefficient	TCVTONML		-1.4		mV/K	13
effective substrate doping	NSUBNML		174		$10^{15}/cm^3$	12
effective mobility	UONML		435		cm^2/Vs	8
mobility exponent	BEXNML		-1.72		-	13

3.7.2 Low VTH MOS 5V P-Channel Electrical Parameters: PMOSML

Negative values are considered as absolute values for their Min/Max limits.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage long channel 10x10	VTO10X10PML	-0.55	-0.65	-0.75	V	6
threshold voltage short channel 10x0.5	VTO10X05PML	-0.57	-0.67	-0.77	V	6
threshold voltage short channel 10x0.5 (measured in linear region)	VT_5P3L	-0.63	-0.73	-0.83	V	6
effective channel length 0.5µm	LEFF05PML	0.58	0.68	0.78	µm	10
effective channel width 0.4µm	WEFF04PML	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAPML	-0.57	-0.67	-0.77	$V^{½}$	12
gain factor	KPPML	25	31	37	$µA/V^2$	7
drain-source breakdown 0.5µm	BVDS05PML	-7	< -8		V	14
saturation current 0.5µm	IDS05PML	-170	-235	-300	µA/µm	15
subthreshold leakage current 0.5µm	SLEAK05PML		-0.12	-3	pA/µm	17

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
gate oxide breakdown	BVGOXPML	-12	< -15		V	19
Output conductance 10/1.2	GDS10X12PML	0.14	0.51	0.88	µA/V	18

Information parameters	Symbol	Min	Typ	Max	Unit	Note
active channel length 0.5µm	LACT05PML		0.41		µm	27
subthreshold leakage current 0.5µm @ 125 C	SLPML125		-0.4	-2.5	nA/µm	17
threshold voltage narrow channel 0.4x10	VTO04X10PML		-0.54		V	6
threshold voltage small channel 0.4x0.5	VTO04X05PML		-0.6		V	6
threshold voltage temperature coefficient	TCVTOPML		2.2		mV/K	13
effective substrate doping	NSUBPML		71		$10^{15}/cm^3$	12
effective mobility	UOPML		135		cm^2/Vs	8
mobility exponent	BEXPML		-1.2		-	13

3.7.3 Low VTH MOS N-Channel High Voltage Electrical Parameters : NMOSMHL

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
threshold voltage 3µm	VTO3NMHL	0.43	0.53	0.63	V	6
drain-source breakdown 3µm	BVDS3NMHL	17	21		V	14
on-resistance 3µm	RON3NMHL	7	11	15	kΩ µm	20

Information parameters	Symbol	Min	Typ	Max	Unit	Note
saturation current 3µm	IDS3NMHL	200	240	280	µA/µm	15
substrate current 3µm	ISUB3NMHL		0.7	5	µA/µm	16

3.7.4 Capacitances

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY1 - DIFF (mid-oxide)						
NMOS GATE – NDIFF overlap	CGSDOMNL	0.0008	0.001	0.0012	fF/µm	27
PMOS GATE - PDIFF overlap	CGSDOMPL	0.056	0.064	0.072	fF/µm	27
NMOS GATE - BULK overlap	CGBOMNL	0.10	0.11	0.12	fF/µm	28
GATE - BULK overlap	CGBOMPL	0.10	0.11	0.12	fF/µm	28
POLY1 – LDD (mid oxide)						
NMOS GATE – LDD overlap	CGSDLMNL	0.381	0.434	0.486	fF/µm	27
PMOS GATE – LDD overlap	CGSDLMPL	0.140	0.160	0.180	fF/µm	27

3.8 Metal 4 Module Parameters

Please refer to "1.2 Process Family " for information on the processes where this module is implemented.

Important application note:

Implementation of metal 4 module results in changing of several CMOS core module parameters. Parameters of this section override corresponding parameters of section “3.2 CMOS Core Module Parameters”.

3.8.1 Structural and Geometrical Parameters

Please refer to chapter ”3.13 Schematic Description” for a general overview of the backend of the 0.35um process.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
metal3 thickness	TMET3	540	640	740	nm	3
metal3-metal4 metal oxide thickness	TIMD3	620	1000	1380	nm	1
metal4 thickness	TMET4	775	925	1075	nm	3

3.8.2 Sheet Resistances

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 sheet resistance	RMET3		70	100	mΩ/□	22
MET4 sheet resistance	RMET4		40	80	mΩ/□	22
VIA3 resistance 0.5x0.5µm²	RVIA3		1.2	3	Ω/via	24

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 effective width 0.6 µm	WMET3		0.5		µm	21
MET4 effective width 0.6 µm	WMET4		0.6		µm	21
MET3 temperature coefficient	TCMET3		3.4		10^{-3}/K	23
MET4 temperature coefficient	TCMET4		3.5		10^{-3}/K	23

3.8.3 Capacitances

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 – WELL						
MET3 – WELL area	CM3FOX	0.006	0.008	0.011	fF/µm²	25
MET3 – WELL perimeter	CM3FOXF	0.028	0.031	0.034	fF/µm	26
MET3 - POLY1/POLY2						
MET3 - POLY1/POLY2 area	CM3P	0.007	0.009	0.013	fF/µm²	25
MET3 - POLY1/POLY2 perimeter	CM3PF	0.029	0.032	0.036	fF/µm	26
MET3 - MET1						
MET3 - MET1 area	CM3M	0.010	0.014	0.020	fF/µm²	25
MET3 - MET1 perimeter	CM3MF	0.033	0.036	0.041	fF/µm	26
MET3 - MET2						
MET3 - MET2 area	CM3M2	0.026	0.036	0.059	fF/µm²	25
MET3 - MET2 perimeter	CM3M2F	0.043	0.048	0.056	fF/µm	26
MET4 – WELL						
MET4 – WELL area	CM4FOX	0.005	0.006	0.008	fF/µm²	25
MET4 – WELL perimeter	CM4FOXF	0.027	0.029	0.032	fF/µm	26
MET4 - POLY1/POLY2						
MET4 - POLY1/POLY2 area	CM4P	0.005	0.006	0.009	fF/µm²	25
MET4 - POLY1/POLY2 perimeter	CM4PF	0.027	0.030	0.034	fF/µm	26
MET4 - MET1						
MET4 - MET1 area	CM4M	0.006	0.008	0.012	fF/µm²	25
MET4 - MET1 perimeter	CM4MF	0.030	0.033	0.037	fF/µm	26
MET4 - MET2						
MET4 - MET2 area	CM4M2	0.010	0.014	0.020	fF/µm²	25
MET4 - MET2 perimeter	CM4M2F	0.034	0.039	0.044	fF/µm	26
MET4 – MET3						
MET4 – MET3 area	CM4M3	0.026	0.036	0.059	fF/µm²	25
MET4 – MET3 perimeter	CM4M3F	0.046	0.053	0.062	fF/µm	26
COUPLING CAPACITANCES						
MET3 – MET3 coupling	CM3M3		0.085		fF/µm	29
MET4 – MET4 coupling	CM4M4		0.097		fF/µm	29

3.9 Thick Metal Module Parameters

Please refer to "1.2 Process Family " for information on the processes where this module is implemented.

Important application note:

Implementation of thick metal module results in changing of several CMOS core module and metal 4 module parameters. Parameters of this section override corresponding parameters of section “3.2 CMOS Core Module Parameters” and of section “3.8 Metal 4 Module Parameters”.

3.9.1 Structural and Geometrical Parameters

Please refer to chapter ”3.13 Schematic Description” for a general overview of the backend of the 0.35um process.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
metal3 thickness	TMET3	540	640	740	nm	3
thick metal-metal3 oxide thickness	TIMDT	600	1000	1200	nm	1
thick metal thickness	TMETT	2500	2800	3100	nm	3

3.9.2 Sheet Resistances

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 sheet resistance	RMET3		70	100	mΩ/□	22
METT sheet resistance	RMETT		10	13	mΩ/□	22
VIA3 resistance 0.5x0.5µm²	RVIA3T		1.2	3	Ω/via	24

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 effective width 0.6 µm	WMET3		0.5		µm	21
MET3 temperature coefficient	TCMET3		3.4		10^{-3}/K	23
METT effective width 2.5µm	WMETT		2.5		µm	21
METT temperature coefficient	TCMETT		3.5		10^{-3}/K	23

3.9.3 Capacitances

Information parameters	Symbol	Min	Typ	Max	Unit	Note
MET3 – WELL						
MET3 – WELL area	CM3FOXT	0.006	0.008	0.011	fF/µm²	25
MET3 – WELL perimeter	CM3FOXFT	0.029	0.032	0.035	fF/µm	26
MET3 – POLY1						
MET3 – POLY area	CM3PT	0.007	0.009	0.013	fF/µm²	25
MET3 - POLY perimeter	CM3PFT	0.030	0.033	0.037	fF/µm	26
MET3 - MET1						
MET3 - MET1 area	CM3MT	0.010	0.014	0.020	fF/µm²	25
MET3 - MET1 perimeter	CM3MFT	0.034	0.037	0.042	fF/µm	26
MET3 - MET2						
MET3 - MET2 area	CM3M2T	0.026	0.036	0.059	fF/µm²	25
MET3 - MET2 perimeter	CM3M2FT	0.043	0.048	0.057	fF/µm	26
METT – WELL						
METT – WELL area	CMTFOX	0.005	0.006	0.008	fF/µm²	25
METT – WELL perimeter	CMTFOXF	0.033	0.037	0.043	fF/µm	26
METT - POLY1/POLY2						
METT - POLY area	CMTP	0.005	0.006	0.009	fF/µm²	25
METT - POLY perimeter	CMTPF	0.034	0.038	0.046	fF/µm	26
METT - MET1						
METT - MET1 area	CMTM	0.007	0.008	0.012	fF/µm²	25
METT - MET1 perimeter	CMTMF	0.037	0.042	0.050	fF/µm	26
METT - MET2						
METT - MET2 area	CMTM2	0.011	0.014	0.021	fF/µm²	25
METT - MET2 perimeter	CMTM2F	0.043	0.050	0.060	fF/µm	26
METT – MET3						
METT – MET3 area	CMTM3	0.030	0.036	0.061	fF/µm²	25
METT – MET3 perimeter	CMTM3F	0.061	0.068	0.083	fF/µm	26
COUPLING CAPACITANCES						
MET3 – MET3 coupling	CM3M3		0.085		fF/µm	29
METT – METT coupling	CMTMT		0.099		fF/µm	29

3.10 High Resistive Poly Module Parameters

Please refer to "1.2 Process Family “ for information on the processes where this module is implemented.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
RPOLYH sheet resistance	RPOLYH	1.0	1.2	1.4	kΩ/□	21
RPOLYH effective width 0.8 µm	WPOLYH	0.50	0.60	0.70	µm	21
MET1-RPOLYH contact resistance 0.4x0.4µm²	RCNTMPH		70	150	Ω/cnt	24

Information parameters	Symbol	Min	Typ	Max	Unit	Note
RPOLYH temperature coefficient linear term W > 4 µm	TC1POLYH		-0.75		10^{-3}/K	23
RPOLYH temperature coefficient quadratic term	TC2POLYH		3.82		10^{-6}/K^2	23
RPOLYH voltage coefficient (W/L=0.8/100)	VCRPOLYH		-0.8		10^{-3}/V	43
RPOLYH extrinsic sheet resistance (contact region)	RPOLYHE		150		Ω/□	21

3.10.1 High Precision Poly2 Sheet Resistance: RPOLY2PH

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 sheet resistance	RPOLY2PH	44	50	56	Ω/□	21
POLY2 effective width 0.65 µm	WPOLY2PH	0.30	0.40	0.50	µm	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
POLY2 sheet resistance temp. coefficient linear term W > 4 µm	TC1POLY2PH		0.59		10^{-3}/K	23
POLY2 sheet resistance temp. coefficient quadratic term	TC2POLY2PH		7.7		10^{-7}/K^2	23

The values specified for RPOLY2PH are only valid for the high resistive poly module.

3.11 Low TC Poly Module Parameters

Please refer to "1.2 Process Family “ for information on the processes where this module is implemented.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
RPOLYZ sheet resistance	RPOLYZ	540	650	760	Ω/□	21
RPOLYZ effective width 0.8 µm	WPOLYZ	0.47	0.57	0.67	µm	21
MET1-RPOLYZ contact resistance 0.4x0.4µm²	RCNTMPZ		70	150	Ω/cnt	21

Information parameters	Symbol	Min	Typ	Max	Unit	Note
RPOLYZ temperature coefficient linear term	TC1POLYZ		-56	-120	10^{-6}/K	23
RPOLYZ temp. coefficient quadratic term	TC2POLYZ		1.7		10^{-6}/K	23
RPOLYZ ΔR for T=-40°C to +150°C	DRRPZ		2.7	4.5	%	52
RPOLYZ effective length 3 µm	LPOLYZ		3.36		µm	21
RPOLYZ voltage coefficient W=0.8µm	VCRPOLYZ		-0.7		10^{-3}/V	43

3.12 Schottky Barrier Diode Module Parameters

Please refer to "1.2 Process Family “ for information on the processes where this module is implemented.

Pass/Fail parameters	Symbol	Min	Typ	Max	Unit	Note
forward current (0.4X12 um)	IFW12SBD5	23	45		µA	53
leakage current (0.4X12 um)	IS12SBD5		0.12	1.0	µA	32
NWELL to substrate breakdown voltage	BVNW12SBD5	28	32		V	31

Information parameters	Symbol	Min	Typ	Max	Unit	Note
reverse voltage (0.4X12 um)	RV12SBD5		-10		V	55
junction capacitance	CJSBD5		2.74		fF/µm²	30
grading coefficient	MSBD5		0.17		-	30
junction potential	PBSBD5		0.29		V	30
junction current temperature exponent coefficient	XTISBD5		5		-	58
NWELL to substrate leakage current	ISNW12SBD5		0.22		pA	32
NWELL to substrate junction capacitance	CJNWSBD5		3.97		fF/µm²	30
NWELL to substrate grading coefficient	MNWSBD5		0.33		-	30
NWELL to substrate junction potential	PBNWSBD5		0.56		V	30

3.13 Schematic Description of Geometrical Parameters

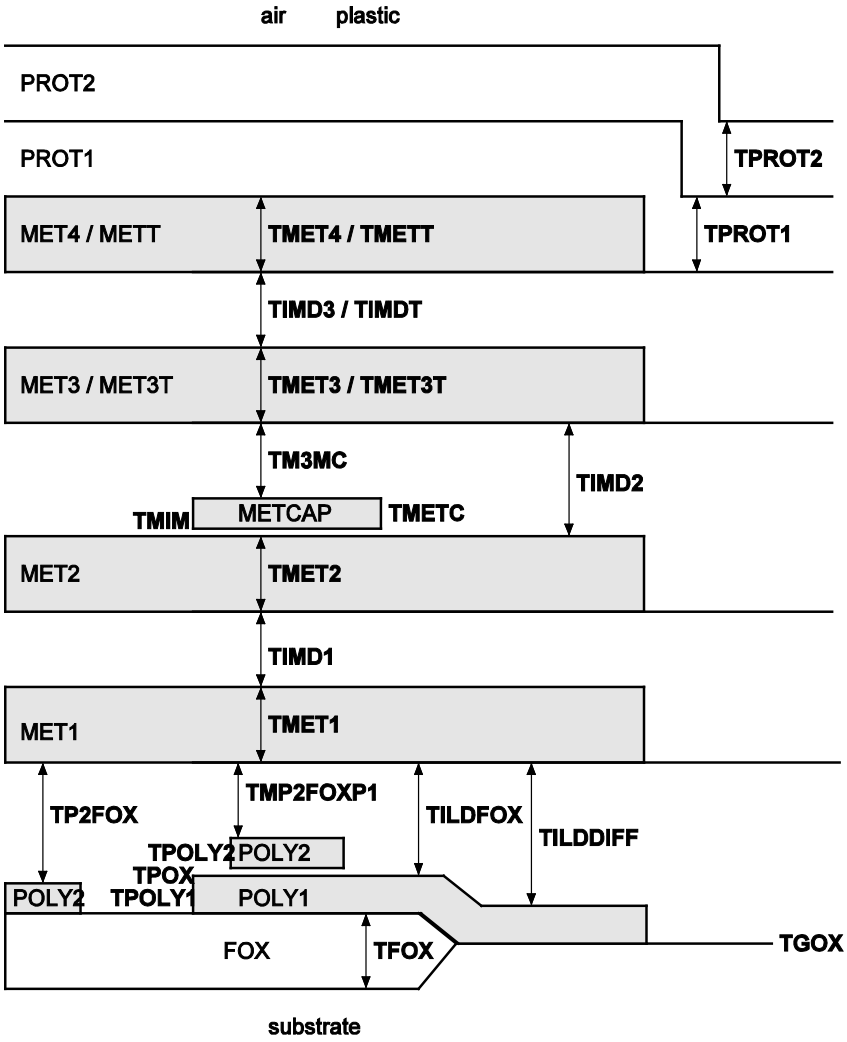


Fig.3.9: Schematic cross section of the backend for the 0.35um process

3.14 Notes / Measurement Conditions

Note 1 **Oxide, nitride and polysilicon thickness monitoring**
is performed by optical interference or ellipsometry at large area structures within the wafer process or on monitor wafers. The parameter values describe the oxide, nitride and polysilicon thickness of fully prepared wafers.
Passivation thickness measured on planar surfaces larger 10x10µm².

Note 2 **Oxide capacitance / oxide thickness**
The capacitance per area COX of a large area capacitor is measured. The oxide thickness TOX is calculated from:

$$TOX = \frac{\varepsilon_0 \cdot \varepsilon_{ox}}{COX}$$

with $\varepsilon_{FOX,GOX,MOX,MIM} = 3.9$, $\varepsilon_{POX} = 4.0$, $\varepsilon_0 = 8.85.10^{-12}$ F/m

Connection scheme:
CPOLY top plate = low, bottom plate = high
CMIM top plate = high, bottom plate = low
CPMIM: common plate (p2m1) = high, top plate (metcapp1) = low

In case of CPMIM the area capacitance is referenced to the area of MIM cap.

Note 3 **Metal thickness**
is monitored by resistivity on monitor wafer or by mechanical step measurement. The specified value describes the thickness of all layers which finally generate the corresponding metal layer.

Note 4 **Junction depth**
is extracted from SIMS or SRS measurements. The measurements are performed on fully processed wafers.

Note 5 **Wafer substrate resistivity and wafer thickness**
Wafer substrate resistivity and wafer thickness is given in reference to wafer supplier specification.

Note 6 **Threshold voltage VTO10X10, VTO10X035, VTO04X10, VTO04X035, VTO10X05, VTO04X05**

The linearly extrapolated threshold voltage with zero substrate bias is measured in saturation: Gate and drain are connected to one voltage source, source and bulk are connected to ground. The voltage is swept in order to find the maximum slope of the square root of the drain current as a function of the gate voltage. A linear regression is performed around this operating point:

Error! Bookmark not defined. $$\sqrt{IDS} = \sqrt{\frac{KP}{2} \cdot \frac{Weff}{Leff}} \cdot (VGS - VTO)$$

Threshold voltage VT_N3, VT_P3, VT_5N3, VT_5P3

The linearly extrapolated threshold voltage with zero substrate bias is measured in the linear region: Source and bulk are connected to ground, drain is set to VD=0.1V. The gate voltage is swept in order to find the maximum gm

$$IDS = KP \cdot \frac{Weff}{Leff} \cdot VDS \cdot \left(VGS - VTH - \frac{VDS}{2} \right)$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices. The intercept with the x-axis is taken as VTO.

Note 7 **Gain factor**

KP is measured from the slope of the large transistor, where Weff / Leff ~ W/L.
The drain voltage is forced to 0.1V, source and bulk are connected to ground. The gate voltage is swept to find the maximum slope of the drain current as a function of the gate voltage. A linear regression is performed around this operating point:

$$IDS = KP \cdot \frac{Weff}{Leff} \cdot VDS \cdot (VGS - VTO - \frac{VDS}{2})$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices.

Note 8 **Mobility**

The mobility UO is calculated from KP (refer to note 7) and COX (refer to note 2):

$$UO = \frac{KP}{COX}$$

Note 9 **Field threshold**

Drain is set to 3.3V. Source and bulk are connected to ground. The voltage at the gate is swept in a binary search within the voltage limits 10V ≤ VTFP(N/P) ≤ 50V until the current reaches 10nA/µm.
The voltage sweep is positive for n-channel devices and negative for p-channel devices.

Note 10 **Effective channel length**

The effective channel length is calculated from two wide transistors of different length.
Drain is set to V_d = 0.1V, source and bulk are connected to ground.
The gate Voltage V_{gm} is determined, where the slope of drain current I_d on gate voltage V_g is a maximum. Then the gate is forced to $V_g = V_{gm}$, $(V_{gm} + V_{cc})/2$, and V_{cc} respectively, and the drain current I_{ds} is recorded.

From a fit to

$$I_{DS} = \frac{\eta(V_{GS} - V_{TH}) \cdot V_{DS}}{1 + \alpha(V_{GS} - V_{TH})}$$

the parameters η, α and V_{th} are obtained. The effective channel length L_{eff} and source-drain resistance R_{DS} is calculated by

$$L_{eff} = \frac{\eta_L(L_S - L_L)}{\eta_L - \eta_S} \qquad R_{DS} = \frac{\alpha_L - \alpha_S}{\eta_L - \eta_S}$$

with subscript L and S denoting the long and short transistor respectively.

Note 11 **Effective channel width**

The effective gain factor KP' = KP · Weff / Leff is measured for a W - array of long transistors according to threshold voltage measurement (refer to note 7 and note 6). The width reduction DW = W - Weff is calculated from the x-intercept of the linear regression:

$$KP' = \frac{KP}{Leff} \cdot (W - DW)$$

Note 12 **Body effect and effective substrate doping concentration**

The threshold voltages VTH as a function of substrate bias voltage from 0 to -2V (+2V for p-channel) are extracted by linear regressions as described in note 6 . The body factor GAMMA is then extracted from the slope of VTH as a function of $(2 \cdot PHI - VBS)^{1/2}$ by another linear regression:

$$VTH = VTO + GAMMA \cdot \left(\sqrt{2 \cdot PHI - VBS} - \sqrt{2 \cdot PHI}\right)$$

The effective substrate doping concentration NSUB is calculated from GAMMA and COX (refer to note 2):

$$GAMMA = \frac{\sqrt{2 \cdot \varepsilon_0 \cdot \varepsilon_{si} \cdot q \cdot NSUB}}{COX} \qquad \varepsilon_{SI} = 11.7$$

The surface potential PHI is a function of the doping concentration NSUB and the intrinsic carrier concentration NI

$$PHI = \frac{kT}{q} \ln\left(\frac{NSUB}{NI}\right)$$

PHI is recalculated using the extracted value of NSUB. This updated value of PHI is then used again in the extraction of GAMMA and NSUB in an iterative procedure.

Note 13 **Temperature coefficient of threshold voltage**
Temperature exponent of mobility
The threshold voltage VTO (refer to note 6) and the gain factor KP (refer to note 7) are measured as a function of the temperature T from 25°C to 125°C. The temperature coefficient of the threshold voltage TCV and the temperature exponent of the mobility BEX are calculated from the slope of the following linear regressions at T0=27°C:

$$VTO(T) = VTO(T0) + TCV \cdot (T - T0)$$

$$\ln\left[KP(T)\right] = \ln\left[KP(T0)\right] + BEX \cdot \left[\ln(T) - \ln(T0)\right]$$

Note 14 **Drain-source breakdown voltage**
Gate, source and bulk are connected to ground. The drain voltage is swept until the current reaches 10 nA/µm (referred to transistor width) at the breakdown voltage BVDS or until the voltage limit is reached.

Note 15 **Saturation current**
Source and bulk are connected to ground. Gate and drain are set to

gate: 3.3V	drain: 3.3V	for NMOS and NMOSL
gate: -3.3V	drain: -3.3V	for PMOS and PMOSL
gate: 5V	drain: 5V	for NMOSM and NMOSML
gate: -5V	drain: -5V	for PMOSM and PMOSML
gate: 3.3V	drain: 15V	for NMOSH and NMOSHL
gate: 5V	drain: 15V	for NMOSMH and NMOSMHL

The transistor saturation current IDS is measured at the drain. IDS is specified per drawn transistor width.

Note 16 **Substrate current**
Source and bulk are forced to 0V. The drain is set to

3.3V	for NMOS and NMOSL
5V	for NMOSM and NMOSML
15V	for NMOSH, NMOSMH, NMOSHL and NMOSMHL

The gate voltage is swept within the allowed operating range in order to find the maximum substrate current ISUB. ISUB is specified per drawn transistor width.

Note 17 **Sub-threshold leakage current**
The drain is set to 3.3V, source and bulk are connected to ground. The drain current as a function of VGS is measured within the sub-threshold region. A linear regression of log(ID)=f(VGS) is performed. The intercept with log(ID)-axis is taken as SLEAK. SLEAK is specified per drawn transistor width.

Note 18 **Output conductance:**

The Threshold voltage is extracted in saturation as explained in note 6

A vd sweep is performed at vg=vth+250mV and the drain current id is measured, source and bulk are connected to ground.

GDS is defined as the derivative of id at vd=vdx.

vdx=0.8V for all NMOSI

vdx=1.0V for all PMOSI

Note 19 **Gate oxide breakdown**

The voltage at the capacitor is swept until a current of 10 nA/µm² is reached at the breakdown voltage BV.

Note 20 **On-resistance**

The drain is set to 0.2V, the gate is forced to 3.3V for NMOSH and NMOSHL and 5V for NMOSMH and NMOSMHL, source and bulk are connected to ground. The drain current IDS is measured. The drain resistance RON = 0.2V/IDS is calculated. RON is referred to drawn transistor width.

Note 21 **Sheet resistance and effective resistor width and length**

A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at the first terminal. The measurements are performed for an array of widths W for Weff measurement of long resistors (Leff ~ L) and array of L for Leff measurements for width resistors (Weff~W). The sheet resistance per square R is calculated from the slope and the width reduction DW = W - Weff and DL = L-Leff is calculated from the x-intercept of the linear regression:

$$\frac{IRES}{VRES} = \frac{1}{R \cdot Leff} \cdot (W - DW); \quad \frac{IRES}{VRES} = \frac{Weff}{R \cdot (L - DL)}$$

Note 22 **Metal sheet resistance**

A minimum width metal line (width Wmin and length L) over most critical topography is measured and the resistance RMET is calculated by dividing the total resistor value RM by the number of drawn squares:

RMET = RM / (L / Wmin)

Note 23 **Temperature coefficient of sheet resistance**

The sheet resistance R (refer to note 21 and 22) is measured as a function of the temperature T from 25°C to 125°C. For RPOLY2, RPOLY2P, RPOLY2PH and RPOLYH the temperature range is -40°C to 180°C. The temperature coefficient of the resistance TCR is calculated from the slope of the following linear regression at T0=27°C:

$$\frac{\mathrm{R(T)}}{\mathrm{R(T0)}} = 1 + \mathrm{TCR1}\cdot\left(\mathrm{T}-\mathrm{T0}\right) + \mathrm{TCR2}\cdot\left(\mathrm{T}-\mathrm{T0}\right)^2$$

Temperature coefficient of rpolyz

The resistance R is measured as a function of the temperature T from -40°C to 180°C for diverse geometries. The temperature coefficient is calculated from global fitting of the whole resistance model described below:

Sheet resistance: $$R_0 = RSH \cdot \frac{l - LD}{w - WD}$$

Linear voltage coefficient: $$RVL = \frac{l}{w} \cdot RVLN$$

Temperature dependent quadratic voltage coefficient:

$$RVQ = \frac{1}{R_0} \cdot \left[RTH \cdot TCR1 \cdot \left(\frac{l}{w}\right)^{WEX} \cdot \left(T - T_0\right) + RT0W \right]$$

Voltage dependency: $$RnV = R_0 \left[1 + RVL\left(\frac{V}{l}\right) + RVQ\left(\frac{V}{l}\right)^2 \right]$$

Temperature dependency: $$RT = RnV\left[1 + TCR1\cdot\left(T - T_0\right) + TCR2\cdot\left(T - T_0\right)^2\right]$$

Note 24 **Contact resistances**

The contact resistances RCNTMDN, RCNTMDP, RCNTMP, RCNTMP2 and RCNTMPZ are measured on single contacts. The contact resistances RVIA, RVIA2, RVIA3 and RVIA2C are calculated from the resistance of a long contact string divided by the number of contacts.

Note 25 **Area capacitance**

The dielectric thickness TOX is measured optically (refer to note 1). The capacitance per area COX of a large area capacitor is calculated from:

$$COX = \frac{\varepsilon 0 \cdot \varepsilon ox}{TOX}$$

with

ε_{ox} = 3.9 TFOX, TPROT1

ε_{ox} = 4.0 TILDFOX, TILDDIFF, TPOX

ε_{ox} = 4.1 TIMD1, TIMD2, TIMD3

ε_{ox} = 7.9 TPROT2

$\varepsilon_0 = 8.85 \cdot 10^{-12}$ F/m

Note 26 **Fringing capacitance**

The fringing capacitance per length (one edge) of a single minimum width interconnect line is calculated with the FEM simulator SCAP (Institute for Microelectronics, University Vienna). Adjacent structures reduce this value.

Note 27 **Active channel length and MOS overlap capacitance to source/drain**

The bias dependent lightly doped source/drain MOS overlap capacitance CGSDL and the bias independent non LDD MOS overlap capacitance CGSDO per width (one edge) are extracted from gate to source/drain capacitance $C_{Gate\text{-}SD}$ measurements of long perimeter gate structures (W/L >> 1).

$$\left(C_{Gate\text{-}SD}\right)\Big|_{VGS=VFB} - \left(C_{Gate\text{-}SD}\right)\Big|_{Accumulation} = 2 \cdot W \cdot L_{ov} \cdot C_{OX'} \cdot \frac{\gamma_{ov}}{\gamma_{ov} + \sqrt{2 \cdot \Phi_t}}$$

$$\gamma_{ov} = \frac{\sqrt{2 \cdot q \cdot N_{LDD} \varepsilon_0 \varepsilon_{Si}}}{C_{OX'}} \quad \gamma_{ov(NMOS)} = 3.326\ V^{-1/2} \quad \gamma_{ov\ (PMOS)} = 1.159\ V^{-1/2}$$

$$\gamma_{ov\ (NMOSM)} = 2.229\ V^{-1/2} \quad \gamma_{ov\ (PMOSM)} = 2.301\ V^{-1/2}$$

$$C_{GSDL} = C_{OX'} \cdot L_{OV}$$

$$C_{GSDO} = \frac{1}{2}\left(C_{Gate-SD}\right)\Big|_{Accumulation}$$

$$L_{ACTIVE} = L - 2 \cdot L_{ov}$$

Note 28 **MOS overlap capacitance to bulk**

The MOS overlap capacitance per length (both edges) is calculated from:

$$CGBO = 2 \cdot \left(WD \cdot CPFOX + CPFOXF \right)$$

The results are in conformity with experimental capacitance measurements of long perimeter gate structures (W/L <<1).

Note 29 **Coupling capacitance**

The coupling capacitance per length of adjacent metal or poly lines with minimum spacing and minimum width is calculated by using the FEM simulator SCAP (Institute for Microelectronics, University Vienna).

Note, that in case of adjacent lines the fringing capacitance (refer to note **26**) is reduced by about 80% (of the coupling capacitance, if the coupling capacitance is less than the fringing capacitance).

Note 30 **Junction capacitances**

The junction capacitances C of an array of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance per drawn area CJ, the junction capacitance per drawn perimeter CJSW, the junction potential PB, the area junction grading coefficient MJ and the sidewall junction grading coefficient MJSW are then extracted from:

$$C = \frac{W \cdot L \cdot CJ}{\left(1 + \frac{V}{PB}\right)^{MJ}} + \frac{2 \cdot (W + L) \cdot CJSW}{\left(1 + \frac{V}{PB}\right)^{MJSW}}$$

Note 31 **Diode breakdown voltage**

The diode reverse voltage is swept until the diode reverse current reaches 10 nA/µm² at the breakdown voltage BV.

Note: The well to substrate breakdown is dominated by the diffusion to substrate breakdown if the well enclosure of the diffusion is not sufficient.

Note 32 **Diode leakage**

Leakage currents IS of a large area diode (W=L) and of a long perimeter diode (W<<L) are measured at 3.3 V reverse bias voltage. The leakage current density per drawn area JS and the leakage current density per drawn perimeter JSSW are calculated from

$$IS = JS \cdot W \cdot L + JSSW \cdot \left(2 \cdot W + 2 \cdot L \right)$$

Note 33 **Vertical PNP**

The current gain of the CMOS vertical PNP bipolar transistor (PDIFF - NWELL - p-substrate) with the specified emitter area is measured as follows:
Base and substrate are connected to 0 V. A current IE = 10µA is forced into the emitter. The base-emitter voltage VBEV is measured. The current IB is measured at the base. The current gain BETAV is calculated:

$$BETAV = -\frac{IE}{IB} - 1$$

The emitter current is then swept to higher values until current gain is reduced to half of the value of BETA. The half gain collector current ICHB is calculated from:

$$ICHB = -IE - IB$$

Note 34 **Lateral PNP**

The current gain of the CMOS lateral PNP bipolar transistor (PDIFF - NWELL - PDIFF) with the specified emitter area is measured as follows:
Base, collector and substrate (= vertical parasitic collector) are connected to 0 V. The GATE is connected to 2V. The specified emitter current IE is forced into the emitter. The base-emitter voltage VBEL is measured. The current IB is measured at the base and the current IC is measured at the collector. The current gain BETAL is calculated from:

$$BETAL = \frac{IC}{IB}$$

The parasitic vertical current gain at IE = 1µA is calculated from:

$$BETAVL = -\frac{IE}{IB} - BETAL - 1$$

Note 35 **Early voltage**

The current IB, which has been measured for the calculation of the current gain BETA is forced into the base. The substrate is connected to 0V. The collector is connected to 0V and the gate is connected to 3.3V for the lateral transistor. The emitter voltage is swept to find the minimum slope of the emitter current as a function of the emitter voltage. The Early voltage VAF is taken from the x-intercept of a linear regression, which is performed around this operating point.

Note 36 **Capacitor oxide breakdown**

The voltage at the capacitor is swept until a current of 10 nA/µm² at the breakdown voltage BV is reached.

Note 37 **Capacitance linearity**

The terminal voltage is swept from –5V to +5V and the corresponding capacitance value C is measured at f=100kHz. The linearity is calculated from:

$$\frac{C}{C(0V)} = 1 + VC1 \cdot V + VC2 \cdot V^2$$

Connection scheme:
Cpoly (70x180): top plate = low, bottom plate = high

Cmim (16 units of 25x25): top plate = high, bottom plate = low

Cpmim (16 units of 30x30): common plate (p2m2) = low, top plate (metcapp1) = high

Note 38 **Capacitance temperature dependence**

Capacitance is measured from 0°C to 175°C and the slope TCPOX is calculated by linear regression method.

$$TCPOX = \frac{d(\Delta C)}{dT} \cdot \frac{1E6}{C(25°C)}$$

Note 39 **Capacitor leakage**

Leakage current ILEAK of a large area capacitor is measured at ±3.3V at T=125°C. The leakage current density per drawn area LKCPOX is calculated from:

$$LKCPOX = \frac{ILEAK}{A}$$

Note 40 **Capacitor voltage ratio**

The capacitor values biased with +5V, -5V and 0V are measured and the maximum ratio is calculated from:

$$x\_C5C0 = \max\left[\frac{C(\pm 5V)}{C(0V)}\right]$$

Note 41 **Varactor CVAR: quality factor QF**

The quality factor QF for 1 pF is extracted from 2 port s-parameter measurements at 2.4 GHz:

Error! Bookmark not defined. $QF = \frac{\mathrm{Im}|Z_1|}{\mathrm{Re}|Z_1|}$

Note 42 **Varactor CVAR: tuning range gamma**

The tuning range gamma for 1 pF is extracted from 2 port s-parameter measurements at 2.4 GHz:

$$gamma = \frac{C_{max} - C_{min}}{C_{max} + C_{min}} \cdot 100$$

Note 43 **Voltage coefficient**
The voltage coefficient of a poly resistor is measured by applying a bias voltage to the bulk substrate. The slope of RPOLYx is then calculated by linear regression method.

Note 44 **MOS varactor**
The MOS Varactor capacitance is measured. “Poly 1” is connected to ground, “Ndif “ is biased and substrate is floating . Biase Voltages are –1,0,1 (CVARM Bias V=-1, CVAR0 Bias V=0V, CVARP Bias V=+1V

Note 45 **Resistance Fuse**
A current of 200µA is forced into the unfused poly resistor. From the voltage drop across the fuse the resistance is calculated.

Note 46 **Resistance Fuse burnt**
To fuse the resistor, one side of the resistor is connected to ground, the other side is connected to the source of the fusing transistor. Drain is connected to 3.3V. A pulse of 3.3V height and 10µs length is applied to the gate to open the transistor and provide the fusing current to the fuse. A backup capacitor should be used to support the current sources.

A voltage of 10mV is applied to the fused poly resistor. From the current measured through the resistor the resistance is calculated.

Note 47 **Idsat of burned transistor**
Source and substrate are connected to ground, drain and gate are set to 3.3V. The current IDS_PF is measured at the drain.

Note 48 **Zener diode breakdown voltage**
The diode reverse voltage is swept until the diode reverse current reaches 50 µA (2 µA) at the breakdown voltage VZENER.

Note 49 **Zener diode reverse leakage**
The Zener diode reverse leakage current LZENER is measured at 1 V reverse bias voltage.

Note 50 **Zapped Zener diode voltage**
The Zener diode is zapped according to the zapping conditions specified in doc. 9991070. The reverse voltage VZAP of the zapped Zener diode is measured at 50 µA reverse current.

Note 51 **Temperature coefficient Zener diode breakdown voltage**
VZENER50 is measured as a function of temperature from 25°C to 125°C as described in note 48. TCVZENER50 is calculated from the slope of the following linear regression at T0=27°C:

$$VZENER50(T) = VZENER50(T0) + TCVZENER50*(T-T0)$$

Note 52 **RPOLYZ resistance variation** in percentage over temperature range (T=-40°C to +150°C) for geometries L=3 to 1000 @ W=0.8 to max. 48µm for a typical wafer.

Note 53 **Forward current**
The forward current of a diode (W=0.4 um L=12 um) is measured under forward bias voltage at 0.3V.

Note 54 **Junction capacitances**
The junction capacitances C of diodes with different area are measured as a function of the reverse bias voltage V. The junction capacitance per drawn area CJ, the junction potential PB, and the area junction grading coefficient MJ are then extracted from:

$$C = \frac{W \cdot L \cdot CJ}{\left(1 + \frac{V}{PB}\right)^{MJ}}$$

Note 55 **Diode reverse voltage**
The diode reverse voltage is swept until the diode reverse current reaches 20 uA at the voltage RV. The RV values are valid for the geometry (W=0.4 um L=12 um) at T0 = 27°C.

Note 56 **Diode breakdown voltage**
The diode reverse voltage is swept until the diode reverse current reaches 10nA/um^2 at the breakdown voltage BV. The BV values are valid for T0 = 27°C.
Note: The well to substrate breakdown is dominated by the diffusion to substrate breakdown if the well enclosure of the diffusion is not sufficient.

Note 57 **Diode leakage**
The leakage current of a schottky diode (W=0.4 um L=12 um) is measured under reverse bias voltage at -3V.

The leakage current of the NWELL to substrate diode (NW Area=739 um$^{2)}$ is measured under reverse bias voltage at -20V.

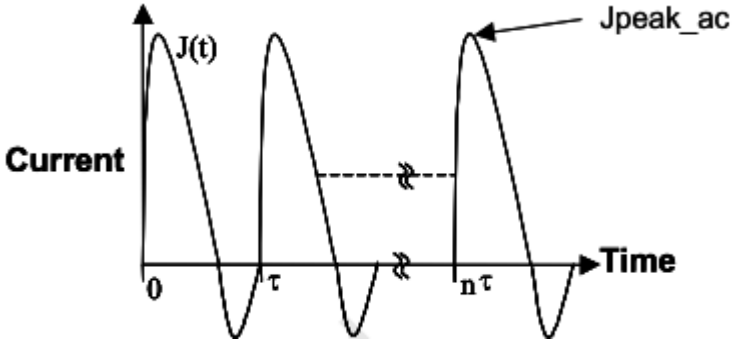
Note 58 **Junction current temperature exponent coefficient**
The temperature exponent coefficient XTI of the saturation current is determined using the following expressions:

$$JS(T) = JS(T_0) \cdot \exp\left[\frac{qE_{G0}}{kT_0} - \frac{qE_G}{kT} + XTI \cdot \ln\left(\frac{T}{T_0}\right)\right]$$

where T0=300K, EG0=1.16-((7.02e-4•T02)/(T0+1108)) and EG=1.16-((7.02e-4•T2)/(T+1108))

3.15 Notes / Reliability Informations

Note Q1 **Current Density AC operation guideline** (this guideline is not applicable to flip package)



$$J_{rms} = \left\{ \int_0^t J(t)^2 \frac{dt}{T} \right\}^{\frac{1}{2}}$$

$$J_{av} = \int_0^t J(t) \quad \frac{dt}{T}$$

Where J(t) is the current density flowing through a metal line.

J_{av} is AVERAGE current density through a metal line. The numbers given below are for 10% resistance increase after 10-year continuous operation at 110°C.

Jav ≤ 1.0mA/um (= 1.49 x 10^5 A/cm2) for M1,

Jav ≤ 1.0mA/um (= 1.56 x 10^5 A/cm2) for M2 to M3,

Jav ≤ 1.6mA/um (= 1.73 x 10^5 A/cm2) for top metal (M3 or M4)

Jav ≤ 5.0mA/um (= 1.73 x 10^5 A/cm2) for thick metal (MT)

It is nominal AlCu thickness instead of genuine total thickness.

J_{rms} is root-mean-square current density through a metal line. The numbers given below are for <10°C Joule heating

J_{rms} ≤ 8ma/um (= 1.2 x 10^6 A/cm^2) for M1,

J_{rms} ≤ 4ma/um (= 0.62 x 10^6 A/cm^2) for M2 to M3,

J_{rms} ≤ 8ma/um (= 0.97 x 10^6 A/cm^2) for top metal (M3, M4 or MT)

J_{peak_ac} is the current density at which metal line will start MELTING due to excessive Joule heating. Design should stay away from J_{peak_ac} as far as possible. J_{peak_ac} can be calculated as follows:

J_{peak_ac} = 2x10^6 /sqrt(Duty cycle), in A/cm^2 for M1 to M4

Duty cycle is the ratio of pulse width of J_{peak_ac} to period. For convenience, one could measure the pulse width of J_{peak_ac} at half of the peak.

Example:

If pulse width is 1ns and period is 10ns, dutycycle is 0.1 or 10%. Square root of 0.1 is 0.31.

J_{peak_ac} = $2x10^6$ /0.31 = $6.45x10^6$ A/cm^2

No J_{rms} and J_{peak} are given for contact and via because Joule heating mainly comes from metal line, and metal line starts melting earlier than via in this technology.

Note: If space permits, it is preferable to have more contacts or vias than required by EM rules. This will reduce interconnect resistance and also improve reliability. Avoid using only one contact or via in one metal line unless it is absolutely necessary and allowed by the rules.

4 Support

For questions on process parameters please refer to:

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