C035M-D
DESIGN RULE MANUAL

Owner : Technology Engineering CMOS

Location : N.A.

REVISION STATUS SUMMARY

Revision	Requestor	Date	Request Number	Pages	Description
01	JDG	10-12-1997	17822	01-138	New document
02	JDG	01-02-1999	19875	01-121	Adjust layer numbers for nwell, nlddprotect, nplusprotect Remove MM9 model files
03	AL	15-12-1999	21688	01-120	Introduction ring bond-pads, inclusion new layer table, guidelines for dummy metal/metdis, addition of new data

TABLE OF CONTENTS

1 CHANGES

1.1 Changes from revision 2 to revision 3.

- Modification of layer table
- Further guidelines for dummy metal and metdis layer
- Increase of maximum metal width without need for holes (all metal layers from 25µm to 30µm)
- Introduction of ring bond-pads
- Physical and electrical parameters
  - modifiction of metal 1 thickness
  - sheet resistance no given for n+ polycide on field
  - correction of error in glue layer thicknesses M2,3,4,5
  - removal of min/max dielectric thicknesses
  - temperatures coefficients added for transistors and resistors
  - new data for diode leakage current

2 PURPOSE

This Layout Rule Specification provides the layout rules and electrical parameters for the design and layout of integrated circuits using the Alcatel Microelectronics C035M-D technology.

C035M-D, is a 0.35 µm single level poly, five layer metal, twin-well CMOS process using a <100> p/p+ epitaxial substrate. It features salicided source and drains and polysilicon, and resistors on unsalicided active area and unsalicided polysilicon.

The technology is developed for the design of digital circuits operating at a power supply voltage of 3.3 volt (+0.3/-0.6 volt).

3 SCOPE

This document applies to Design Engineers, Technology Engineers, CAD Engineers, Process Engineers, Quality Assurance Engineers, Reliability Engineers and Product Engineers.

It is the prime reference to be applied for the design and layout of any digital CMOS 0.35 µm product to be fabricated in the Alcatel Microelectronics production line. For additional information relating to analogue design, see also document DS13337.

Updates of this document are possible. It is the user's responsability to consult the Alcatel Microelectronics document control centre on the availability of updated revisions of this specification.

4 REFERENCE DOCUMENTS

DS 13600: Assembly Layout Rules

DS 13337: C035M Design Rule Manual Supplement for Analogue Option (C035M-A)

DS 13336: SPICE models C035

5 MASK IDENTIFICATION

5.1 Introduction

The Alcatel Microelectronics 0.35 µm CMOS technology family consists of a core digital technology C035M-D and a mixed-signal technology C035M-A; C035M-A is built on C035M-D with the addition of two specific options: high precision double polysilicon capacitors and high ohmic polysilicon resistors. Refer to the Alcatel Microelectronics C035M-A Design Rule Manual for analogue specific layout rules and electrical parameters.
In case further derived application-specific technologies are made available in the future, the related layout rules and electrical parameters will be added to this specification.

The C035M technology family is designed for 3.3 volt (+ 0.3/-0.6 volt) power supply operation and features salicided junctions and polysilicon, and unsalicided resistors and I/O transistors.

The metallization processes offer 5 layers of metal interconnect.

5.2 Characterized Devices for Circuit Design

Hereafter, the list of characterized devices available for circuit design is given. Several classes of devices can be defined. Other devices than those specified are not allowed.

5.2.1 Fully Characterized Devices

For this first class of devices, room temperature characterization, temperature sensistivity, voltage sensitivity, matching, statistical behavior, description in terms of DRC, extraction of layout, symbol, SPICE modelling are available. These devices can be used for any kind of application.

5.2.1.1 NMOS transistor
PMOS transistor

5.2.1.2 Unsalicided N^+ polysilicon resistor
Unsalicided P^+ polysilicon resistor
Unsalicided N^+ active resistor
Salicided N^+ polysilicon resistor
Nwell resistor

5.2.1.3 Salicided N^+/p-substrate junction diode
Salicided P^+/nwell junction diode

5.2.2 Devices available for specific applications

This second class of devices is available only for a restricted kind of applications. The characterization of these devices is limited to the strict minimum for use in the targeted application.

5.2.2.1 P^+/nwell/p-substrate (vertical pnp) bipolar transistor
Application: Bandgap voltage reference

5.2.2.2 NMOS transistor with unsalicided source, drain and gate
PMOS transistor with unsalicided source, drain and gate
Application: I/O transistors

5.2.2.3 NMOS transistor without LDD implant
Application: clamping device for ESD protection

5.2.2.4 P^+/NLDD diode
Application: ESD protection

5.2.3 Natural Devices

This third class includes "naturally built-in devices". Any characterization performed on these devices is for process control purposes only. The support of these devices is not guaranteed.

5.2.3.1 Unsalicided P^+ active resistor

5.2.3.2 Salicided P+ polysilicon resistor
Salicided N^+ active resistor
Salicided P^+ active resistor

5.2.3.3 Nwell/p-substrate junction diode

5.3 Process Flow

5.3.1 Key Features

POLY BUFFERED LOCOS (PBL): PBL is used for active area isolation to reduce active area pitch. Typical bird's beak encroachment for PBL is < 0.15 µm; conventional LOCOS typically yields an encroachment of 0.4 µm.

RETROGRADE WELLS have lower lateral well diffusion which allows smaller N^+/P^+ spacing across the well border with enhanced latch-up behaviour as compared to conventionally diffused wells. Lower well sheet resistances can be achieved and an additional advantage is the good control of parasitic field transistors.

N^+/P^+ POLY GATE: N^+ poly gate is used for NMOS transistors, P^+ poly gate is used for PMOS transistors. This allows symmetrical design of the active devices. For PMOS transistors, compared to N^+ poly gate, P^+ poly gate improves short channel behaviour and sensitivity to hot carrier degradation.

SALICIDE: the salicide technology provides low gate and source/drain series resistance. The salicide is needed to short N^+ poly and P^+ poly. Circuit packing density can be increased because the salicide allows abutting straps with only one contact.

SALICIDE PROTECTION: this features allows to prevent salicide formation over I/O transistors for improved ESD performance. It is also used to obtain unsalicided resistors in active area and/or polysilicon.

PLANARIZED DIELECTRICS: for enhanced step coverage of metal lines and lithography performance (depth-of-focus). CHEMICAL MECHANICAL POLISHING (CMP) is used to achieve the required level of planarization.

TUNGSTEN PLUGS: contacts and vias are filled with tungsten; This results in enhanced step coverage of the metal lines in the contacts and vias. This technology feature allows random placement of contacts and vias, without proximity rules. Full stacking of contacts and vias is allowed.

5.3.2 Simplified Process Flow

This section gives a brief summary of the process flow for the C035M-D technology.

- Active Area
  - oxide, polysilicon, nitride stack deposition
  - active area patterning
  - field oxidation
  - sacrificial oxidation

- N-well and PMOS channel doping
  - n-well patterning
  - retrograde n-well implant
  - PMOS V_t & anti-punch through implant
  - annealing

- P-well and NMOS channel doping
  - p-well patterning
  - retrograde p-well implant
  - NMOS V_t & anti-punch through implant

- Gate
  - wet etch sacrificial oxide
  - gate oxidation
  - polysilicon deposition and doping
  - polysilicon patterning
  - polysilicon oxidation

- Lightly Doped Drain's (LDD)
  - NMOS LDD mask & implant
  - PMOS LDD mask & implant
  - oxide sidewall spacer deposition
  - oxide sidewall spacer etch

- Source & Drain
  - pre-implant oxide
  - N^+ source/drain mask & implant
  - P^+ source/drain mask & implant
  - junction annealing

- Salicide
  - salicide protect nitride deposition
  - salicide protect patterning
  - Titanium deposition
  - Titanium salicide formation

- selective etch
- salicide anneal

- Inter-Level Dielectric (ILD)
  - oxide deposition
  - doped oxide deposition
  - planarisation
  - oxide deposition and densification

- Contacts & metal 1
  - contact window patterning
  - glue layer deposition
  - tungsten plug formation
  - metal 1 deposition
  - metal 1 patterning

- Inter-Metal Dielectric (IMD1)
  - oxide deposition
  - CMP planarisation

- Via 1 & metal 2
  - via 1 patterning
  - glue layer deposition
  - tungsten plug formation
  - metal 2 deposition
  - metal 2 patterning

- Inter-Metal Dielectric (IMD2)
  - oxide deposition
  - CMP planarisation

- Via 2 & metal 3
  - via 2 patterning
  - glue layer deposition
  - tungsten plug formation
  - metal 3 deposition
  - metal 3 patterning

- Inter-Metal Dielectric (IMD3)
  - oxide deposition
  - CMP planarisation

- Via 3 & metal 4
  - via 3 patterning
  - glue layer deposition
  - tungsten plug formation

- metal 4 deposition
- metal 4 patterning

- Inter-Metal Dielectric (IMD4)
  - oxide deposition
  - CMP planarisation

- Via 4 & metal 5
  - via 4 patterning
  - glue layer deposition
  - tungsten plug formation
  - metal 5 deposition
  - metal 5 patterning

- Final passivation and annealing

5.4 General Requirements for IGS numbering

Data on an IGS layer might be elaborated on to generate a mask, or several IGS layers might be used to generate one mask. In order to distinguish between data on an IGS layer and data on a mask, in this specification the name of an IGS layer is expressed with small letters (e.g. active), while the name of the corresponding mask (if any) is put in capitals (e.g. ACTIVE).

Alcatel Microelectronics will only accept layout databases meeting the requirements listed hereafter:

5.4.1 Layout data must be present on the correct IGS layers as given in the next section.

5.4.2 Layout data present on other IGS layers than those indicated in this specification will be ignored during mask preparation. An overview of the allowed IGS layers is given below. Besides IGS layers containing drawn and/or automatically generated (see section 5.4.3.) layout data, various special-purpose IGS layers might be used as given in section 5.6.

5.4.3 Generally, a number of IGS layers are not "drawn" (i.e. during layout), but automatically "generated" from one or more other layers. No layout data must be present on the IGS layers which are generated automatically, unless they are covered by IGS layer 61 (no_gen). IGS layer 61 (no_gen) disables ALL automatic data generations, meaning that all data on the area covered by layer 61 is used as drawn. All data, present on automatically generated IGS layers and which are not covered by IGS layer 61 will be ignored during mask preparation. Use of nogen is not permitted except in consultation with the Technology Department at Alcatel Microelectronics.

The following IGS layers are automatically generated out of drawn IGS layers:

Output IGS layer	Output Name	Input IGS-layer(s)
08	pwell	01, 08, 112, 61
16	nplus	02, 16, 17, 66, 61
14	nldd	02, 14, 17, 38, 61

5.4.4 In principle, non-layout data such as CD structures, layer identifications and/or revision numbers, logo's, teststructures etc., must not introduce any layout rule violations. When layout rule violations cannot be avoided, the customer shall always notify Alcatel Microelectronics prior to tape delivery, giving details of the cell names of the structures not complying with this layout rule specification.

5.4.5 Layout data must be datatype 0 (NORMAL LAYOUT) or datatype 30 (special purpose layout). All other datatypes are for CAD purposes only and will be ignored during mask generation/preparation. The table given in section 5.6 gives the full list of CAD layers with their corresponding datatype.

5.5 Layout data IGS numbering and mask identification

The table hereafter gives the list of IGS layers which will contain data that will be translated into processing masks. The full C035M layerstable, including special purpose CAD layers is given in the next section.

IGS layer Number	IGS layer Name	Mask Number	Drawn ?	Notes	Mask Name
02	active	20	yes	-	ACTIVE
01	nwell	10	yes	(1)	N-WELL
112	rnwell	-	yes	-	-
08	pwell	15	no	(2)	P-WELL
13	poly	90	yes	-	POLY
14	nldd	100	no	(3)	NLDD
16	nplus	110	no	(4)	N^+ IMPLANT
17	pplus	120	yes	-	P^+ IMPLANT
38	nlddprot	-	yes	(5)	-
66	nplusprot	-	yes	(6)	-
18	sal_prot	125	yes	-	SALPROTECT
19	contact	130	yes	-	CONTACT
23	metal_1	140	yes	-	METAL 1
25	via_1	150	yes	-	VIA 1
27	metal_2	160	yes	-	METAL 2
32	via_2	180	yes	-	VIA 2
34	metal_3	190	yes	-	METAL 3
35	via_3	210	yes	-	VIA 3
36	metal_4	220	yes	-	METAL 4
52	via_4	240	yes	-	VIA 4
53	metal_5	250	yes	-	METAL 5
31	nitride	170	yes	-	PASSIVATION
15	dractext	-	yes	(7)	-

Notes:

(1) Final nwell data are generated from drawn IGS layer 1 data (drawn nwell data) and IGS layer 112 (nwell resistors) data.

NWELL mask data = drawn nwell + drawn rnwell

(2) Pwell data are generated from final nwell data. Pwell reticle field tone is opposite to nwell.

PWELL mask data = nwell mask data
= drawn nwell + drawn rnwell

(3) NLDD mask is needed only if LDD removal in the I/O's is requested; in other cases, N^+ IMPLANT mask is used. If used, the NLDD mask data are generated from drawn IGS layer 17 data (drawn pplus data) and IGS layer 38 (drawn nlddprot data)

NLDD mask data = drawn pplus + drawn nlddprot

(4) N^+ IMPLANT mask data is generated from drawn IGS layer 17 data (drawn pplus data) and IGS layer 66 (drawn nplusprot data).

N^+ IMPLANT mask data = drawn pplus + drawn nplusprot

(5) IGS layer 38 (nlddprot) is used to exclude the NLDD implant from NMOS transistors, used as clamping devices for ESD protection.

(6) IGS layer 66 (nplusprot) is used to exclude the N^+ IMPLANT on n-type active areas; it is used for defining the P^+/NLDD clamping diode for ESD protection.

(7) To allow use of Alcatel Microelectronics' bonding diagram editor, all bonding pads must be labeled using IGS layer 15, "dractext". Labels must have a unique name per pad (e.g. all VDD pads must have a different name, i.e. VDD1, VDD2, ...). Bonding labels must have their origin within the layer passivation.

5.6 C035M layers table

The following gives a full listing of the streamout layers used for the various process options in C035M: digital and analogue.

digital drawing layers for cmos035

nwell	drawing		1	0
active	drawing		2	0
poly	drawing		13	0
pplus	drawing		17	0
siprot[1]	drawing	18	0	
contact	drawing	19	0	
metal1	drawing	23	0	
v1	drawing		25	0
metal2	drawing	27	0	
v2	drawing	32	0	
metal3	drawing	34	0	
v3	drawing	35	0	
metal4	drawing	36	0	
v4	drawing	52	0	
metal5	drawing	53	0	
nitride	drawing	31	0	
rnwell	drawing	112	0	
mexclude	drawing	62	4	
y9	drawing	0	63	
noring	drawing	51	0	
metdis	drawing	63	0	
nlddprot	drawing	38	0	
nplusprot	drawing	66	0	
metal1	positivePS	23	1	
metal1	negativePS	23	2	
metal2	positivePS	27	1	
metal2	negativePS	27	2	
metal3	positivePS	34	1	
metal3	negativePS	34	2	
metal4	positivePS	36	1	
metal4	negativePS	36	2	
metal5	positivePS	53	1	
metal5	negativePS	53	2	

analog drawing layers for cmos035

poly2	drawing	11	0
capa	drawing	12	0
hipo	drawing	26	0

digital drawing layers for cmos035 (AME specific)

dractxt	drawing	15	0

digital drawing layers for cmos035 (Other)

[1] Also referred to as salprot

c4	drawing	39	0

digital mask making layers for cmos035 (do NOT draw)

pwell	drawing	8	0
nldd	drawing	14	0
nplus	drawing	16	0
nogen	drawing	61	0

CAD layers for cmos035 (Other)

nwell	hd	1	30
active	hd	2	30
poly	hd	13	30
pplus	hd	17	30
siprot	hd	18	30
contact	hd	19	30
metal1	hd	23	30
v1	hd	25	30
metal2	hd	27	30
v2	hd	32	30
metal3	hd	34	30
v3	hd	35	30
metal4	hd	36	30
v4	hd	52	30
metal5	hd	53	30
mcapa	drawing	3	0
mdiode	drawing	4	0
mnpn	drawing	5	0
mpnp	drawing	6	0
mres	drawing	7	0
msub	drawing	9	0
nogate	drawing	10	0
nondrc	drawing	62	47
mfuse	drawing	62	48
mio	drawing	62	56
mshield	drawing	62	49
mfgpp	drawing	46	0
poly	markerR	13	17
metal1	markerR	23	17
metal2	markerR	27	17
metal3	markerR	34	17
metal4	markerR	36	17
metal5	markerR	53	17

CAD texting layers for cmos035 (Other)

text	drawing	0	0
poly	pintext	13	21
metal1	lpetext	23	22
metal1	pintext	23	21
metal1	flatext	23	20
metal2	lpetext	27	22
metal2	pintext	27	21
metal2	flatext	27	20
metal3	lpetext	34	22

metal3	pintext	34	21
metal3	flatext	34	20
metal4	lpetext	36	22
metal4	pintext	36	21
metal4	flatext	36	20
metal5	lpetext	53	22
metal5	pintext	53	21
metal5	flatext	53	20

CAD P&R layers for cmos035

prBoundary	drawing	60	0
flatext	drawing	60	20
lpetext	drawing	60	21
pintext	drawing	60	22
metal1	boundary	37	0
metal2	boundary	40	0
metal3	boundary	41	0
metal4	boundary	54	0
metal5	boundary	55	0
v1	boundary	56	0
v2	boundary	57	0
v3	boundary	58	0
v4	boundary	59	0
metal1	pin	23	10
metal2	pin	27	10
metal3	pin	34	10
metal4	pin	36	10
metal5	pin	53	10

CAD layers for cmos035 (AME specific)

notusedlayers	drawing	70	0
dracula	drawing	45	0
stext	drawing	116	0

5.7 Dummy Metal Procedure

- As a standard procedure for the C035M technology, dummy metal will be generated on all 5 metal layers. This is done in order to guarantee high manufacturability (yield) by ensuring that overall metal coverage on the wafer is within specified limits.
- The presence of dummy metal can have an impact on circuit performance and therefore IGS layer 63 (metdis) allows the designer to define product areas where dummy metal generation is excluded. Typical examples of such areas are sensitive analogue structures such as matched structures, sensors, inductors (see also Design Rule Manual Supplement for Analogue Option C035M-A, DS13337). It is the designer's responsibility to draw metdis on these areas.
- In order to obtain optimised processing, it is necessary that the overall metal density be in the range 25 - 70% for each of the metal layers. If

this is not the case, lower yields will be obtained. For this reason, the size of metdis features should be limited. In case problems with metal coverage are expected, a warning may be given to the customer.

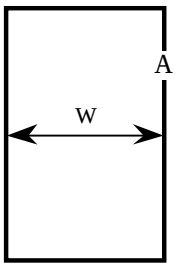
Notwithstanding the above, the possibility exists to process prototypes of a design without any dummy metal. This should be indicated in the Product Database.

6 TERMS AND DEFINITIONS

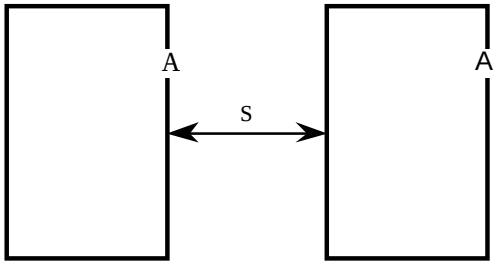
6.1 Convention for specifying layout rules

The following conventions are used to specify the layout rules in this specification:

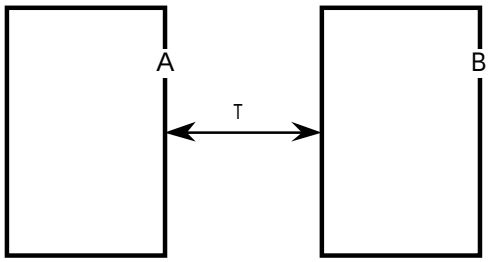
6.1.1 Level A width "W" is defined as:



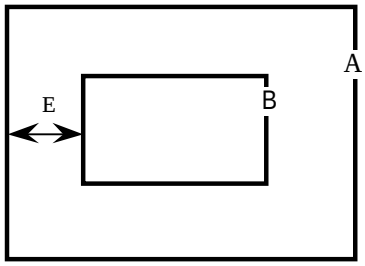
6.1.2 Level A spacing "S" is defined as:



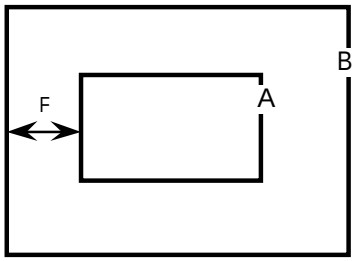
6.1.3 Level A spacing "T" to level B is defined as:



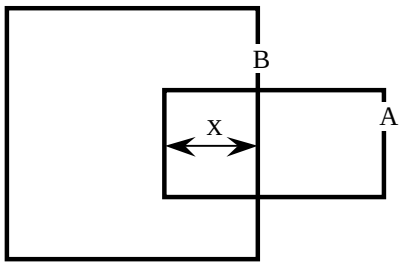
6.1.4 Level A enclosure "E" of level B is defined as:



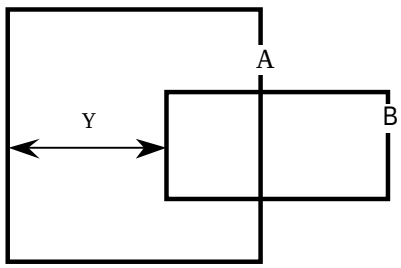
6.1.5 Level A enclosure "F" by level B is defined as:



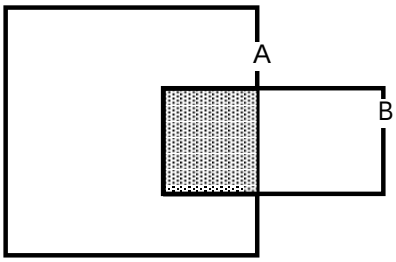
6.1.6 Level A intersection "X" with level B is defined as:



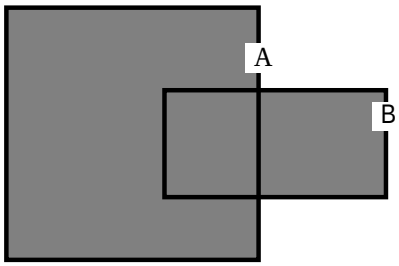
6.1.7 Level A extension "Y" on level B geometry is defined as:



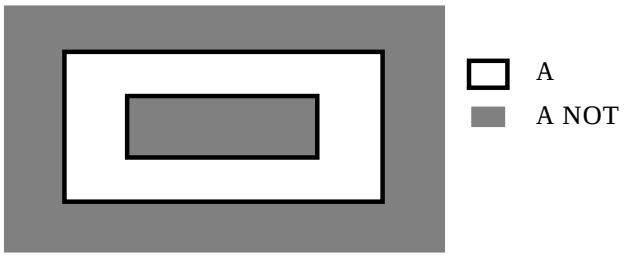
6.1.8 Level A "AND" level B is defined as the area common to both:



6.1.9 Level A "OR" level B is defined as the union of both geometries:



6.1.10 Level "A NOT" is defined as the complement of level A:



6.2 Logical description of derived geometries

This section describes the geometries of the CMOS 0.35 µm processes as a logical operation between the drawn layers:

nwell	=	nwell
pwell	=	.NOT. nwell
active area	=	active
polysilicon	=	poly
n^+ source/drain	=	active .AND. (.NOT. pplus) .AND. pwell .AND. (.NOT. poly)
p^+ source/drain	=	active .AND. pplus .AND. nwell .AND. (.NOT. poly)
source/drain	=	n^+ source/drain .OR. p^+ source/drain
nwell strap	=	active .AND. (.NOT. pplus) .AND. nwell
pwell strap	=	active .AND. pplus .AND. pwell
substrate strap	=	pwell strap
strap	=	nwell strap .OR. pwell strap
gate area	=	active .AND. poly
n-channel gate	=	active .AND. (.NOT. pplus) .AND. pwell .AND. poly
p-channel gate	=	active .AND. pplus .AND. nwell .AND. poly
active gate	=	n-channel gate .OR. p-channel gate
n^+ active area	=	active .AND. (.NOT. pplus)
	=	n^+ source/drain .OR. n-channel gate .OR. nwell strap
p^+ active area	=	active .AND. pplus
	=	p^+ source/drain .OR. p-channel gate .OR. pwell strap
field	=	.NOT. active
nmos field	=	field .AND. pwell
pmos field	=	field .AND. nwell
endcap	=	poly extension of the transistor gate in the transistor width direction
poly interconnect	=	poly .AND. (.NOT. active gate)
n^+ poly resistor	=	poly interconnect .AND. sal_prot

p^+ poly resistor	=	poly interconnect .AND. pplus .AND. sal_prot
n^+ active resistor	=	active .AND. (.NOT. pplus) .AND. pwell .AND. sal_prot
p^+ active resistor	=	active .AND. pplus .AND. nwell .AND. sal_prot
bond pad via	=	via .CUTTING. passivation

7 LAYOUT RULES

7.1 Introduction

In this section, the process layout rules are presented.

7.1.1 All dimensions given below are dimensions as drawn on the Interactive Graphical System (IGS).

7.1.2 All dimensions are given in microns (µm), unless specified otherwise.

7.1.3 Each layout rule is identified by a code in the following format: "IGS layer.x" where IGS layer refers to the IGS layer and x is a number, e.g. 13.1 refers to the first layout rule applicable for IGS layer 13 which corresponds to the polysilicon mask.

7.1.4 The layout rules in this document are minimum dimensions only, except for contacts and vias; wherever possible, if chipsize is not significantly increased and/or circuit electrical performance is altered, the minimum dimensions should not be used.

7.1.5 Each layout will be subject to a DRC (Design Rule Check) prior to final tape preparation.

7.1.6 All drawings are for illustrative purposes only. They are not drawn to scale.

7.1.7 All dimensions given in the layout rules are FINAL-ON-WAFER dimensions. During reticle fabrication proper sizing is applied in order to ensure that final dimensions are the same as drawn.

7.1.7.1 ACTIVE

Active width is defined as the distance from bird's beak to bird's beak of the field oxide, after gate oxidation or polysilicon etch

7.1.7.2 N&P WELLS

The width is defined as the distance between metallurgical junctions, assuming that N-well and P-well are drawn complementary.

7.1.7.3 P^+

P^+ width is defined as the width of the resist opening at source/drain implant.

7.1.7.4 NLDDPROT

NLDDPROT width is defined as the width of the resist mask at the NLDD implant

7.1.7.5 POLY, METAL 1, METAL 2, METAL 3, METAL 4 and METAL 5

The width is defined as the interconnect width at mid-height, after resist removal

7.1.7.6 CONTACT, VIA 1, VIA 2, VIA 3, VIA 4

The width is defined as the contact or via hole dimension at mid-height after resist removal

7.1.7.7 PASSIVATION

The width is defined as the width of the resist opening after develop inspection.

7.1.8 This document has to be read in conjunction with Alcatel Microelectronics specification DS 13600 "Assembly Layout Rules", which contains additional rules which must be regarded as part of the total layout rule set. In case of discrepancy between this document and the quoted Assembly Layout Rules specification, the highest number must always be used.

7.2 General Layout Requirements

7.2.1 The standard layout grid size is 0.05 µm, and the spot size is 0.25 µm @ 5X. In order to allow the use of minimum rule 19.6 (minimum active area contact spacing to polysilicon gate = 0.375 µm), 0.025 µm grid is to be used for IGS layer 13 (poly) and IGS later 19 (contacts). These 2 layers are always fractured and ordered to maskshops with 0.125 µm spot size. The use of 0.025 µm layout design grid is restricted to those 2 layers. All edges of polygons must be on the grid.

7.2.2 The chip dimensions in X- and Y- directions, defined as the distance from the center of the scribe lane to the center of the adjacent scribe lane, must be a multiple of 10 µm to allow compatibility with test- and assembly requirements.

7.2.3 Apart from 0° and 90° layout, only 45° layout is allowed. This rule will be checked by the DRC deck.

7.2.4 Transistor length is measured from drain to source as defined by the polysilicon mask. Transistor width is equal to the width center line of the gate with one half the device channel length subtracted for each 90° bend.

7.2.5 Salicided resistor length is measured by counting the numbers of squares from contact edge to contact edge. Non-salicided resistor length is measured by counting the number of squares under IGS layer 18 (sal_prot). A 90° bend is counted as one half square.

7.3 Product Identification

7.3.1 Chip Name

7.3.1.1 Alcatel Microelectronics will assign a chip name to every device. This chip identification will be placed according to the rules specified hereafter.

7.3.1.2 The chip identification, or chip name, must always be present in the circuit. It must appear only once in the circuit.

7.3.1.3 The chip name must be written on the metal 1 layer only.

7.3.1.4 The chip name should be designed according to the layout rules; only 45° angles can be used.

7.3.1.5 An empty space of 150 µm x 25 µm must be preserved for the purpose of placing the chip name.

7.3.1.6 Other chip identifications are allowed, provided they do not introduce any layout rule violations; also, they should be present on the metal 1 layer only.

7.3.2 Alcatel Microelectronics logo

7.3.2.1 The Alcatel Microelectronics logo will always be present in the circuit, unless clearly forbidden. The Alcatel Microelectronics logo will be placed according to the rules specified hereafter.

7.3.2.2 The Alcatel Microelectronics logo shall preferably be placed near the chip name. It must appear only once in the circuit.

7.3.2.3 The Alcatel Microelectronics logo must be written on the metal 1 layer only.

7.3.2.4 An empty space of 100 µm x 50 µm must be preserved for the purpose of placing the Alcatel Microelectronics logo.

7.3.2.5 Other logos are allowed, provided they do not introduce any layout rule violations; also, they should be present on the metal 1 layer only.

7.3.3 Mask and Iteration Numbering

7.3.3.1 Every circuit must contain the correct mask numbering on each layer, including the automatically generated layers (e.g. pwell, nplus) but with the exception of the passivation layer (IGS layer 31). The mask number corresponds to the mask number defined in this document (e.g. mask number for the active area mask is 20).

7.3.3.2 On every layer, including the non-drawn layers (e.g. pwell, nplus) but with the exception of the passivation layer (IGS layer 31), the iteration number must be present. All layer iterations for a completely new design will be "A".

7.3.3.3 Mask numbers and iteration numbers must not be superimposed. They will be covered by the no_gen layer (IGS layer 61). They can be combined with the CD structures (see section 7.3.4.).

7.3.3.4 To ensure process compatibility the following rules apply for the letters:

- poly pad must be drawn under contact letters
- contact letters to be covered by metal 1
- metal i to be drawn under via i (for i = 1→ 4)
- via i to be covered by metal (i+ 1) (for i = 1→ 4)

All related enclosures to be 1.0 µm minimum

7.3.3.5 Layer- and iteration numberings shall not introduce any layout rule violations; only 45° angles are allowed.

7.3.4 CD structures

7.3.4.1 Every circuit must contain the CD structures on each layer, including the automatically generated layers (e.g. pwell, nplus) but with the exception of the passivation layer (IGS layer 31).

7.3.4.2 The CD structures must not be superimposed. They will be covered by the no_gen layer (IGS layer 61).

7.3.4.3 To ensure process compatibility the following rules apply for the CD structures:

- active pad must be drawn under contact CD bar
- contact CD bar to be covered by metal 1
- metal i to be drawn under via i (for i = 1→ 4)
- via i to be covered by metal (i+ 1) (for i = 1→ 4)

All related enclosures to be 1.0 µm minimum

7.3.4.4 CD structures shall not introduce any layout rule violations; only 45° angles are allowed.

7.4 I/O's

7.4.1 An n-well cannot be used as a cross-under for V_{dd} connections.

7.4.2 Resistors in I/O protection circuitry must not be used as cross-under. Minimum spacing to unrelated metal shall be 19 µm. The corners of bends of I/O protection resistors must be at 45° angles.

7.4.3 All I/O protection diodes must be hard-wired to the V_{dd} or V_{ss} pads through metal. Cross-unders or substrate contacts to these devices are not allowed.

7.5 Diagonal Layout Rules

The layout rules in this chapter are valid for layout of lines in X and Y directions, and 45 degree lines.

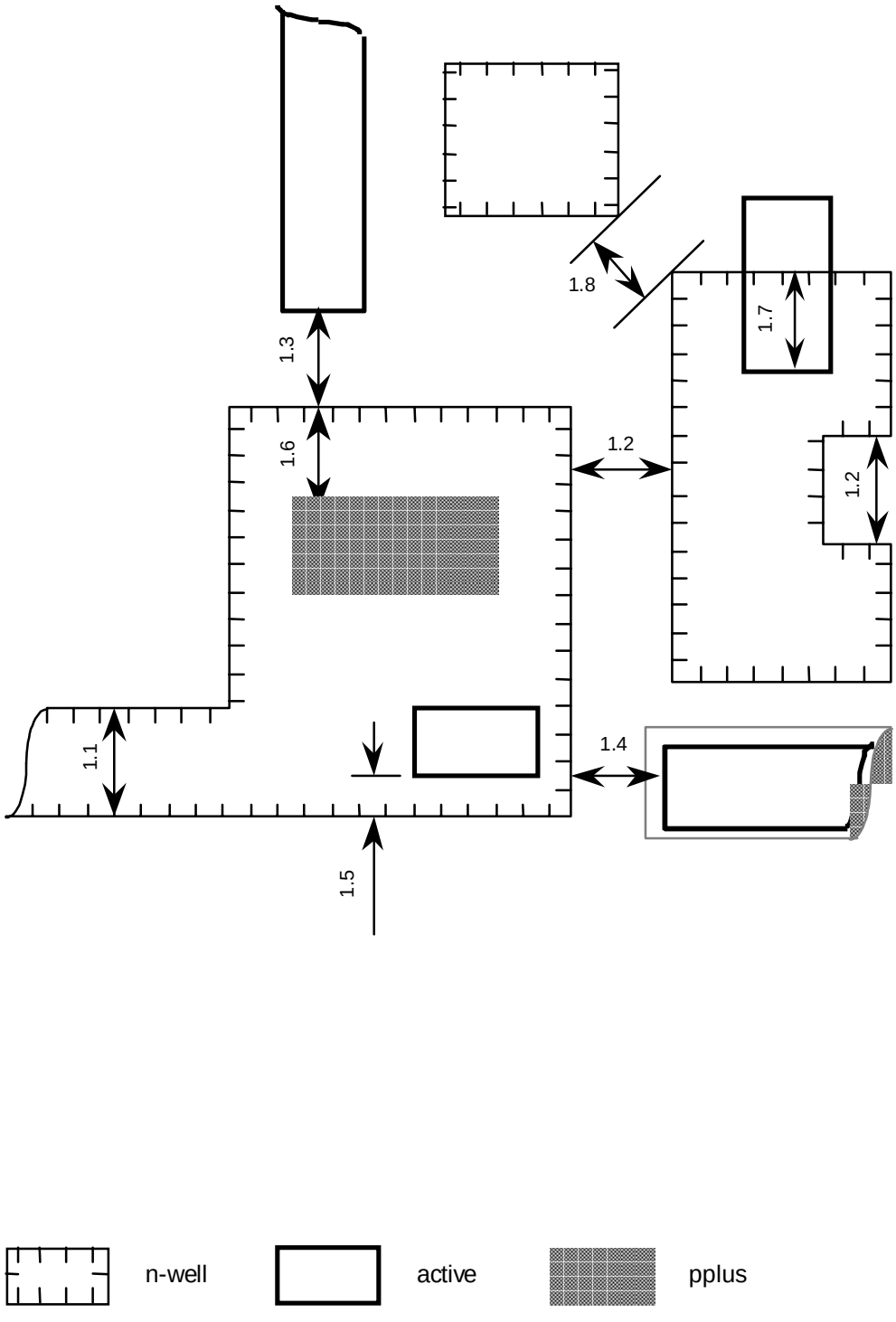
For layers with positive sizing such as e.g. active area, the way the sizing is done during final tape preparation may lead to a spacing on the mask smaller at 45 degrees than in X or Y direction. Specific layout rules apply for active area and n-well to prevent these small spacings at 45 degrees.

7.6 N-WELL (IGS layer 1)

Defines all n-well areas.

1.1.	Minimum n-well width	1.70
1.2.	Minimum n-well spacing - at different potential - at same potential (merge if less) - on same geometry	 2.10 1.40 1.40
1.3.	Minimum n-well spacing to n^+ active area	1.10
1.4.	Minimum n-well spacing to p-well strap	0.50
1.5.	Minimum n-well enclosure of n-well strap; n-well strap is allowed to cross n-well boundary	N/A
1.6.	Minimum n-well enclosure of p^+ active area	1.10
1.7.	Minimum n-well intersection with n-well strap if n-well strap crosses n-well boundary	0.70
1.8.	Minimum n-well spacing after 0.20 µm sizing (diagonal rule) - at different potential - at same potential (merge if less)	 1.70 1.00

N-WELL (IGS layer 1)



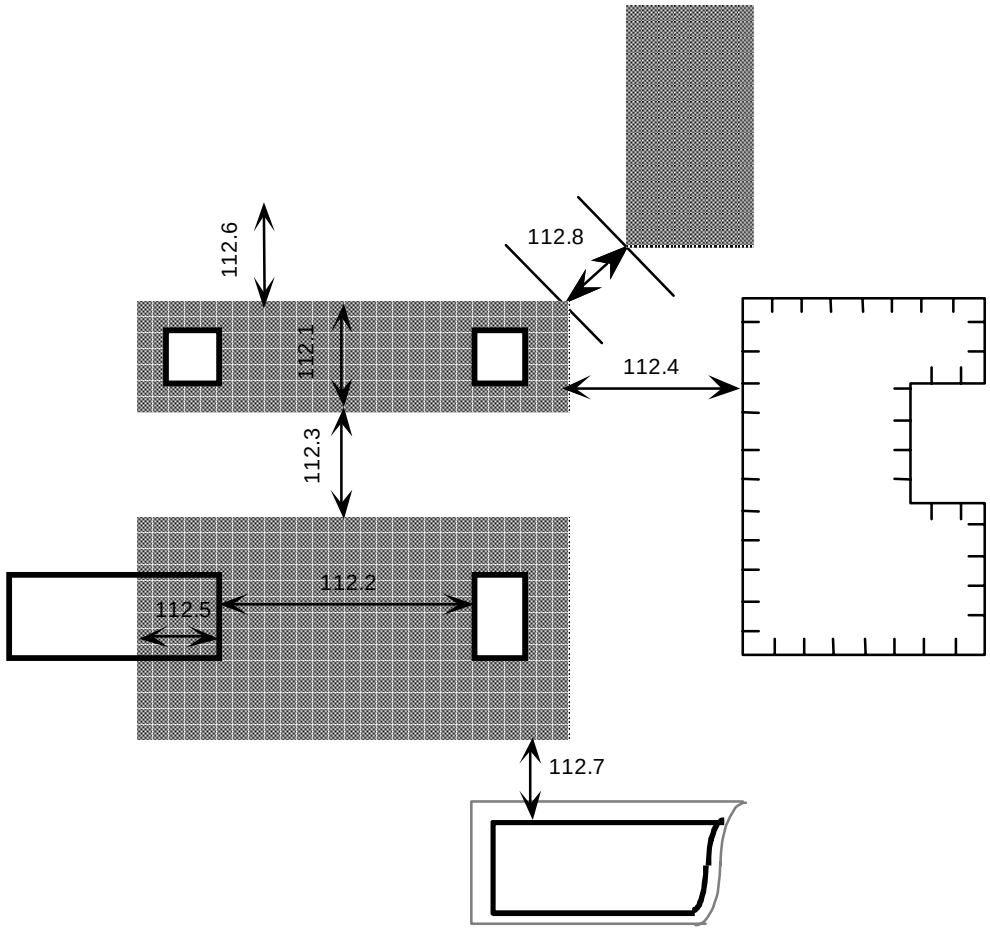
7.7 RNWELL (IGS layer 112)

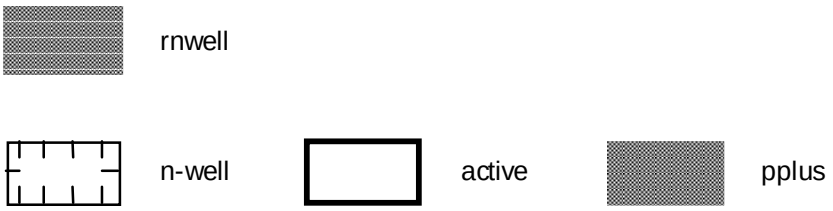
RNWELL is used to define n-well resistors. An n-well resistor is defined as n-well between two N^+ active areas. The width is defined as the n-well width; the length is defined as the space between the N^+ active areas.

Rules 112.1 and 112.2 give the minimum dimensions that are technologically feasible. These dimensions however do not guarantee proper characteristics in terms of linearity with respect to voltage.

112.1.	Minimum rnwell width	1.70
112.2.	Minimum rnwell length	1.00
112.3.	Minimum rnwell spacing	2.10
112.4.	Minimum rnwell spacing to n-well	2.10
112.5.	N^+ active across rnwell is allowed; minimum rnwell intersection with n^+ active if n^+ active crosses rnwell boundary	0.70
112.6.	Minimum rnwell spacing to n^+ active area	1.10
112.7.	Minimum rnwell spacing to p-well strap	0.50
112.8.	Minimum rnwell spacing after 0.20 µm sizing (diagonal rule)	1.70
112.9.	Minimum rnwell spacing to n-well after 0.20 µm sizing (diagonal rule)	1.70
112.10	P^+ active area in rnwell is not allowed	
112.11	Polysilicon in rnwell is not allowed	

RNWELL (IGS layer 112)





7.8 PWELL (IGS layer 8)

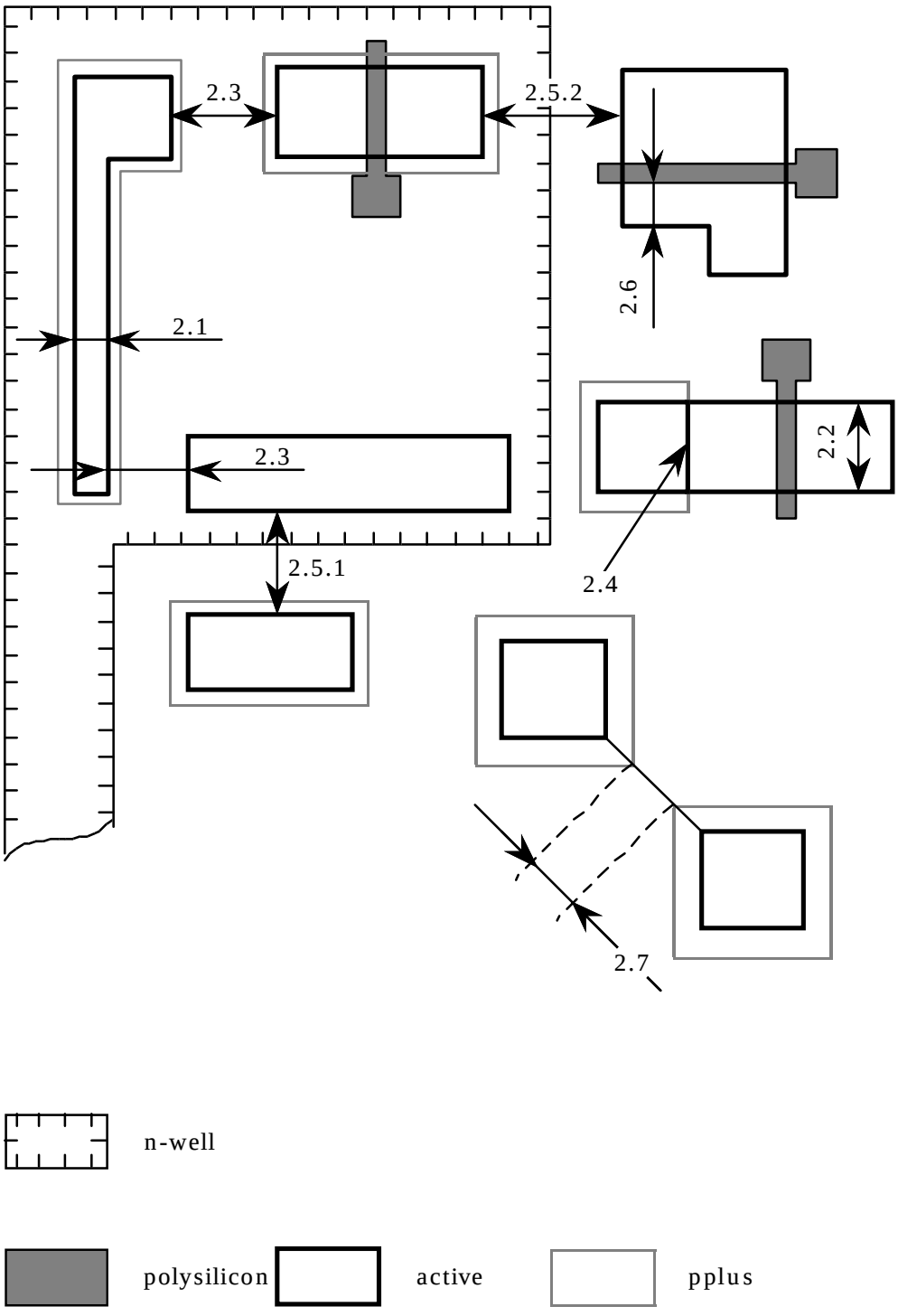
Defines all p-well implanted areas outside the n-wells. This layer must not be drawn. It is automatically generated from the drawn n-well data and drawn rnwell data.

7.9 ACTIVE AREA (IGS layer 2)

Defines all MOS source and drain areas, diffused areas for inter-connect, resistors and substrate- and n-well straps.

2.1.	Minimum active area width for interconnect, resistors and straps	0.40
2.2.	Minimum active area width for transistors	0.50
2.3.	Minimum active area spacing	0.70
2.4.	Abutting (touching) active areas are allowed if they are at the same potential	
2.5.	Minimum spacing between opposite type of active areas across the n-well border: - straps (also covered by rule 2.3) - transistors & diffusions (combined rule 1.3 + 1.6)	 0.70 2.20
2.6.	Minimum active area enclosure of polysilicon (source/drain length)	0.65
2.7.	Minimum active area spacing after sizing by 0.1 µm (to cover diagonal active area spacing)	0.50

ACTIVE AREA (IGS layer 2)

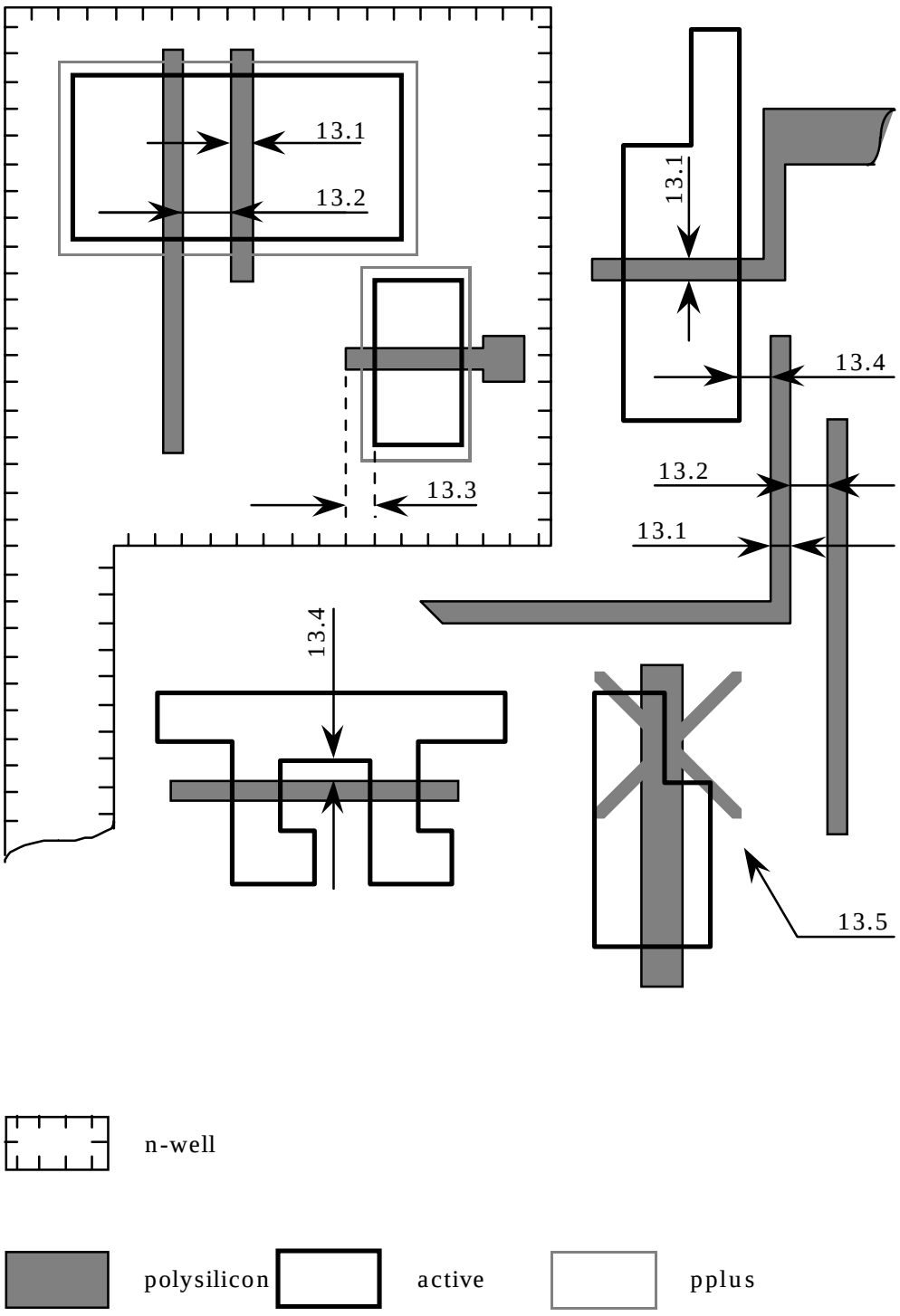


7.10 POLYSILICON (IGS layer 13)

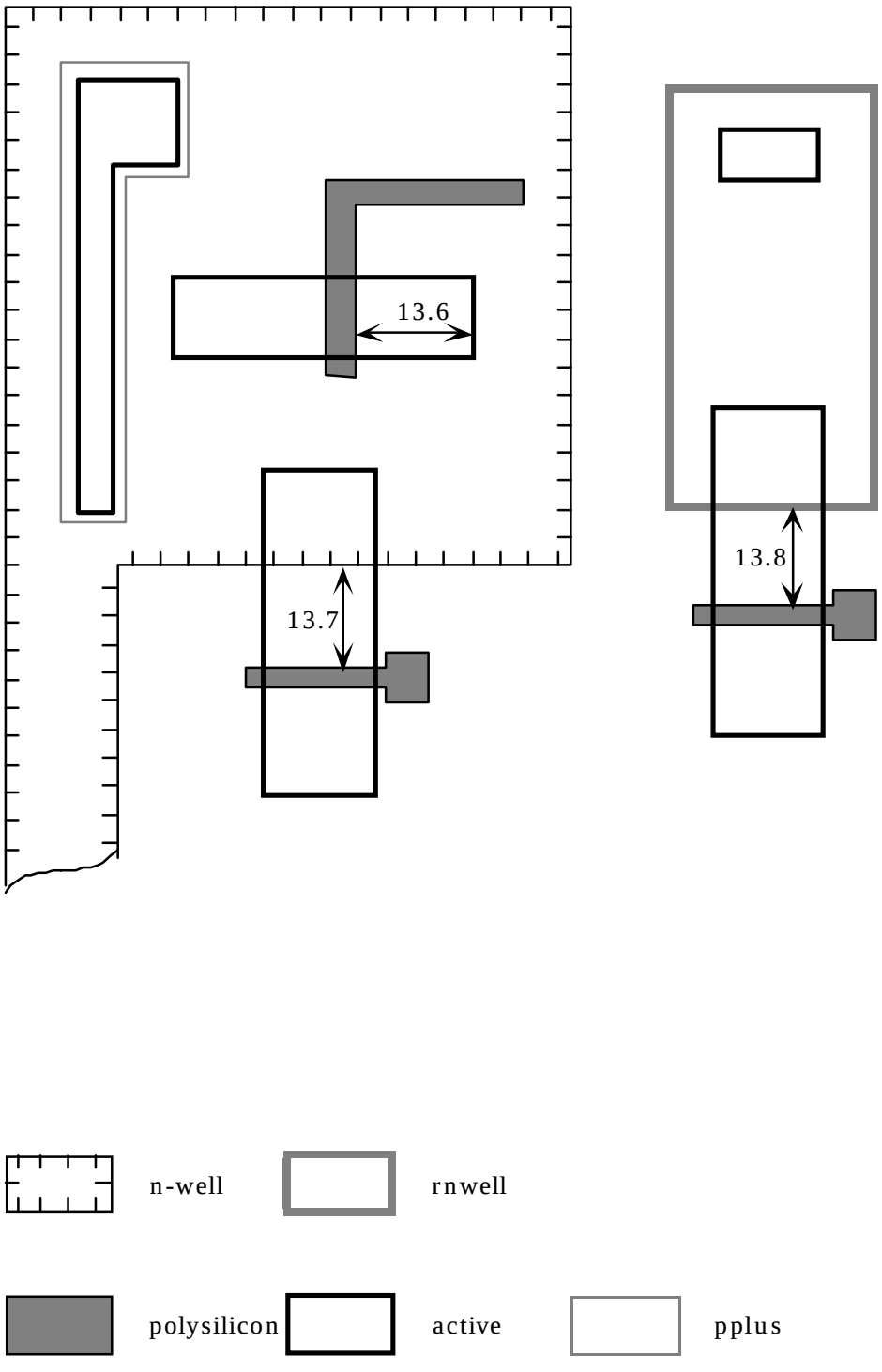
Defines the MOS gate areas and polysilicon interconnect.

13.1.	Minimum polysilicon width - interconnect - transistors	0.35
13.2.	Minimum polysilicon spacing - on field oxide - on thin oxide	0.55
13.3.	Minimum polysilicon extension beyond gate, on field oxide (= endcap)	0.40
13.4.	Minimum polysilicon spacing to active area	0.30
13.5.	Polysilicon gate running over active area corner is not allowed	
13.6.	Minimum polysilicon on active spacing to active edge of non drain/source active	0.40
13.7.	Minimum polysilicon spacing to n-well, on active, in case this active crosses the n-well boundary	1.00
13.8.	Minimum polysilicon spacing to rnwell, on active, in case this active crosses the rnwell boundary	1.00

POLYSILICON (IGS layer 13)



POLYSILICON (IGS layer 13, continued)

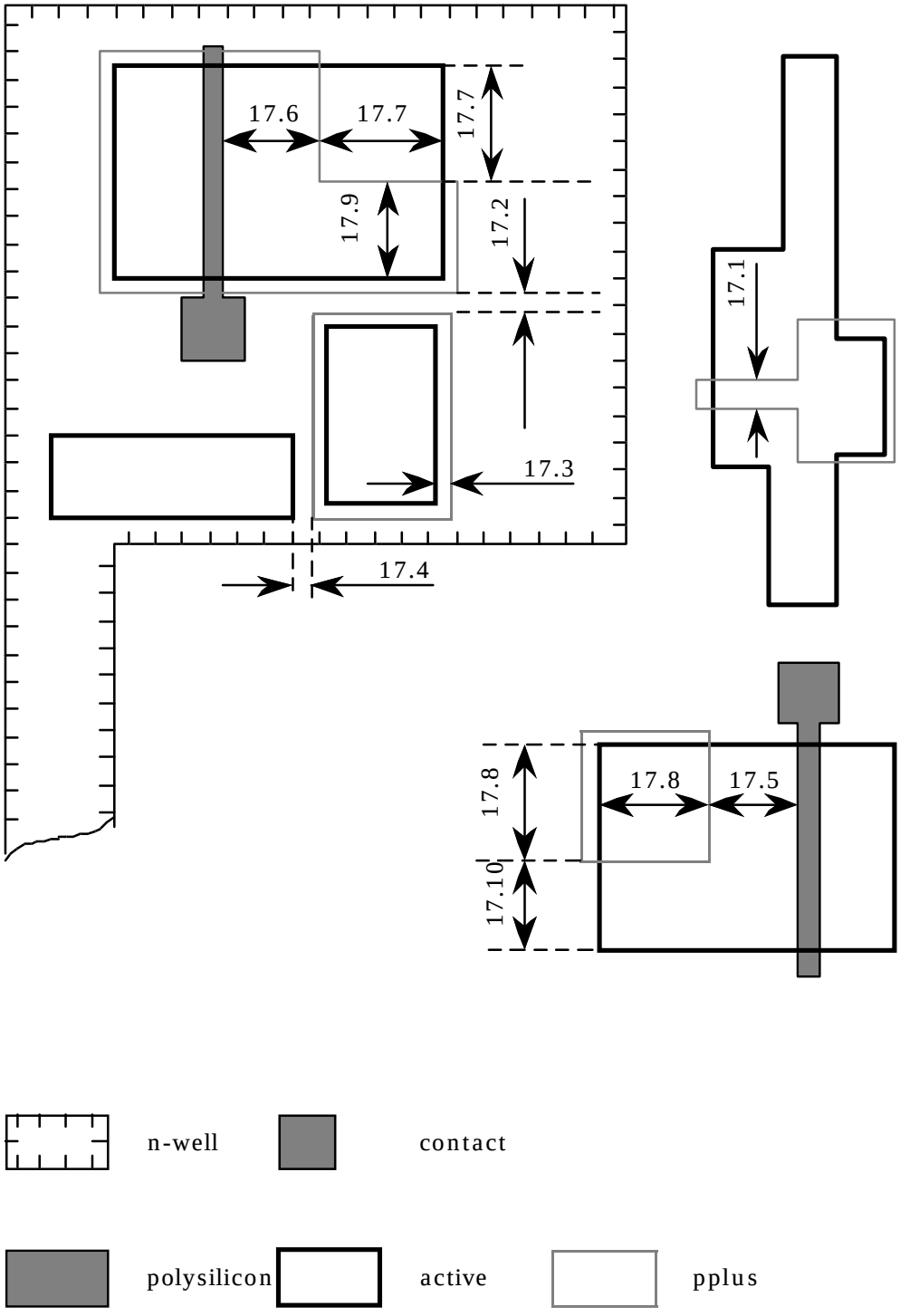


7.11 P+ IMPLANT (IGS layer 17)

Defines the areas to be implanted by p^+. It is used to define active areas to become p^+ source/drains, p-well straps, p^+ active resistors and/or interconnects and p^+ doped polysilicon resistors.

17.1.	Minimum pplus width	0.50
17.2.	Minimum pplus spacing	0.50
17.3.	Minimum pplus enclosure of p^+ active area	0.30
17.4.	Minimum pplus spacing to n^+ active area	0.30
17.5.	Minimum NMOS polysilicon gate spacing to p^+ active area of abutting p-well strap.	0.80
17.6.	Minimum PMOS polysilicon gate spacing to n^+ active area of abutting n-well strap.	0.80
17.7.	Minimum n^+ active area width of abutting n-well strap	0.50
17.8.	Minimum p^+ active area width of abutting p-well strap	0.50
17.9.	Minimum p^+ active area width	0.40
17.10.	Minimum n^+ active area width	0.40

P^+ IMPLANT (IGS layer 17)

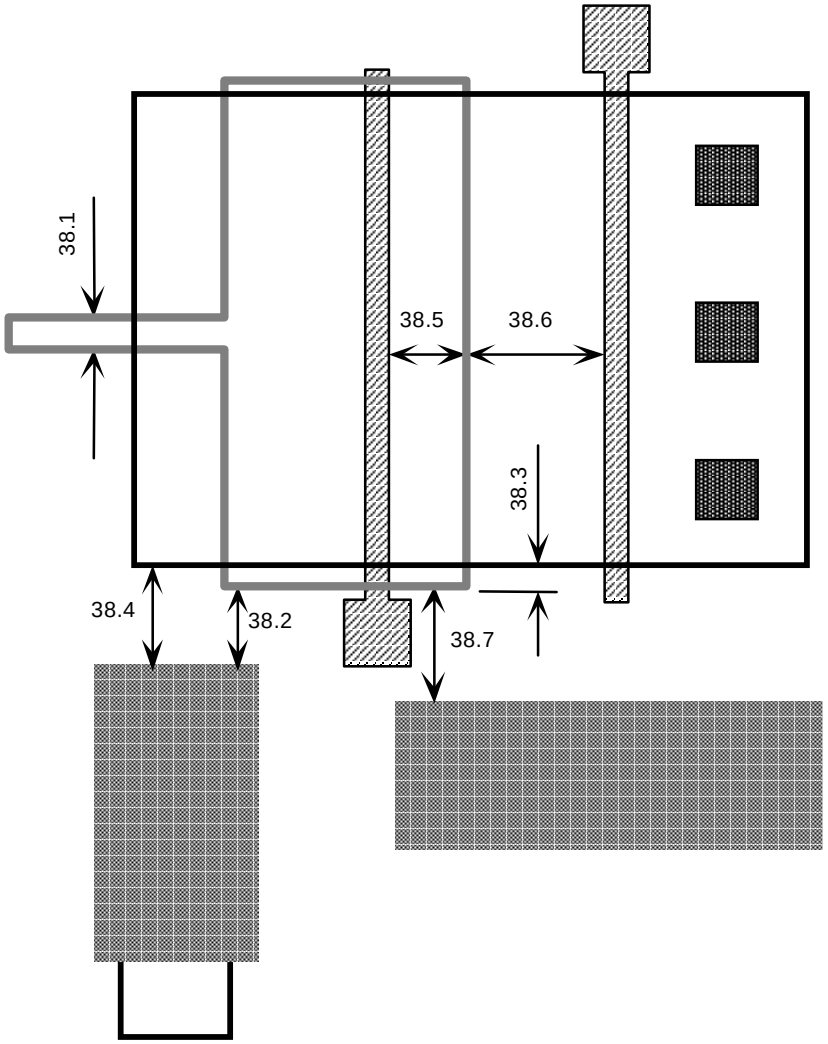


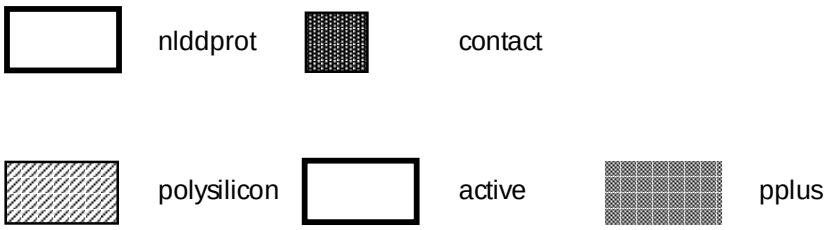
7.12 NLDDPROT (IGS layer 38)

Optional layer to be used for blocking the NLDD implant from NMOS transistors used as clamping devices for ESD protection in the I/O's. Where NLDDPROT is drawn, there will be the N^+ IMPLANT, but no NLDD implant.

38.1.	Minimum nlddprot width	0.50
38.2.	Minimum nlddprot spacing	0.50
38.3.	Minimum nlddprot extension on n^+ active area	0.30
38.4.	Minimum nlddprot spacing to n^+ active area	0.30
38.5.	Minimum nlddprot extension on polysilicon on active area	0.70
38.6.	Minimum nlddprot spacing to polysilicon gate on active area (distance between nlddprot on active to transistor gate with LDD)	0.70
38.7.	Minimum nlddprot spacing to pplus	0.50

NLDDPROT (IGS layer 38)



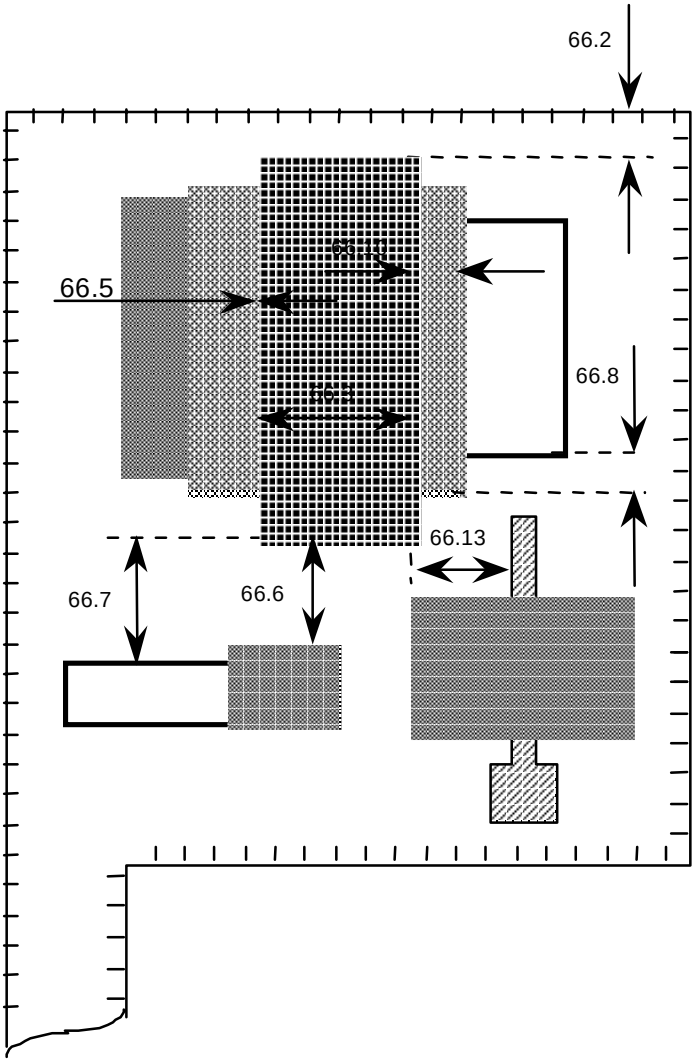


7.13 NPLUSPROT (IGS layer 66)

Optional layer to be used for blocking the N^+ implant. Where NPLUSPROT is drawn, there will be no N^+ IMPLANT, but only the NLDD implant. This level is intended to be used in the I/O's to get P^+/NLDD junction diodes for ESD protection.

66.1.	nplusprot is authorized only on n-well	
66.2.	Minimum nplusprot enclosure by n-well	0.60
66.3.	Minimum nplusprot width	1.20
66.4.	Minimum nplusprot spacing	0.80
66.5.	Fixed nplusprot spacing to pplus of related P^+/NLDD diode	0.00
66.6.	Minimum nplusprot spacing to pplus of unrelated device	0.50
66.7.	Minimum nplusprot spacing to active	0.40
66.8.	Minimum nplusprot extension on active	0.50
66.9.	nplusprot on active must be covered by sal_prot	
66.10	Minimum sal_prot extension on nplusprot (on active)	0.40
66.11	nplusprot must not intersect nlddprot	
66.12	Minimum nplusprot spacing to nlddprot, on active	0.40
66.13	Minimum nplusprot spacing to polysilicon	0.40

NPLUSPROT (IGS layer 66)



nplusprot

n-well

contact

sal_prot

polysilicon

active

pplus

7.14 N+ IMPLANT (IGS layer 16)

Defines the areas to be implanted by n^+. It is used to define active areas to become n^+ source/drains, p-well straps, n^+ active resistors and/or interconnects and n^+ doped polysilicon resistors.

This layer must not be drawn. It is automatically generated from the drawn pplus data and the drawn nplusprot data.

7.15 NLDD (IGS layer 14)

Defines the areas to be implanted by NLDD. In case no NLDDPROT is used (see section 7.12), the LDD mask is identical to the N^+ IMPLANT mask.

In case NLDDPROT is used, this IGS layer will be generated automatically from the drawn pplus data and the drawn nlddprot data.

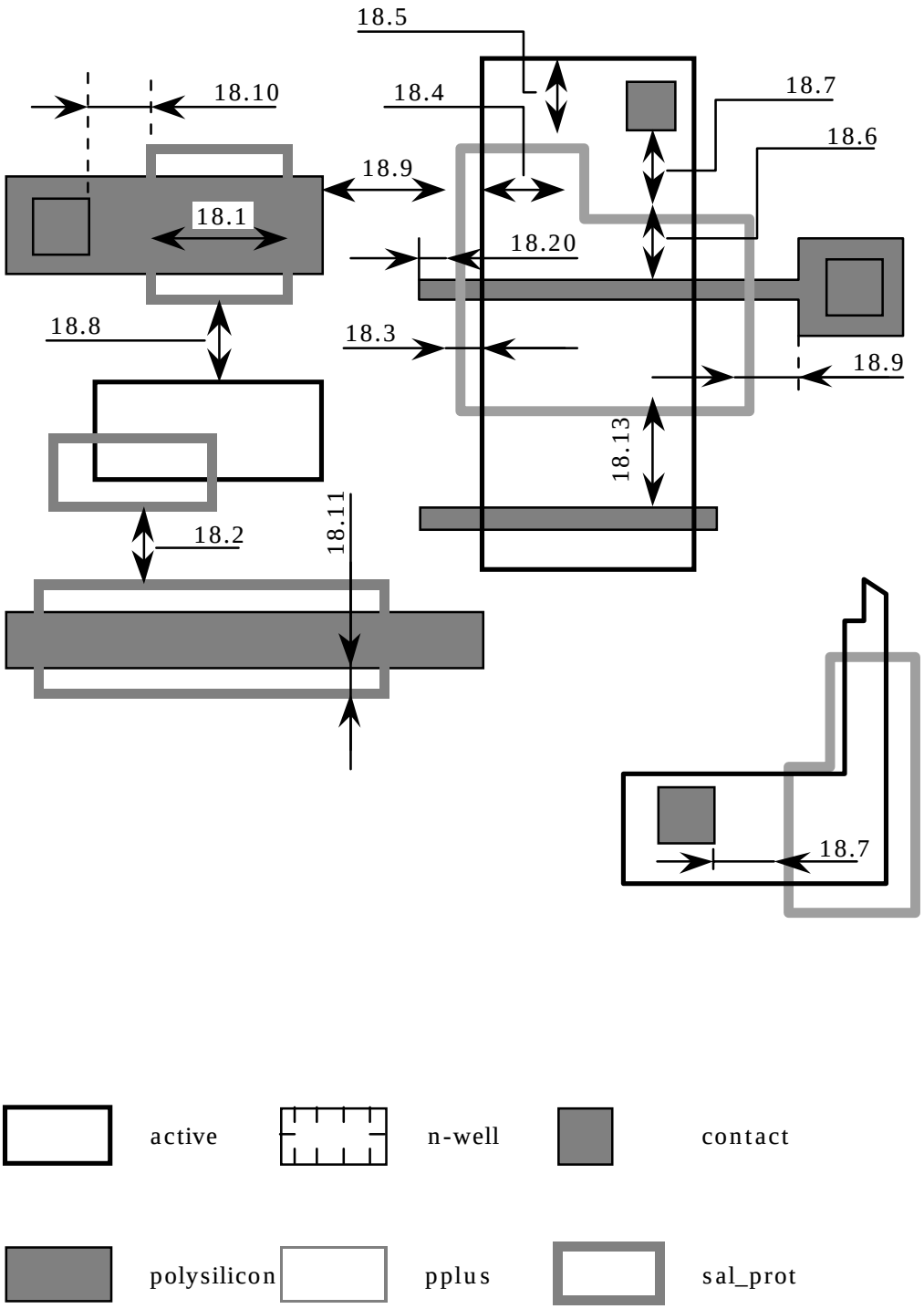
7.16 SALICIDE PROTECT (IGS layer 18)

Defines the areas where no salicidation of source, drain or poly will occur. Outside the drawn features on this layer, all active areas and polysilicon will be salicided. It is used to form unsalicided I/O transistors, unsalicided p^+ active or p^+ polysilicon resistors, and unsalicided n^+ active or n^+ polysilicon resistors. The terminals of resistors, where contact is made, will always be salicided. Resistor length is determined by the sal_prot layer; resistor width is defined by the width of the active area or the polsyilicon. The formation of unsalicided n^+/p^+ diodes in active and/or polysilicon is not allowed.

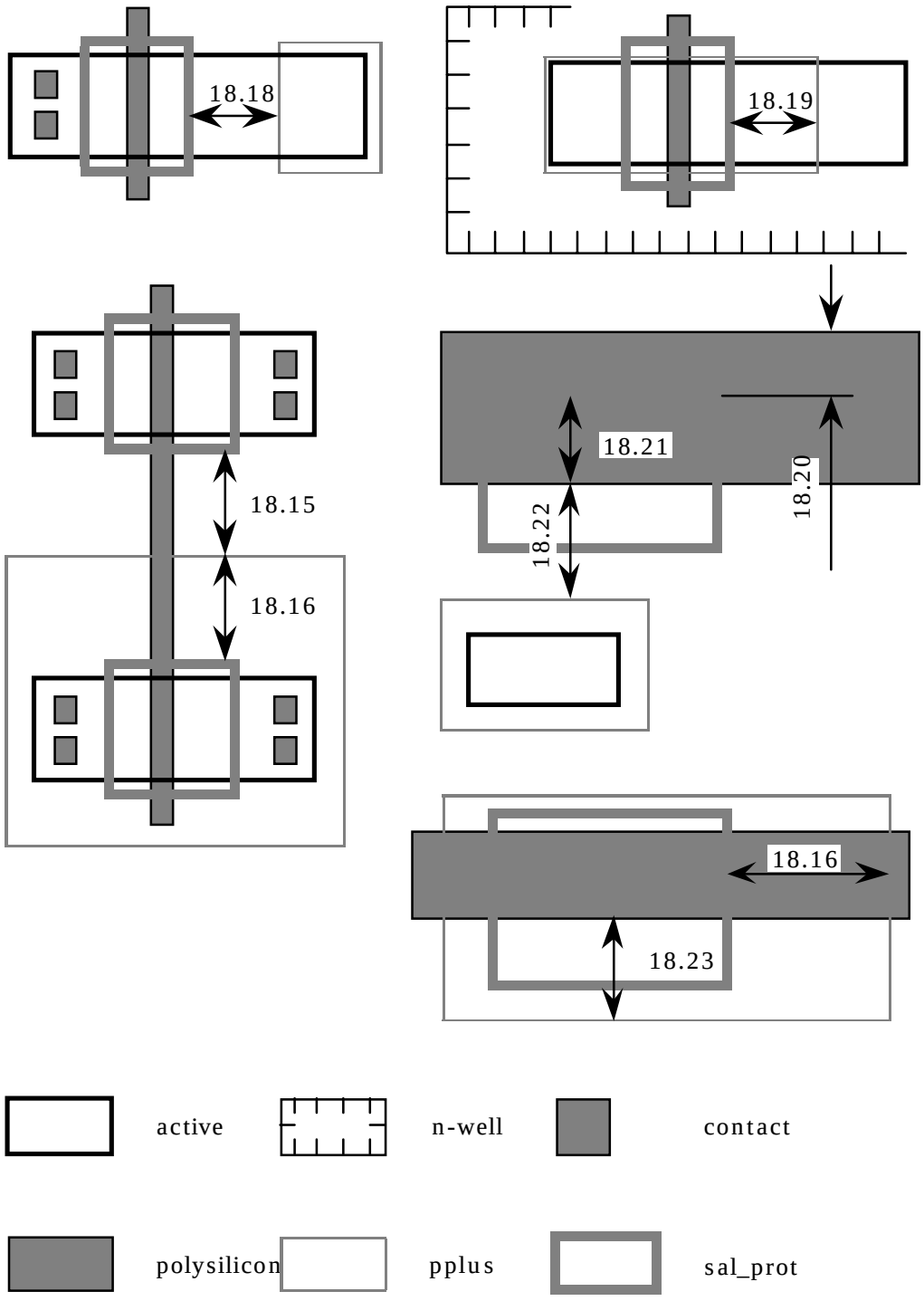
18.1.	Minimum sal_prot width	0.90
18.2.	Minimum sal_prot spacing	0.70
18.3.	Fixed sal_prot extension on active area for unsalicided source/drain	0.30
18.4.	Minimum sal_prot intersection with active area for unsalicided source/drain	0.40
18.5.	Minimum active area extension on sal_prot	0.55
18.6.	Minimum sal_prot extension on polysilicon on active area	1.20
18.7.	Minimum sal_prot spacing to contact on active area	0.35
18.8.	Minimum sal_prot spacing to active area	0.40
18.9.	Minimum sal_prot spacing to polysilicon on field oxide	0.40
18.10.	Minimum sal_prot spacing to contact on polysilicon for resistors	0.35
18.11.	Minimum sal_prot extension on polysilicon on field	0.30
18.12.	Sal_prot must overlap polysilicon gate on both sides	

18.13.	Minimum sal_prot spacing to polysilicon gate, on active area (= unsalicided active area spacing to salicided active gate)	0.65
18.14.	Unsalicided polysilicon must not be crossed by pplus boundary	
18.15.	Minimum sal_prot spacing to p^+ polysilicon, on polysilicon	0.80
18.16.	Minimum p^+ polysilicon extension on sal_prot	0.80
18.17.	In case of sal_prot intersection with abutting straps sal_prot must cross the pplus boundary	
18.18.	Minimum sal_prot spacing to p^+ active area, on active (abutting n^+/p^+)	0.80
18.19.	Minimum p^+ active area extension on sal_prot (abutting n^+/p^+)	0.80
18.20.	Minimum polysilicon extension on sal_prot	0.55
18.21.	Minimum sal_prot intersection of polysilicon for unsalicided polysilicon.	0.40
18.22.	Minimum pplus spacing to unsalicided polysilicon	0.35
18.23	Minimum pplus enclosure of unsalicided polysilicon	0.35

SALICIDE PROTECT (IGS layer 18)

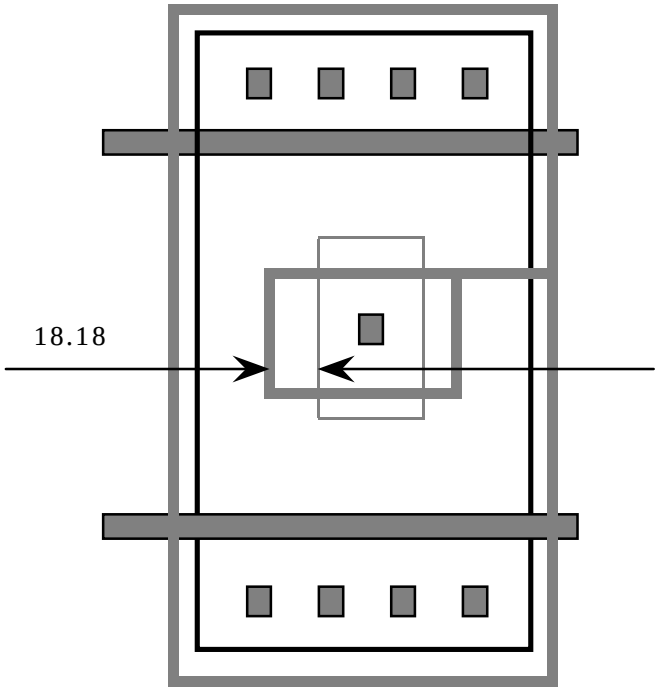


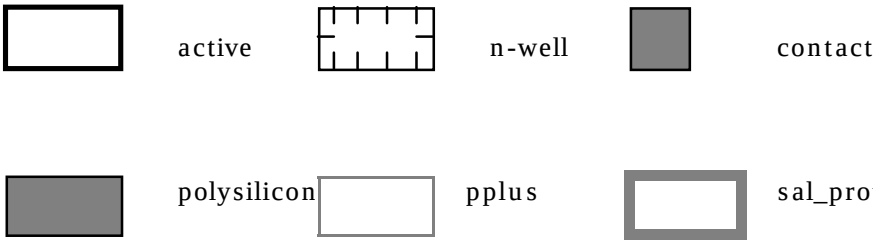
SALICIDE PROTECT (IGS layer 18, continued))



SALICIDE PROTECT (IGS layer 18, continued))

The following layout is authorised (rule 18.17).



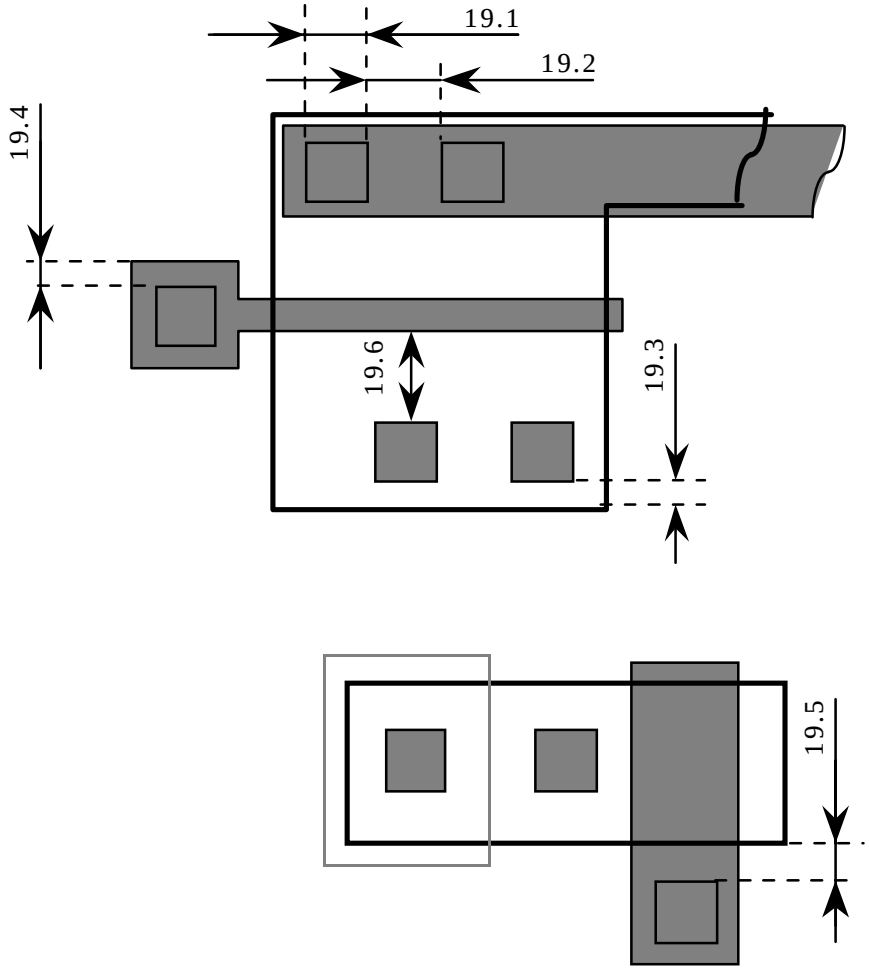


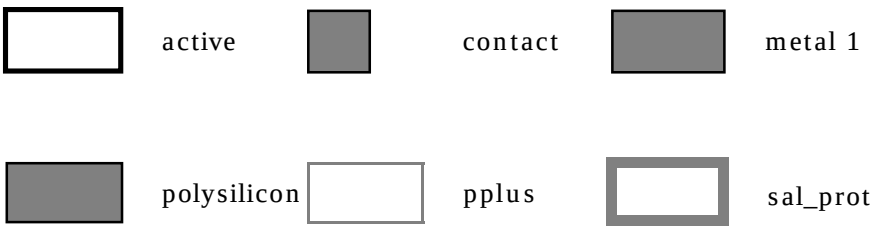
7.17 CONTACTS (IGS layer 19)

Defines the areas where contact is made from metal 1 to polysilicon and to n^+ and p^+ active areas.

19.1.	Fixed contact dimensions (width = length)	0.40
19.2.	Minimum contact spacing	0.50
19.3.	Minimum active area enclosure of contact	0.20
19.4.	Minimum polysilicon enclosure of contact	0.20
19.5.	Minimum polysilicon contact spacing to active area	0.40
19.6.	Minimum active area contact spacing to polysilicon gate	0.375
19.7.	Minimum pplus enclosure of contact (abutting p^+/n^+)	N/A
19.8.	Minimum pplus spacing to contact (abutting p^+/n^+)	N/A
19.9.	Contacts on polysilicon over active area are not allowed	
19.10.	Contacts inside sal_prot are not allowed	
19.11.	All contacts must be covered by metal 1	

CONTACTS (IGS layer 19)



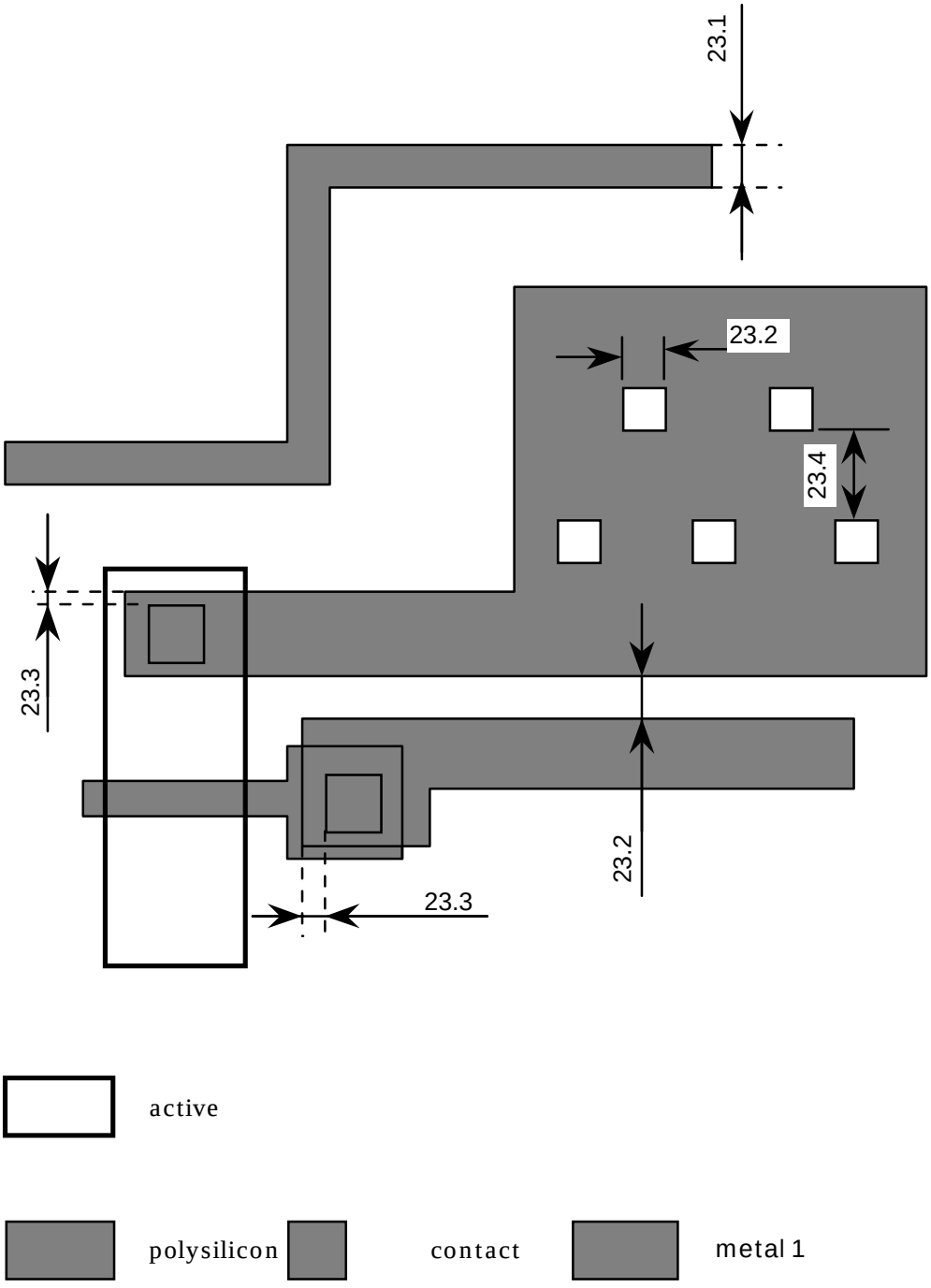


7.18 METAL 1 (IGS layer 23)

Defines the interconnect to all contacts and via 1.

23.1.	Minimum metal 1 width	0.50
23.2.	Minimum metal 1 spacing	0.60
23.3.	Minimum metal 1 enclosure of contact	0.15
23.4.	Maximum metal 1 width simultaneously in both directions If the linewidth as determined by the electromigration rules is larger than 30 µm, holes should be introduced in the layout of the metal line; the holes may have minimum layout rule dimensions, and should be staggered.	30.00

METAL 1 (IGS layer 23)

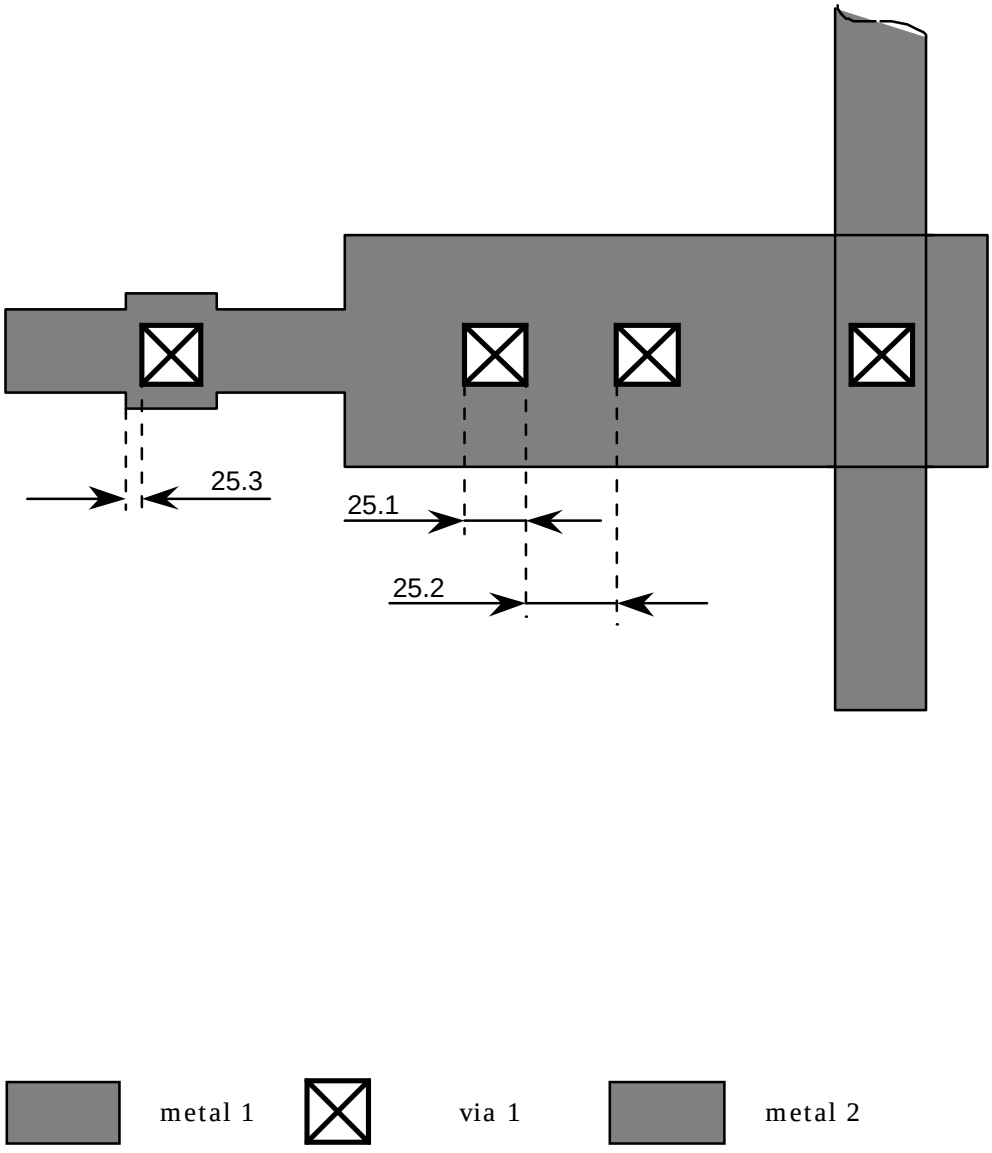


7.19 VIA 1 (IGS layer 25).19. VIA 1

Defines all contacts to be made from metal 1 to metal 2.

25.1.	Fixed via 1 dimensions (width = length)	0.40
25.2.	Minimum via 1 spacing	0.50
25.3.	Minimum metal 1 enclosure of via 1	0.15
25.4.	Via 1 over contact (stacked contact / via 1) is allowed	
25.5.	All via 1 must have underlaying metal 1	
25.6.	All via 1 must be covered by metal 2	

VIA 1(IGS layer 25)

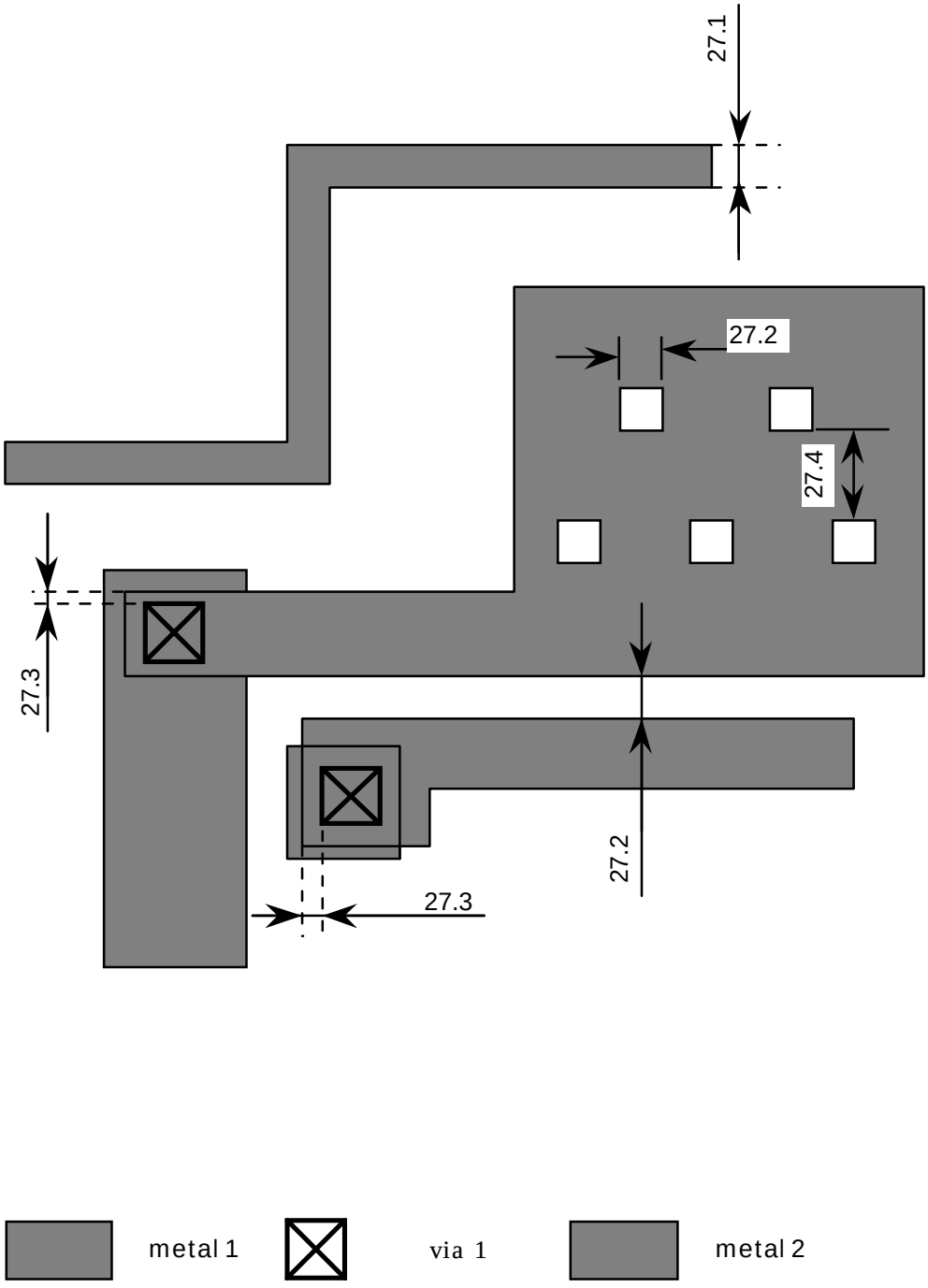


7.20 METAL 2 (IGS layer 27)

Defines the interconnect to all via 1 and via 2.

27.1.	Minimum metal 2 width	0.70
27.2.	Minimum metal 2 spacing	0.70
27.3.	Minimum metal 2 enclosure of via 1	0.15
27.4.	Maximum metal 2 width simultaneously in both directions If the linewidth as determined by the electromigration rules is larger than 30 µm, holes should be introduced in the layout of the metal line; the holes may have minimum layout rule dimensions, and should be staggered.	30.00

METAL 2 (IGS layer 27)

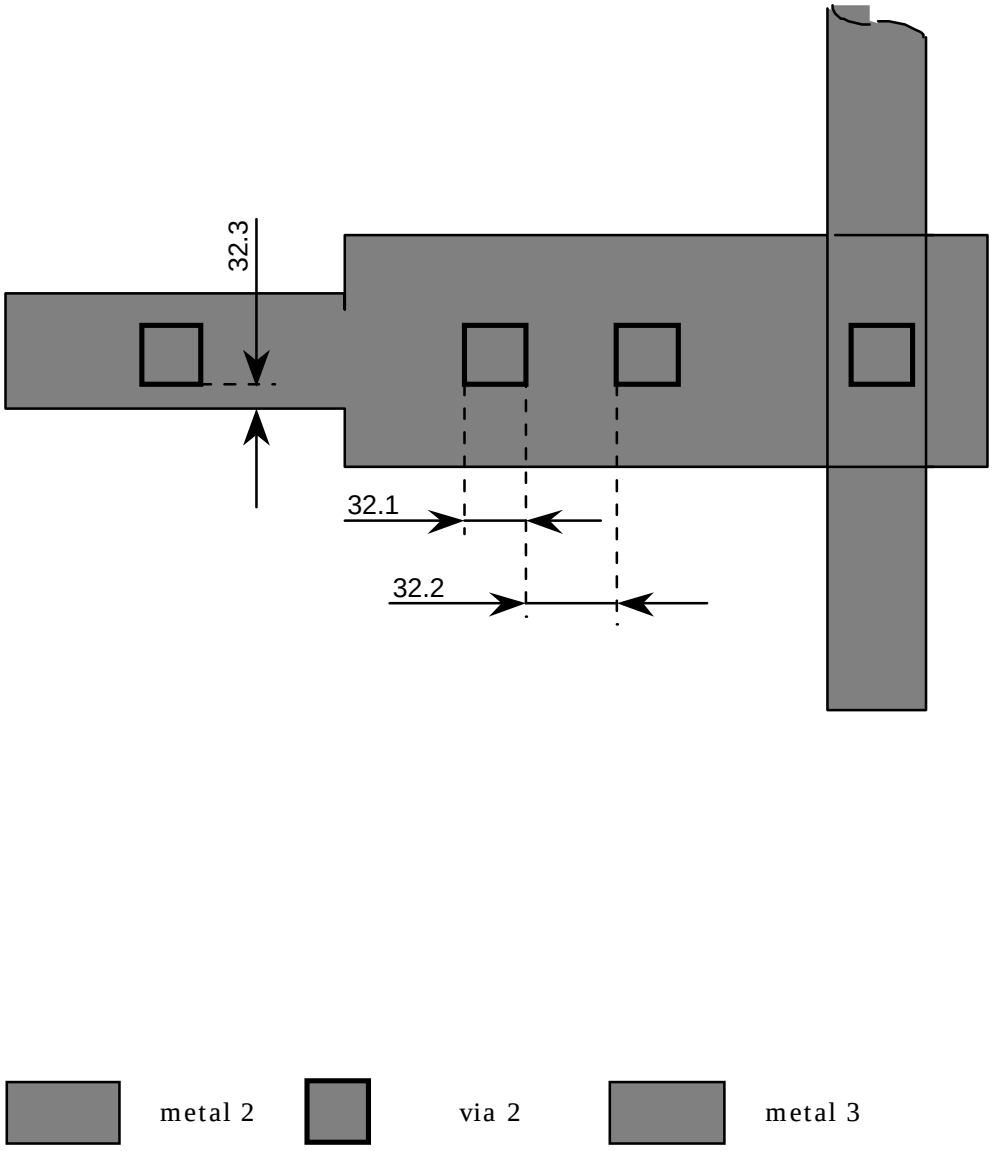


7.21 VIA 2 (IGS layer 32)

Defines all contacts to be made from metal 2 to metal 3.

32.1. Fixed via 2 dimensions (width = length)	0.40
32.2. Minimum via 2 spacing	0.50
32.3. Minimum metal 2 enclosure of via 2	0.15
32.4. Via 2 over via 1 is allowed	
32.5. All via 2 must have underlaying metal 2	
32.6. All via 2 must be covered by metal 3	

VIA 2 (IGS layer 32)

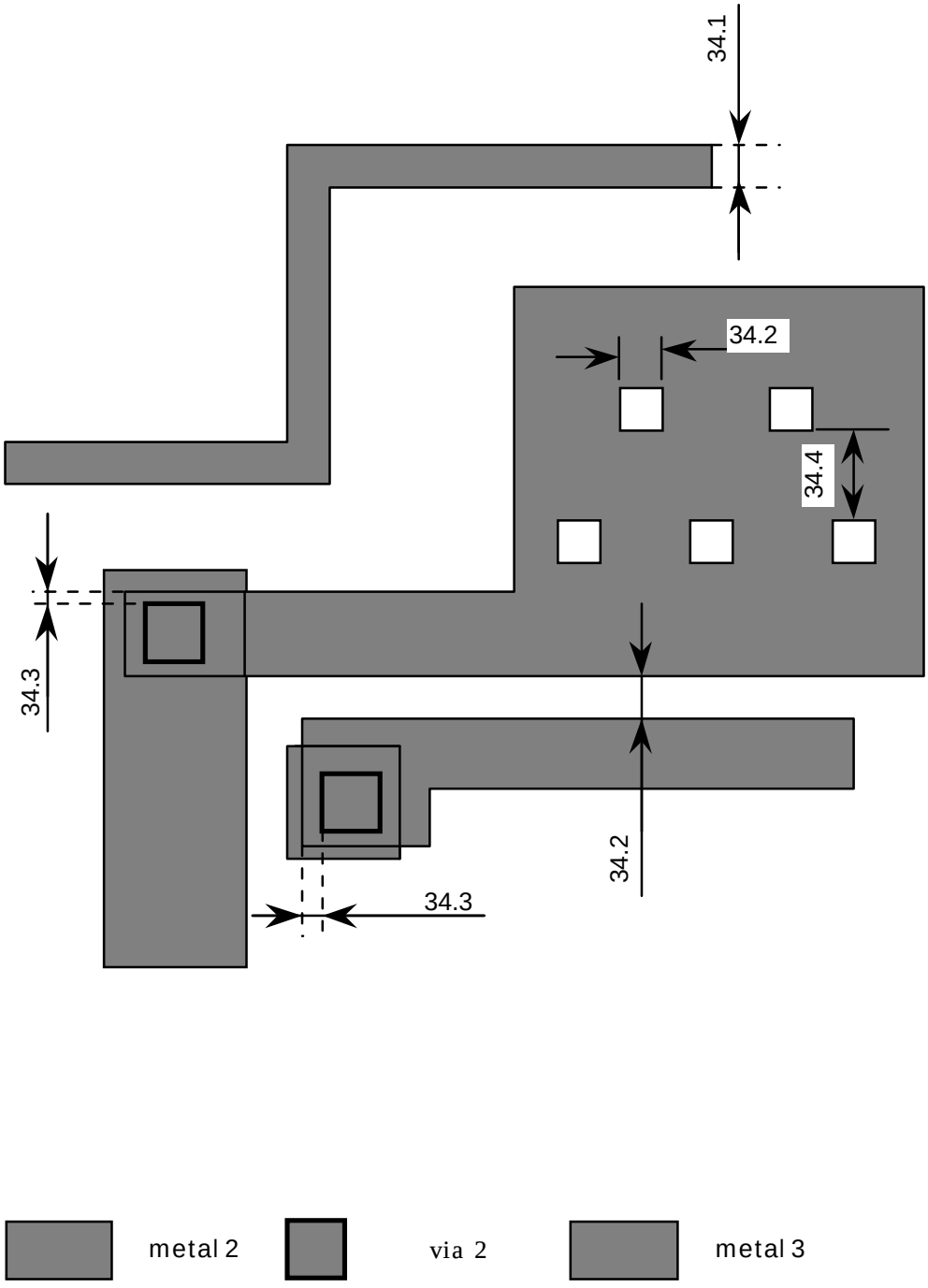


7.22 METAL 3 (IGS layer 34)

Defines the interconnect to all via 2 and via 3.

34.1.	Minimum metal 3 width	0.70
34.2.	Minimum metal 3 spacing	0.70
34.3.	Minimum metal 3 enclosure of via 2	0.15
34.4.	Maximum metal 3 width simultaneously in both directions If the linewidth as determined by the electromigration rules is larger than 30 µm, holes should be introduced in the layout of the metal line; the holes may have minimum layout rule dimensions, and should be staggered.	30.00

METAL 3 (IGS layer 34)

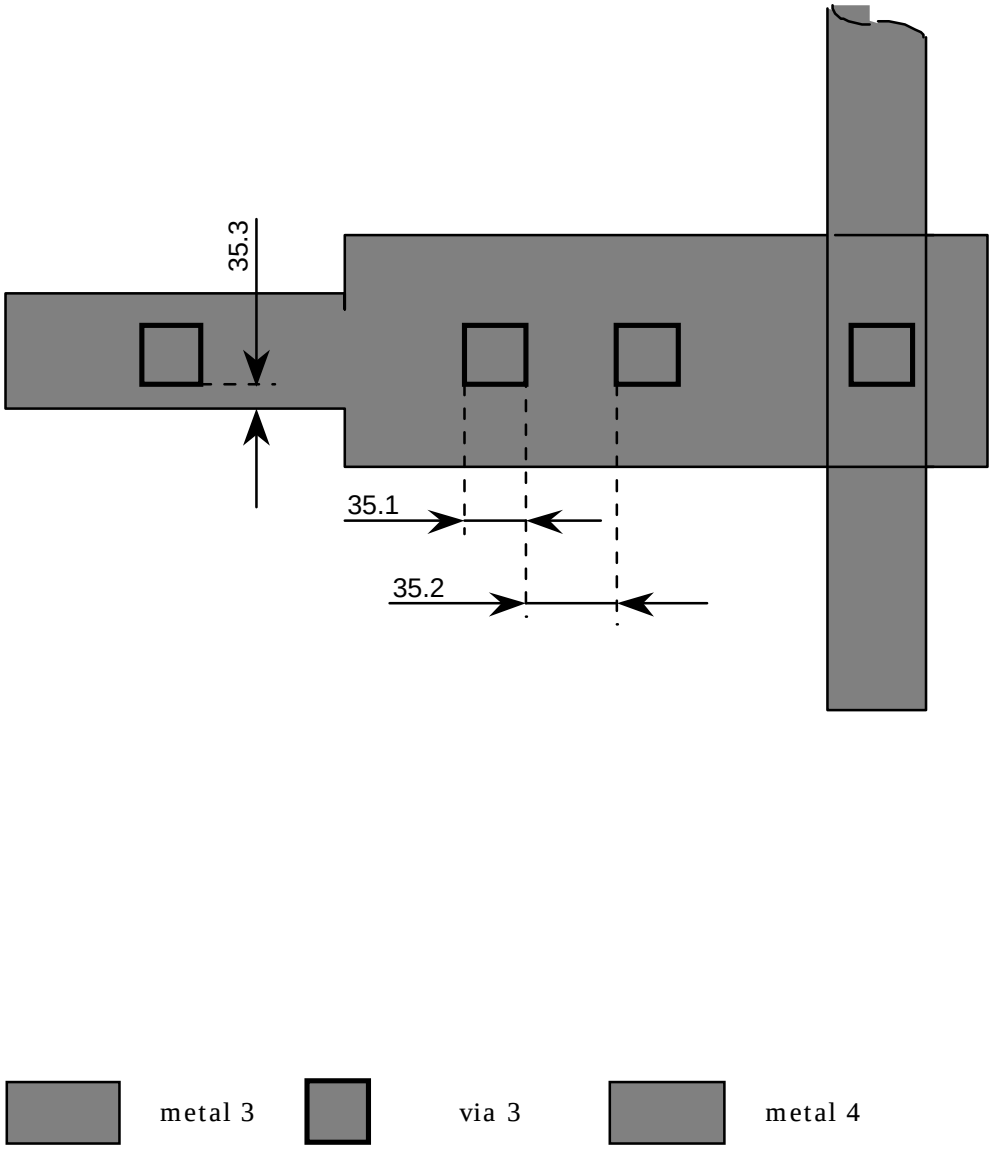


7.23 VIA 3 (IGS layer 35)

Defines all contacts to be made from metal 3 to metal 4.

35.1.	Fixed via 3 dimensions (width = length)	0.40
35.2.	Minimum via 3 spacing	0.50
35.3.	Minimum metal 3 enclosure of via 3	0.15
35.4.	Via 3 over via 2 is allowed	
35.5.	All via 3 must have underlaying metal 3	
35.6.	All via 3 must be covered by metal 4	

VIA 3 (IGS layer 35)

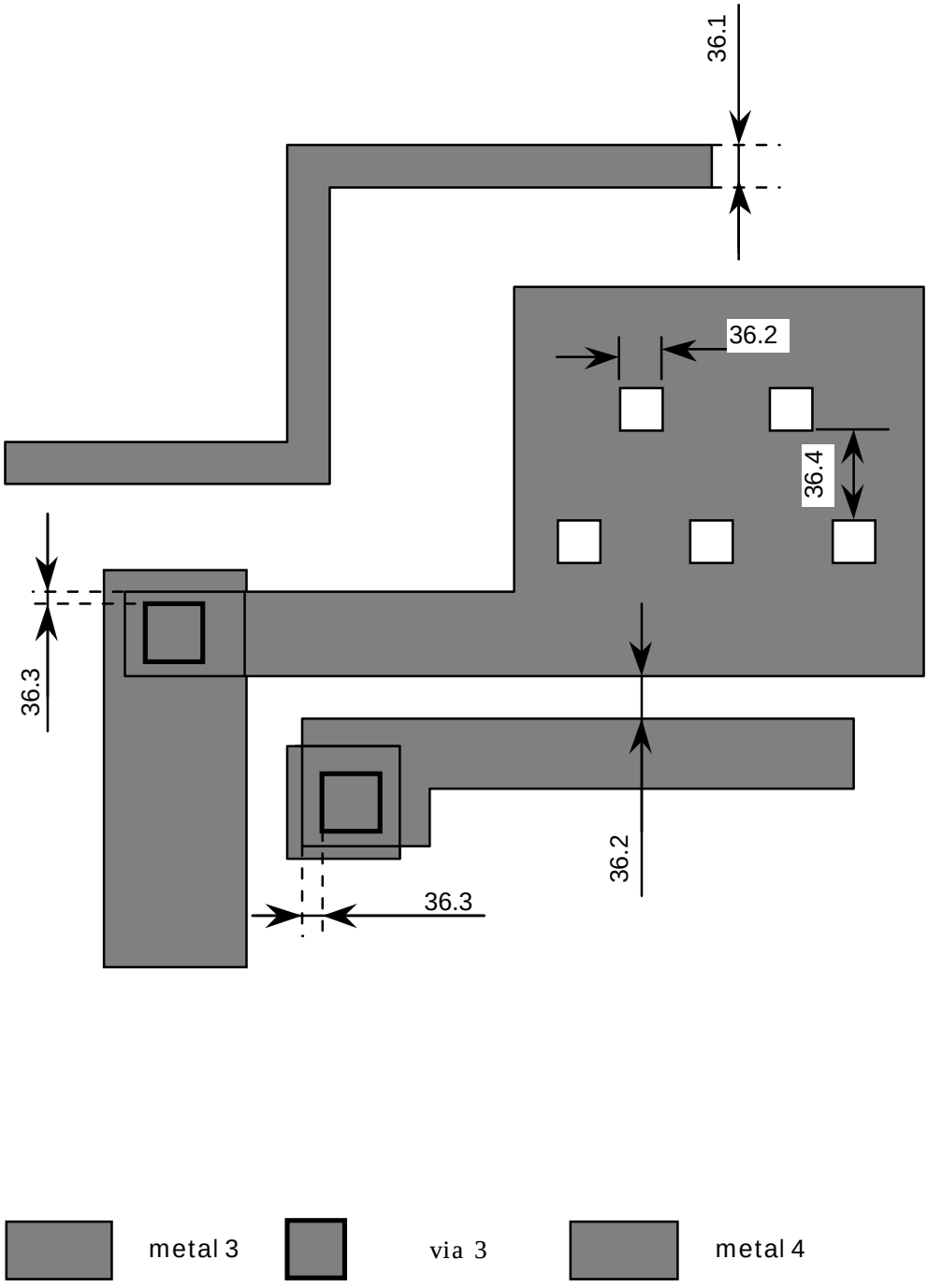


7.24 METAL 4 (IGS layer 36)

Defines the interconnect to all via 3 and via 4.

36.1.	Minimum metal 4 width	0.70
36.2.	Minimum metal 4 spacing	0.70
36.3.	Minimum metal 4 enclosure of via 3	0.15
36.4.	Maximum metal 4 width simultaneously in both directions If the linewidth as determined by the electromigration rules is larger than 30 µm, holes should be introduced in the layout of the metal line; the holes may have minimum layout rule dimensions, and should be staggered.	30.00

METAL 4 (IGS layer 36)

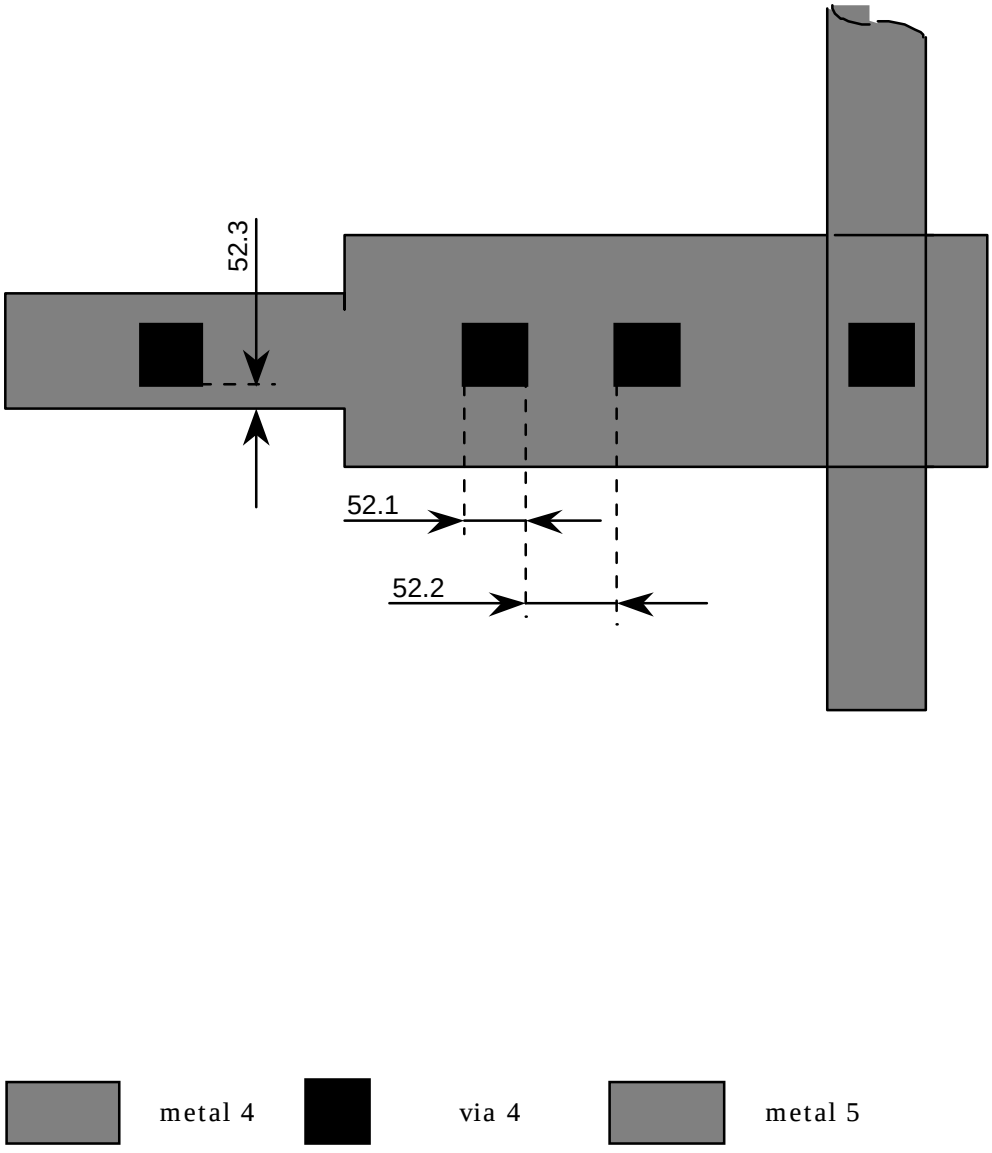


7.25 VIA 4 (IGS layer 52)

Defines all contacts to be made from metal 4 to metal 5.

52.1.	Fixed via 4 dimensions (width = length)	0.40
52.2.	Minimum via 4 spacing	0.50
52.3.	Minimum metal 4 enclosure of via 4	0.15
52.4.	Via 4 over via 3 is allowed	
52.5.	All via 4 must have underlaying metal 4	
52.6.	All via 4 must be covered by metal 5	

VIA 4 (IGS layer 52)

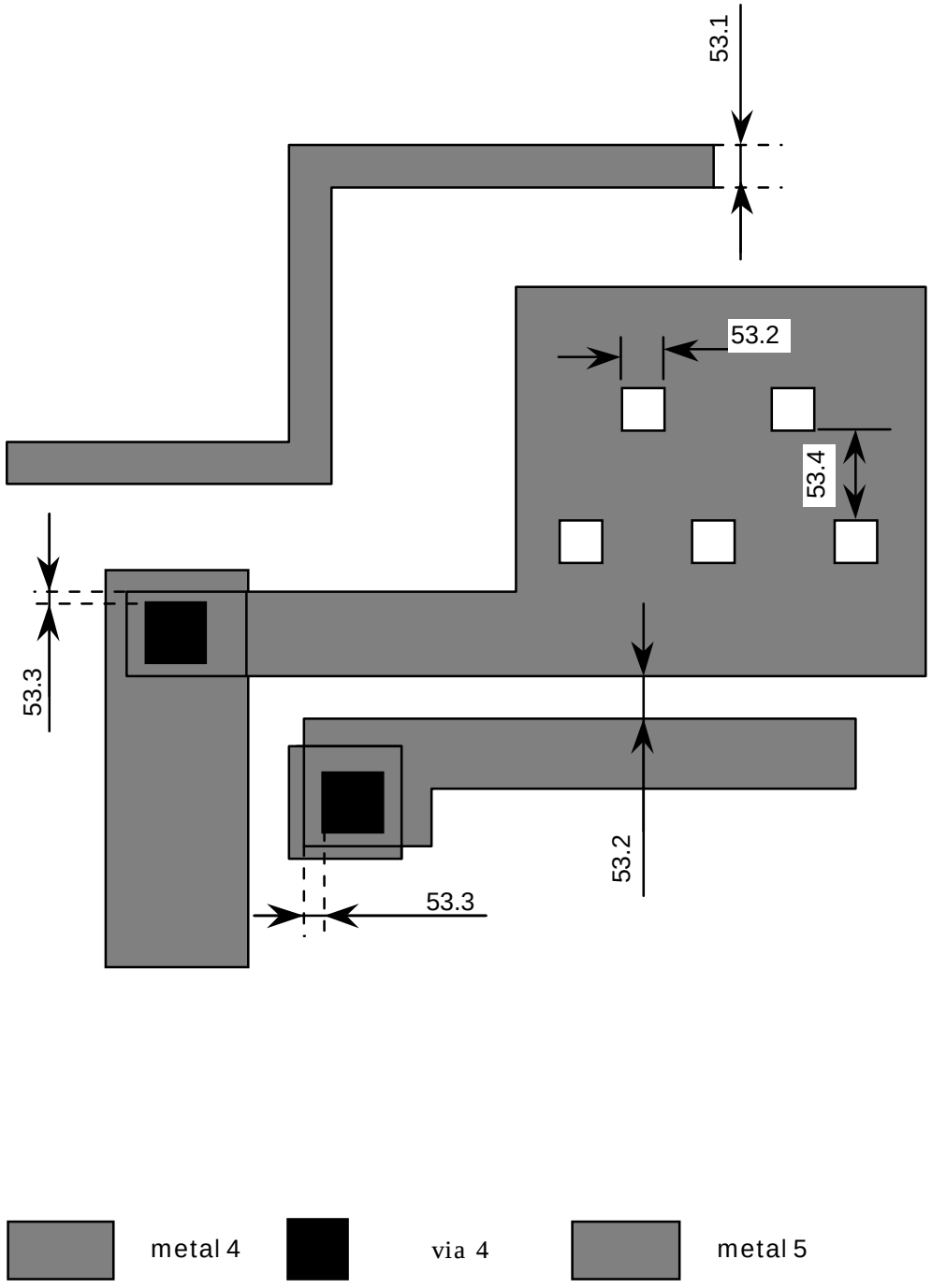


7.26 METAL 5 (IGS layer 53)

Defines the interconnect to all via 4 and bonding pads.

53.1.	Minimum metal 5 width	0.80
53.2.	Minimum metal 5 spacing	2.00
53.3.	Minimum metal 5 enclosure of via 4	0.20
53.4.	Maximum metal 5 width simultaneously in both directions If the linewidth as determined by the electromigration rules is larger than 30 µm, holes should be introduced in the layout of the metal line; the holes may have minimum layout rule dimensions, and should be staggered.	30.00

METAL 5 (IGS layer 53)



7.27 PASSIVATION (IGS layer 31)

Defines the cut-out areas for bonding pads and test pads. This is a dark field mask. Inside the feature, there is an opening in the nitride passivation.

No openings allowed except over bonding pads and test pads.

Refer to section 8 for bonding pad rules. Note that minimum pad opening and minimum pad spacing is defined by the assembly layout rules (DS 13600).

8 BONDING PADS

IN ORDER TO COMPLY WITH ASSEMBLY REQUIREMENTS, THE BOND PADS ARE MODIFIED DURING MASK GENERATION. SEE SECTION 8.3 FOR DETAILS.

8.1 Introduction

This section covers the process layout rules for bonding pads. The introduction covers definitions and general requirements.

8.1.1 A pad (bonding pad or test pad) is defined as the metal 5 area, not covered by passivation (IGS layer 31).

8.1.2 A pad consists of:

- a metal 1 pad
- a via 1 window array (see section 8.1.3.)
- a metal 2 pad
- a via 2 window array (see section 8.1.3.)
- a metal 3 pad
- a via 3 window array (see section 8.1.3.)
- a metal 4 pad
- a via 4 window array (see section 8.1.3.)
- a metal 5 pad
- a nitride (passivation) opening

8.1.3 Tungsten plug processing is not compatible with large open contacts and vias. In this process, for via 1, via 2, via 3 and via 4, the large via is replaced by an array of minimum size vias with a 2.0 µm pitch.

The via 3 array is superimposed with the via 1 array.
The via 4 array is superimposed with the via 2 array.
The via 2 and via 4 arrays are shifted by 1.0 µm from the via 1 and via 3 array, both in X- and Y- directions.

8.1.4 An isolated n-well under the pads is recommended (but not mandatory) to eliminate leakage. There must be no active area nor polysilicon under the pads.

8.1.5 The minimum pad opening and the minimum pad spacing are package type specific and are defined by the assembly layout rules (refer to Alcatel Microelectronics specification DS 13600).

8.1.6 Bonding pad 1 will preferably be angled at all four corners; only 45° angles are allowed.

8.1.7 It is recommended that metallization to a bonding pad is through a metal fillet and leadaway. The related rules in the section hereafter are not mandatory but recommended rules.

8.2 BONDING PAD LAYOUT RULES

8.2.1. Minimum metal 5 enclosure of pad	5.00
8.2.2. Minimum metal 4 enclosure of pad	4.00
8.2.3. Minimum metal 3 enclosure of pad	3.00
8.2.4. Minimum metal 2 enclosure of pad	2.00
8.2.5. Minimum metal 1 enclosure of pad	1.00
8.2.6. Minimum metal 4 enclosure of via 4	5.00
8.2.7. Minimum metal 3 enclosure of via 3	5.00
8.2.8. Minimum metal 2 enclosure of via 2	5.00
8.2.9. Minimum metal 1 enclosure of via 1	5.00
8.2.10. Fixed via 4 size in the array (width = length)	0.40
8.2.11. Fixed via 4 spacing in the array	1.60
8.2.12. Fixed via 3 size in the array (width = length)	0.40
8.2.13. Fixed via 3 spacing in the array	1.60
8.2.14. Fixed via 2 size in the array (width = length)	0.40
8.2.15. Fixed via 2 spacing in the array	1.60
8.2.16. Fixed via 1 size in the array (width = length)	0.40

8.2.17.	Fixed via 1 spacing in the array	1.60
8.2.18.	Minimum n-well enclosure of pad (note that the presence of a n-well is not mandatory)	8.00
8.2.19.	Minimum rnwell enclosure of pad, if rnwell is drawn under the pad	8.00
8.2.20.	Minimum metal fillet width along the pad	1.00
8.2.21.	Minimum metal fillet length	15.00
8.2.22.	Minimum metal leadaway width	8.00
8.2.23.	Minimum metal leadaway length	15.00
8.2.24.	Active area under pad is not allowed	
8.2.25.	Polysilicon under pad is not allowed	

8.3 RING BOND PADS

In order to comply with assembly requirements, it is necessary to generate “ring bond-pads” by cutting away a section of metal from the central region of the bond pad. This operation is carried out at mask preparation on all metal layers except metal 5. Metal 5 is not changed.

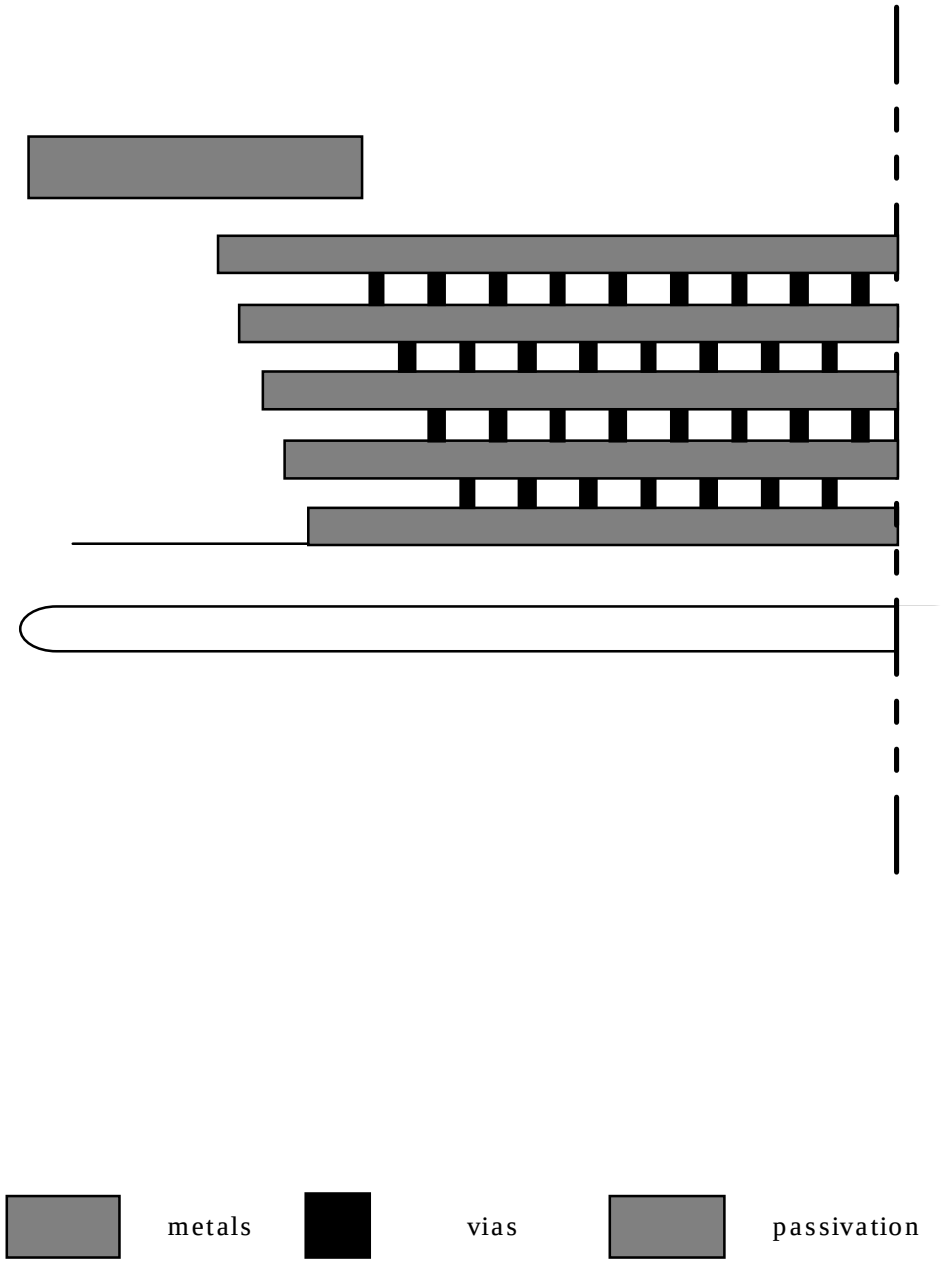
The size of the hole to be cut is determined as follows:

- The central region of the pad is cut, up to a distance of 16microns inside the passivation opening. For a bond-pad of 65µm square, designed in accordance with the rules in sections 8.1 and 8.2, with the additional requirement that the outer edge of the outermost ring of via’s must be no more than 6µm inside the pad opening, this results in at least 500 vias remaining after cutting the hole (500 via1 and more of the higher layers). This corresponds to a maximum current of 250mA at the maximum current of 0.5mA/via (see Electromigration Rules in section 10 of this document). Pads with larger opening have more vias provided they are also designed according to these rules.

NOTES:

- the size of the pad opening is checked by the DRC. Pads less than 65µm in one dimension give a warning. It will be assumed that no wire bonding is required on these pads and therefore no holes will be cut.

BOND PAD ARCHITECTURE



9 SCRIBE LANE AND EDGE OF DIE

9.1 Introduction

This section covers the process layout rules for the scribe lane and the edge of die. The introduction covers definitions and general requirements.

9.1.1 The purpose of this section is to define a scribe lane and an edge of die which will give a moisture resistant die, without the possibility that cracks generated during sawing can propagate into the die.

9.1.2 For the following rules, all dimensions are in microns and refer to the internal side of the edge of die. The seal ring width is 23 µm. In the table (see section 9.2), 0 means internal side of the die (near the circuit), and 23 is the external side of the die.

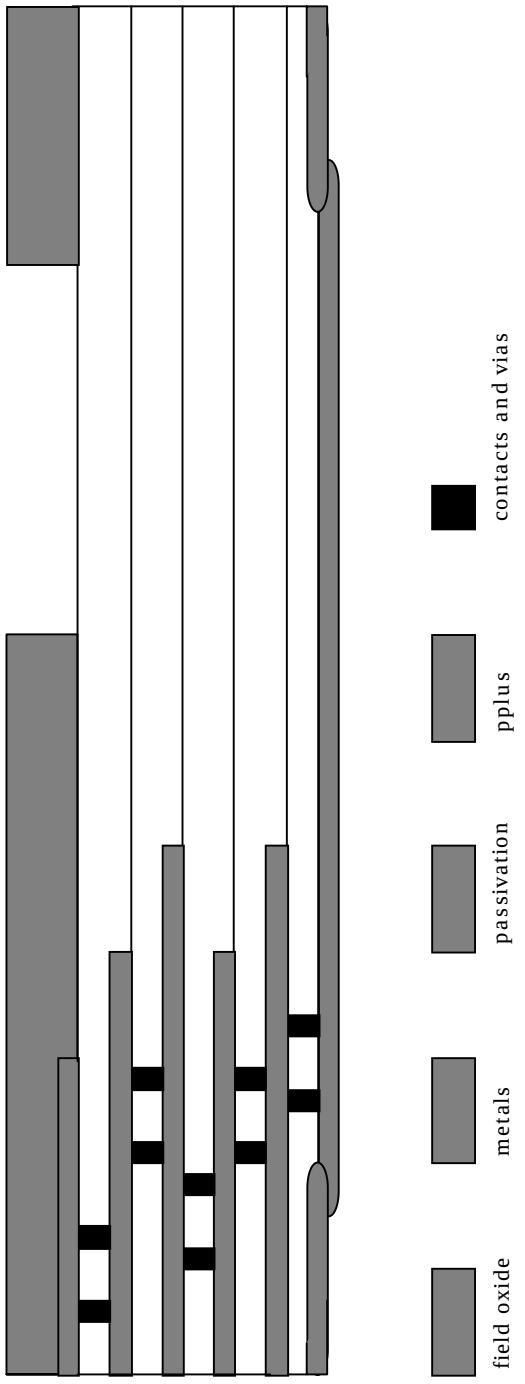
9.1.3 Contacts and vias of the seal ring are organized in 2 rows of 0.5 µm x 0.5 µm contacts/vias; in each row, contacts and vias are separated by 0.6 µm, and displaced with respect to each other by half the period (0.55 µm). As the total length of contact/via row is probably not a multiple of the pitch, some spaces can be increased, but the contacts/via size can not be changed.

9.2 LAYOUT OF EDGE OF DIE

	Layer	Drawn ?	From	To
9.2.1.	nwell	no		
9.2.2.	active	yes	4.00	22.00
9.2.3.	poly	no		
9.2.4.	pplus	yes	3.00	23.00
9.2.5.	sal_prot	no		
9.2.6.	contact	yes (2 dash lines)	5.00 6.50	5.50 7.00

9.2.7.	metal 1	yes	0.00	10.00
9.2.8.	via 1	yes (2 dashed lines)	4.00 5.50	4.50 6.00
9.2.9.	metal 2	yes	0.00	8.00
9.2.10.	via 2	yes (2 dashed lines)	2.00 3.50	2.50 4.00
9.2.11.	metal 3	yes	0.00	10.00
9.2.12.	via 3	yes (2 dashed lines)	4.00 5.50	4.50 6.00
9.2.13.	metal 4	Yes	0.00	8.00
9.2.14.	via 4	Yes (2 dashed lines)	1.00 2.50	1.50 3.00
9.2.15.	metal 5	Yes	0.00	6.00
9.2.16.	passivation	Yes	14.00	21.00

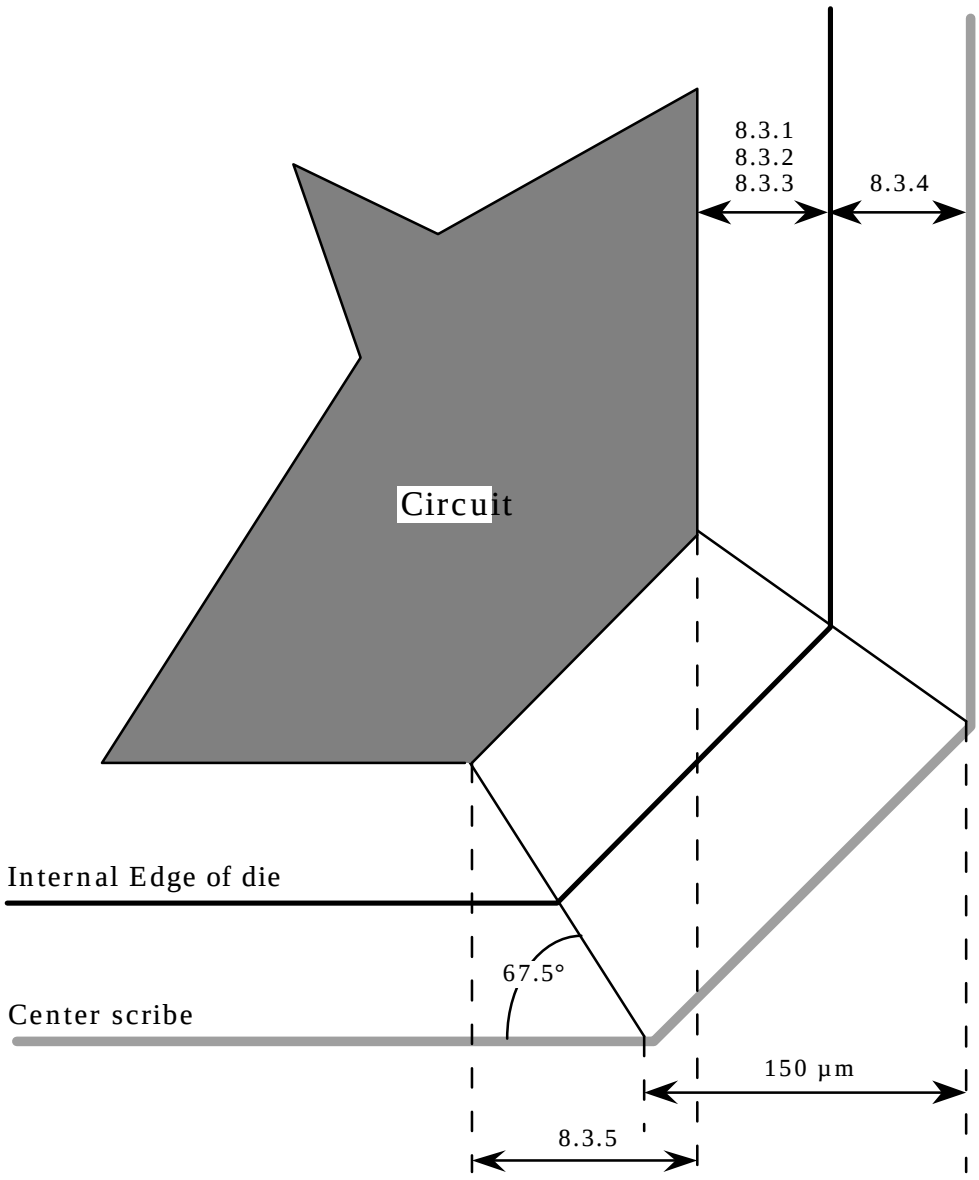
LAYOUT OF EDGE OF DIE - CROSS SECTION



9.3 EDGE OF DIE PLACEMENT RULES

9.3.1.	Minimum n-well spacing to internal edge of die	35.00
9.3.2.	Minimum active area spacing to internal edge of die	35.00
9.3.3.	Minimum polysilicon spacing to internal edge of die	35.00
9.3.4.	Minimum internal edge of die spacing to centre of scribe lane	80.00
9.3.5.	Minimum circuit corner truncation	89.00
9.3.6.	Minimum internal edge of die spacing to circuit V_{SS} metal bus if at same potential	0.00
9.3.7.	Minimum internal edge of die spacing to circuit V_{SS} metal bus if at different potential	3.00
9.3.8.	Minimum bonding pad spacing to internal edge of die	30.00

EDGE OF DIE - PLACEMENT RULES



10 RELIABILITY LAYOUT RULES

10.1 CMOS Latch-Up and ESD

10.1.1 I/O Cells

Only standard I/O cells are allowed for latch-up and ESD protection. Any deviations from the standard I/O cells should be communicated to Alcatel Microelectronics.

10.1.2 Core Cells

10.1.2.1 It is recommended to use as many n-well and p-well straps as possible.

10.1.2.2 Active area should be covered with contacts and metal straps as much as possible.

10.2 Electromigration layout rules.

The purpose of this section is to provide layout rules for interconnect linewidths and contacts and vias, such that the current density will not exceed 2 $mA/\mu m^2$, a level consistent with the failure rate goal of 1% failures in 20 years or 57 FITs.

10.2.1 Contacts and vias

10.2.1.1 Only minimum dimension contacts and vias are allowed.

10.2.1.2 The minimum number of contacts or vias required for an equivalent current level is:

$$N = K_c \times I_{eq} \times f(T)$$

where

$K_c = 1 /$ (max. current through single contact)

$f(T) = \exp \{ 11.7 \times (1 - 415/T) \}$

T is the absolute operating temperature (in Kelvin) determined for the worst case of each design.

I_{eq} is the equivalent current determined as specified in section 10.2.3.

10.2.1.3 The appropriate values for K_c and the maximum current per contact are given in the table below:

a	Units	Contacts	Vias
size	[µm]	0.40	0.40
max current /contact	[mA / ct]	1.10	0.53
K_C	[mA^{-1}]	0.90	1.88

10.2.2 Conductors

10.2.2.1 The minimum drawn line width for aluminum-alloy interconnections (metal layers) is given by:

$$W = K \times I_{eq} \times f(T) + \Delta(W)$$

where

$$K = 1 / \{ T_{Al}(min) \times SC_{Al} \times I_{max} \}$$

T_{Al} (min) = minimum aluminum thickness

SC_{Al} = aluminum stepcoverage

$$f(T) = \exp \{ 9.8 \times (1 - 415/T) \}$$

$\Delta(W)$ = metal CD variation

I_{max} = 2 $mA/\mu m^2$

T is the absolute operating temperature (in Kelvin) determined for the worst case application and package type of each design.

I_{eq} is the equivalent current determined as specified in section 10.2.3..

10.2.2.2 The appropriate values for K, minimum metal thickness, metal step-coverage and $\Delta(W)$ are given in the table below:

a	Units	Metal 1	Metals 2, 3, 4	Metal 5
T_{Al} (min)	nm	396	495	765
SC_{Al} (min)		0.95	0.95	0.95
K	µm/mA	1.33	1.06	0.68
$\Delta(W)_{max}$	µm	0.05	0.07	0.08

10.2.3 Determination of Equivalent Current

10.2.3.1 Low frequencies (period > 200 nsec)

For repetition frequencies less than 5 MHz, the RMS current equivalent should be used.

DC current: the equivalent current is equal to the direct current.

Pulse DC: the RMS current shall be calculated as:

$$I_{Ieq} = \sqrt{\frac{\int_{T_0}^{T_0+T_c} i(t)^2 \times dt}{T_c}}$$

The limits of the integral are T_0 to $T_0 + T_c$, or the equivalent derived from circuit simulations.

AC current (Bi-directional): for AC current, each pulse shall be considered separately so each one shall be integrated over the full period, and the maximum value has to be taken.

10.2.3.2 High frequencies (period = 200 nsec)

For repetition frequencies greater than 5 MHz, the average of the absolute value of the current equivalent should be used.

DC current: the equivalent current is equal to the direct current.

Pulse DC: for pulse DC current, irregular current waveforms in one direction, and each direction component of AC current, the current shall be averaged over the worst case operating cycle.

AC current (Bi-directional): for AC current, each pulse shall be considered separately so each one shall be integrated over the full period, and the maximum value has to be taken.

10.2.3.3 Peak Current

The table below summarizes the peak current to consider depending on the peak duration.

Peak Duration (ns)	= 5 ns	> 5ns < 100 ns	= 100 ns
Peak Current ($ma/\mu m^2$)	200	100	50

10.3 ESD Protection

In previous generation processes, contact to poly space in output buffers was increased to avoid metal melting in the contacts during an ESD event. This was also reducing current crowding.

Five major design related parameters are critical for ESD performance:

10.3.1 Unsalicided active area

In C035M, as in C05M, salicided active areas make current crowding more critical, so ESD performance is increased by preventing salicide formation. This is done with the salicide protect mask (IGS layer 18, sal_prot). Layout rule 18.6 is process related; it does not guarantee ESD performance. A larger value, in particular at the hot side of the transistor, is necessary to achieve the ESD performance required for each product.

10.3.2 Gate length of the transistor

Optimum ESD performance occurs for the minimum channel length, due to the better activation offered by the parasitic npn transistor. This is the reason why it is advised to use minimum gate length for ESD protection devices in I/O's.

10.3.3 Width of the transistor

Due to current density considerations, it is advised to use large transistors.

10.3.4 LDD suppression

NMOS transistors have been proven to be efficient as clamping devices without LDD structure. This can be done by using the nlddprot layer (IGS layer 38).

10.3.5 N+ implant suppression

This feature is used to create P^+/NLDD clamping diodes which are used in I/O protection circuitry.

10.4 Hot carrier injection constraints

10.4.1 Introduction

The hot carrier elementary device drift-time is conventionally defined by the time necessary to attain 10% degradation of typical MOS parameters:

g_m, V_t (extrapolated, @ V_{ds}= 100 mV), I_{dlin} (@ V_{ds}= 100 mV, V_{gs}= 3.3 V), I_{dsat} (@ V_{gs}= V_{ds}= 3.3 V, measured in both normal and reverse mode)

under static worst case stress conditions.

For NMOS transistors, the classical 10 years drift-time under nominal operating conditions (i.e. bias and gate length) for worst case DC bias conditions is no longer guaranteed for all the parameters.

While V_t and I_{dsat} present drift-time higher than 10 years, this is not the case for other parameters. However, it is well known that actual product lifetime is much higher than worst case DC elementary device drift-time, but the relation between them depends on each particular design.

Worst case DC bias conditions, for n-channel transistors corresponding to maximum substrate current conditions, are not realistic compared to the

actual internal bias conditions inside logic circuits. For a given power supply voltage, there is a very high ratio of stress between worst DC case and actual circuit cases.

10.4.2 AC Lifetime Calculation

Transistors do not normally operate continuously in worst case degradation conditions. The real lifetime (AC lifetime) can be calculated from the DC lifetime according to the following formula:

$$\tau_{AC} = \tau_{DC} \times \frac{TotalPeriod}{Timecurrentnotzero}$$

Where τ_{AC} = AC lifetime
and τ_{DC} = DC lifetime

For digital circuits this can be approximated by:

$$\tau_{AC} = \tau_{DC} \times \frac{TotalPeriod}{\tau_{rise} + \tau_{fall}}$$

10.5 Plasma induced charging rules

10.5.1 Introduction

In today's deep-submicron technologies, more and more plasma enhanced process steps are used. It is the case for metal etch, polysilicon etch, via etch, resist ashing, oxide deposition, etc..

Plasma steps are subject to non-uniformity across the wafer. This can lead to local non-equilibrium between ion flux and electron flux, creating either positive or negative charges to be abnormally generated. When collected by conducting wires directly connected to the gate of MOS devices, these charges can have several impacts of different damages:

- Vt shift between metal 1 and metal 5 test
- oxide degradation
- hot carrier performance degradation

It has been demonstrated that MOS devices connected to the routing metallizations with high antenna ratio can have latent oxide defects which leads to degradation of the oxide lifetime.

The following "antenna rules" should be considered in order to avoid reliability of the circuit being affected during life time.

10.5.2 Antenna ratio definition

The different metal layers wires can act as "antennas" for collection of charges. The antenna ratio for a polysilicon node is defined as:

$$AR = \frac{A_{m1} + A_{m2} + A_{m3} + A_{m4}}{A_{gate}}$$

where

A_{gate} = gate area connected to the node

A_{m1} = metal 1 area electrically connected to the node either directly or through a polysilicon line, and not connected to an active area

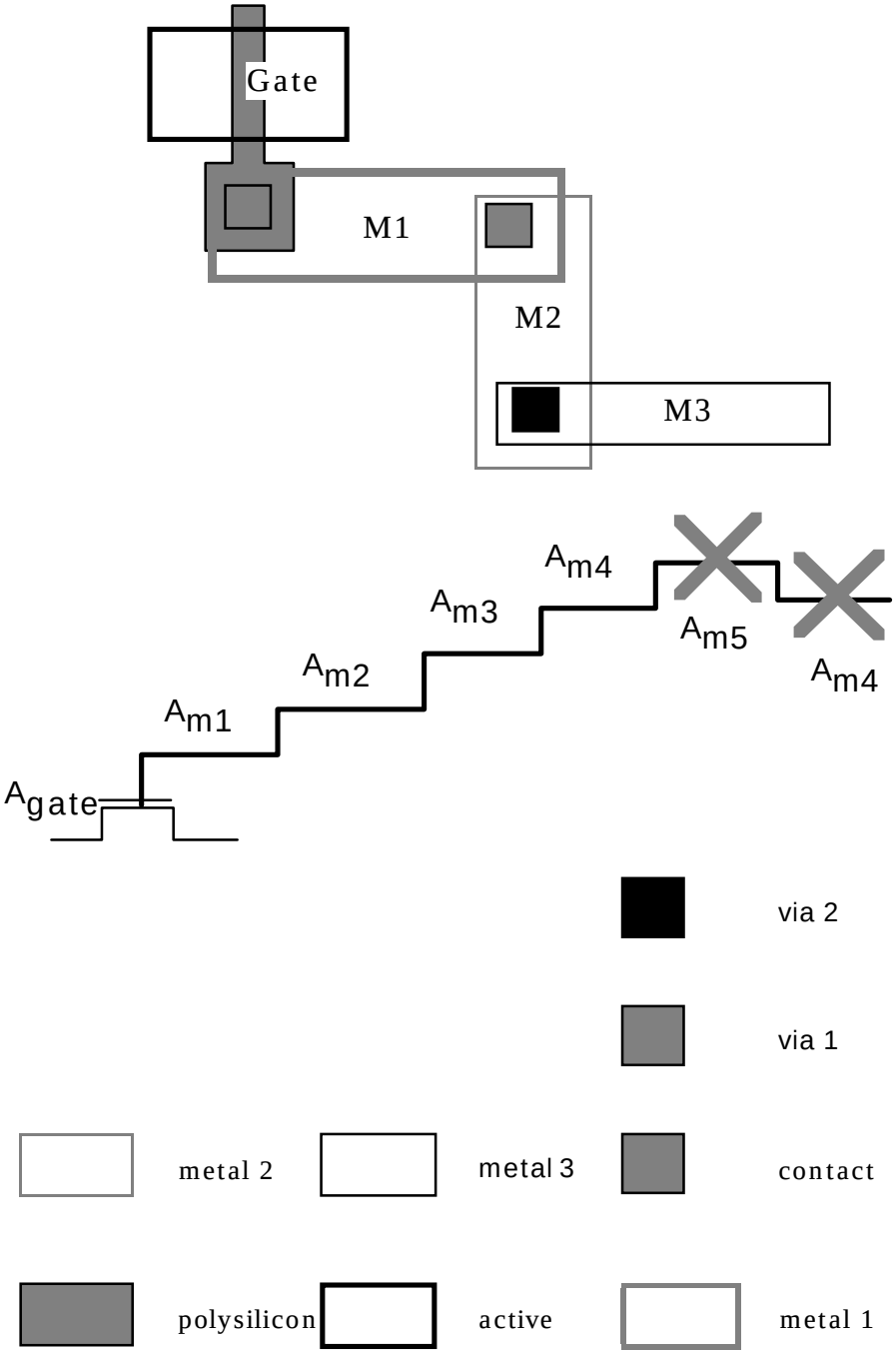
A_{m2} = metal 2 area electrically connected to the node without using metal 3,and not connected to an active area at metal 1

A_{m3} = metal 3 area electrically connected to the node without using metal 4,and not connected to an active area at metal 1 or metal 2

A_{m4} = metal 4 area electrically connected to the node without using metal 5,and not connected to an active area at metal 1, metal 2 and metal 3

The definition of antenna ratio is illustrated on the next page. The maximum allowed antenna ratio is 300.

ANTENNA RATIO (definition)



10.5.3 Guidelines to decrease the antenna ratio

In all cases where it is possible in terms of silicon area availability, diode connection of metal lines to active area is recommended. The diodes act as a sink to the substrate for the charges created during following processing steps, preventing the transistor from subsequent damage.

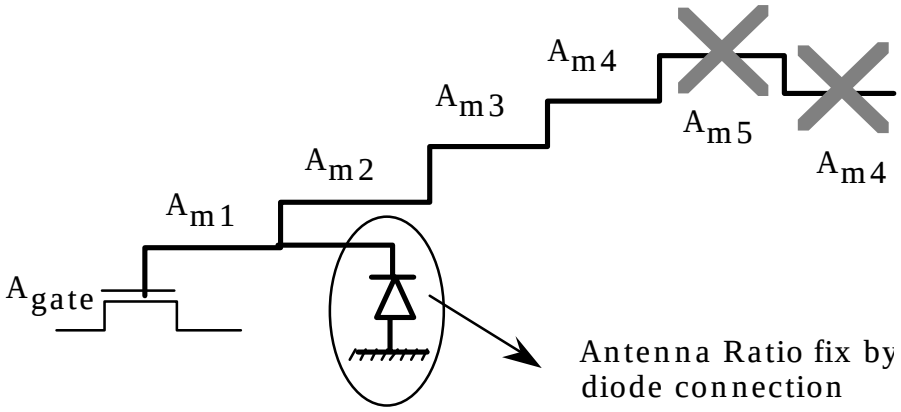
To be more efficient, such diode protection has to be connected to the gate and introduced at the metal 1 level if possible.

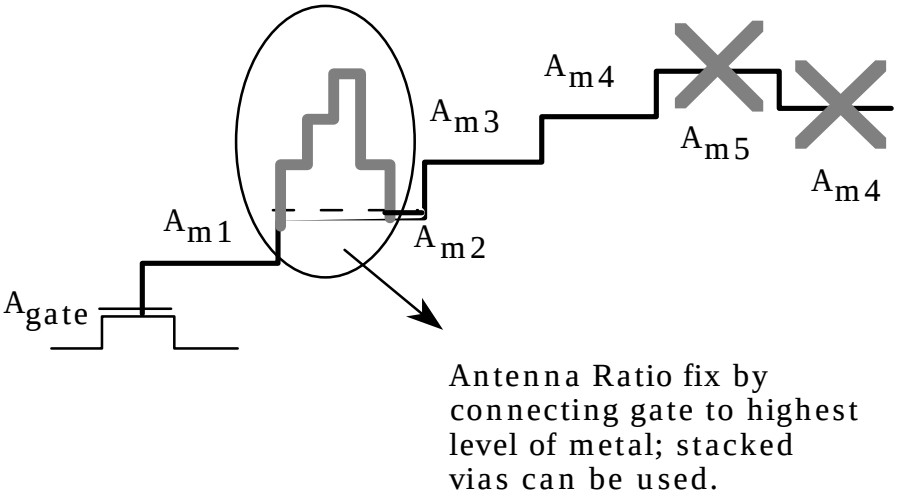
Any error detected at the DRC must be corrected using one of the following design solutions:

- connect directly the node to the output of the driver with a lower metal level and reduce the metal area
- connect the node to a diode; n^+ / p-well is preferred
- connect the gate to the highest metal level as close to the gate as possible; this metal 5 can then be routed using the other metal layers.

In cases where transistor matching is a concern, strong care has to be taken when designing the connection to the paired devices. In order to avoid mismatch between antenna ratio, metal lines must be as much symmetrical as possible. For the same reason, the connection lengths have to be minimized.

ANTENNA RATIO (fix methodologies)





11 ELECTRICAL DESIGN RULES

This section provides the designer with electrical design rules and process attributes that influence the electrical characteristics of a circuit.

11.1 Introduction

11.1.1 Only characterised devices are available for circuit. These devices are routinely monitored, the data of which is used to provide the electrical rules hereafter. Other devices than those specified are not allowed. If a designer wishes to use a device which is possible in the technology but is not characterised, then the Alcatel Microelectronics Technology Engineering Department must be consulted before the actual design of the product. Refer to section 5.2 for the list of available characterised devices.

11.1.2 All dimensions given in this section are as drawn dimensions on the IGS system.

11.1.3 All values of the parameters given hereafter are measured at room temperature (300K) unless specified otherwise.

11.1.4 All values of the parameters are valid for all device dimensions except where these dimensions are specified.

11.1.5 A brief description of the measurement conditions is given for each parameter. Refer to Alcatel Microelectronics specification GP10800 for the details of the measurement procedures.

11.1.6 IMPORTANT NOTE: all electrical parameters given for active transistors are given as indication only, and are a result of data collections performed on production lots fabricated in the Alcatel Microelectronics FAB II production facility. The correct values to be used for circuit design should be obtained from the C035M-D transistor model cards. The measurements of electrical parameters are performed on the test structures present in the scribe lane inserts, or on dedicated test structures.

11.1.7 Temperature Coefficients

All temperatures are in Kelvin. All formulas given below are valid over the temperature range from 218K to 423K (-55C to 150C).

MOS Threshold Voltage ($V_t(0)$)

$$V_t(0)(T) = V_t(0)(300) + TC_{Vt(0)} \times (T - 300)$$

MOS Linear Transconductance (β_{lin})

$$Log[\beta_{lin}(T)/\beta_{lin}(300)] = A\beta_{lin} + TC\beta_{lin} \times Log[T/300]$$

MOS Saturation Current (I_{dsat})

$$I_{dsat}(T) = I_{dsat}(300) \times [1 + TCIY \times (T - 300)]$$

Sheet Resistance (ρ_S)

$$\rho_s(T) = \rho_{s(}300) \times [1 + TC_L \times (T\text{-}300) + TC_Q \times (T\text{-}300)^2]$$

11.1.8 Diode Leakage

Diode leakage is given as the sum of two components: area leakage and periphery leakage:

$$I_{leak} = T_a \times \text{diode area} + I_p \times \text{diode periphery}$$

I_a and I_p are characterised at 30C, 85C and 150C.

11.1.9 Junction Capacitance

Junction capacitance as a function of reverse bias is given by:

$$C(V) = C(0) / [1 + V/P_b]^{Mj}$$

where:
- $C(V)$ = junction capacitance under reverse bias
- $C(0)$ = zero bias junction capacitance
- V = applied reverse bias voltage
- P_b = built in potential
- M_j = capacitance gradient factor

11.2 NMOS Transistors - Electrical Parameters

11.2.1 Wide/Long Transistor: W = 10 µm, L = 10 µm

Device W/L	Parameter	Unit	Low	Typical	High	Condition
Nch10/10	$V_t(0)$	V	0.52	0.60	0.68	V_{ds} = 100 mV V_{bs} = 0 V
Nch10/10	BVDS	V	7			V_{gs} = 0 V, V_{bs} = 0 V V_{ds} @ I_{ds} = 1 µA
Nch10/10	TC [$V_t(0)$]	mV/C		-1.1		V_{ds} = 100 mV V_{bs} = 0 V
Nch10/10	TC [β_{lin}]	N/A		-1.85		V_{ds} = 100 mV V_{bs} = 0 V
Nch10/10	TC [I_{dsat}]	%/C		-0.36		V_{gs} = V_{ds} = 3.3 V V_{bs} = 0 V

11.2.2 Wide/Short Transistor: W = 10 µm, L = 0.35 µm

Device W/L	Parameter	Unit	Low	Typical	High	Condition
Nch10/0.35	$V_t(0)$	V		0.59		V_{ds} = 100 mV V_{bs} = 0 V
Nch10/0.35	I_{dsat}/W	µA/µm	455	530	650	V_{gs} = V_{ds} = 3.3 V V_{bs} = 0 V
Nch10/0.35	BVDS	V	7			V_{gs} = 0 V, V_{bs} = 0 V V_{ds} @ I_{ds} = 1 µA
Nch10/0.35	I_{leak}/W	pA/µm		1	20	V_{ds} = V_{dmax} = 3.63 V V_{gs} = 0 V I_{ds} measured @ source
Nch10/0.35	TC [$V_t(0)$]	mV/C		-1.0		V_{ds} = 100 mV V_{bs} = 0 V
Nch10/0.35	TC [β_{lin}]	N/A		-1.6		V_{ds} = 100 mV V_{bs} = 0 V
Nch10/0.35	TC [I_{dsat}]	%/C		-0.16		V_{gs} = V_{ds} = 3.3 V V_{bs} = 0 V

11.3 PMOS Transistors - Electrical Parameters

11.3.1 Wide/Long Transistor: W = 10 µm, L = 10 µm

Device W/L	Parameter	Unit	Low	Typical	High	Condition
Pch10/10	$V_t(0)$	V	-0.69	-0.60	-0.51	V_{ds} = -100 mV V_{bs} = 0 V
Pch10/10	BVDS	V			-7	V_{gs} = 0 V, V_{bs} = 0 V V_{ds} @ I_{ds} = -1 µA
Pch10/10	TC [$V_t(0)$]	mV/C		+ 1.0		V_{ds} = -100 mV V_{bs} = 0 V
Pch10/10	TC [β_{lin}]	N/A		-1.2		V_{ds} = -100 mV V_{bs} = 0 V
Pch10/10	TC [I_{dsat}]	%/C		-0.2		V_{gs} = V_{ds} = -3.3 V V_{bs} = 0 V

11.3.2 Wide/Short Transistor: W = 10 µm, L = 0.35 µm

Device W/L	Parameter	Unit	Low	Typical	High	Condition
Pch10/0.35	$V_t(0)$	V		-0.57		V_{ds} = -100 mV V_{bs} = 0 V
Pch10/0.35	I_{dsat}/W	µA/µm	-300	-250	-200	V_{gs} = V_{ds} = -3.3 V V_{bs} = 0 V
Pch10/0.35	BVDS	V			-7	V_{gs} = 0 V, V_{bs} = 0 V V_{ds} @ I_{ds} = -1 µA
Pch10/0.35	I_{leak}/W	pA/µm	-20	-1		V_{ds} = V_{dmax} = 3.63 V V_{gs} = 0 V I_{ds} measured @ source
Pch10/0.35	TC [$V_t(0)$]	mV/C		+ 1.0		V_{ds} = -100 mV V_{bs} = 0 V
Pch10/0.35	TC [β_{lin}]	N/A		-1.1		V_{ds} = -100 mV V_{bs} = 0 V
Pch10/0.35	TC [I_{dsat}]	%/C		-0.11		V_{gs} = V_{ds} = -3.3 V V_{bs} = 0 V

11.4 Parasitic Transistors

Parasitic transistors are designed as finger structures with minimum active area spacing.

Device	Parameter	Unit	Low	High	Condition
NField Poly Gate	V_{gsat}	V	7		V_{ds} = 6 V Ramp V_{gs} V_{gsat} = V_{gs} @ 1 µA
NField Poly Gate	I_{leak}	pA/µm		1.0	V_{ds} = V_{gs} = Vd_{max} = 3.63 V V_{bs} = 0 V
PField Poly Gate	V_{gsat}	V		-7	V_{ds} = -6 V Ramp V_{gs} V_{gsat} = V_{gs} @ -1 µA
PField Poly Gate	I_{leak}	pA/µm	-1.0		V_{ds} = V_{gs} = Vd_{max} = -3.63 V V_{bs} = 0 V
NField Metal Gate	V_{gsat}	V	7		V_{ds} = 6 V Ramp V_{gs} V_{gsat} = V_{gs} @ -1 µA
NField Metal Gate	I_{leak}	pA/µm		1.0	V_{ds} = V_{gs} = Vd_{max} = 3.63 V V_{bs} = 0 V
PField Metal Gate	V_{gsat}	V		-7	V_{ds} = -6 V Ramp V_{gs} V_{gsat} = V_{gs} @ -1 µA
PField Metal Gate	I_{leak}	pA/µm	-1.0		V_{ds} = V_{gs} = Vd_{max} = -3.63 V V_{bs} = 0 V

11.5 Resistors

11.5.1 Resistance Values

Device	Parameter	Unit	Low	Typical	High	Condition
N-well Under Field	ρ_S	kΩ/sq	1.15	1.35	1.55	I = 10 µA/µm
n^+ active salicided	ρ_S	Ω/sq	1.5	2.7	4.0	I = 1 mA/µm
p^+ active salicided	ρ_S	Ω/sq	1.5	2.4	4.0	I = 1 mA/µm
n^+ polycide on field oxide	ρ_S	Ω/sq	1.0	2.2	4.0	I = 1 mA/µm
p^+ polycide on field oxide	ρ_S	Ω/sq	1.5	2.5	5.0	I = 1 mA/µm
n^+ active unsalicided	ρ_S	Ω/sq	40	50	60	I = 100 µA/µm
p^+ active unsalicided	ρ_S	Ω/sq	50	70	90	I = 100 µA/µm
n^+ poly unsalicided	ρ_S	Ω/sq	110	150	190	I = 200 µA/µm
p^+ poly unsalicided	ρ_S	Ω/sq	80	120	160	I = 100 µA/µm
metal 1	ρ_S	mΩ/sq	57	72	87	See note[1]
metal 2,3,4	ρ_S	mΩ/sq	44	55	66	See note[1]
metal 5	ρ_S	mΩ/sq	27	34	39	See note[1]

[1] Measurements are made for process control purposes and are to some extent structure-dependent.

11.5.2 Temperature Coefficients of Resistance's

Measurements were made on resistors with W in the range 8 - 10 microns at 2V bias over a temperature range 30 – 150°C

Device	Parameter	Unit	Typical
nwell	TC_L	ppm/C	3700
	TC_Q	ppm/C^2	8.1
n^+ active unsalicided	TC_L	ppm/C	1460
	TC_Q	ppm/C^2	0.5
p^+ active unsalicided	TC_L	ppm/C	1820
	TC_Q	ppm/C^2	0
n^+ poly unsalicided	TC_L	ppm/C	-1040
	TC_Q	ppm/C^2	2.6
p^+ poly unsalicided	TC_L	ppm/C	830
	TC_Q	ppm/C^2	0.6

11.6 Contact Resistance's

Device	Parameter	Unit	Low	Typical	High	Condition
n^+ active	R_c	Ω/ct	1.5	4.5	12.0	I = 20 µA/contact
p^+ active	R_c	Ω/ct	2.5	5.5	12.0	I = 20 µA/contact
n^+ poly	R_c	Ω/ct	3.0	5.5	12.0	I = 20 µA/contact
p^+ poly	R_c	Ω/ct	3.0	6.5	12.0	I = 20 µA/contact
via 1	R_c	Ω/via	0.4	1.5	4.0	I = 0.2 mA/via
via 2	R_c	Ω/via	0.4	1.5	4.0	I = 0.2 mA/via
via 3	R_c	Ω/via	0.4	1.5	4.0	I = 0.2 mA/via
via 4	R_c	Ω/via	0.4	1.5	4.0	I = 0.2 mA/via

11.7 Gate Oxide and Junction Capacitance's

11.7.1 Gate Oxide Capacitance's

Device	Parameter	Unit	Low	Typical	High	Condition
Nchannel Gate Oxide	T_{ox}	nm	6.3	7.0	7.7	optical meassurement
		nm		7.4		calculated from C_{plate}
	Cplate	F/m		4.66E-3		V = 4 V
	VBD	V	7			I = 1 mA/cm2
Pchannel Gate Oxide	T_{ox}	nm	6.3	7.0	7.4	optical measurement
		nm		7.4		calculated from C_{plate}
	Cplate	F/m		4.66E-3		V = 4 V
	VBD	V	7		-	I = 1 mA/cm2

11.7.2 Junction Capacitance's

Device	Parameter	Unit	Typical	Condition
n^+ / p-well	Cj	F/m2	9.33E-4	V = 0 V
	Mj		0.37	fitted
	Cjsw	F/m	2.99E-10	V = 0 V
	Mjsw		0.21	fitted
	Pb		0.80	fitted
	Cjc	F/m	2.09E-10	V = 0 V
p^+ / n-well	Cj	F/m2	1.33E-3	V = 0 V
	Mj		0.43	fitted
	Cjsw	F/m	3.15E-10	V = 0 V
	Mjsw		0.33	fitted
	Pb		0.80	fitted
	Cjc	F/m	1.86E-10	V = 0 V
n-well/ p-substrate	Cj	F/m2	2.31E-4	V = 0 V
	Mj		0.218	fitted
	Cjsw	F/m	2.55E-10	V = 0 V
	Mjsw		0.205	fitted
	Pb			fitted

11.8 Interconnect Capacitance's

Interconnect capacitances are calculated from the dielectric and conductor thicknesses.

11.8.1 Dielectric Thicknesses

For a planarised technology the dielectric thickness varies depending upon the layout and conductor density. For example: the metal 2 to metal 1 oxide thickness is less for an isolated metal 1 line than for an array of metal 1 lines.

The dielectric thicknesses given in the table below correspond to the most probable conditions: thickness over an array of lines at minimum spacing.

To avoid unrealistically pessimistic worst cases, for capacitance calculations the process spread on these dielectric thicknesses may be set to ± 10%.

Description	Unit	Typical
Poly - well	µm	0.380
Metal 1 - active	µm	1.250
Metal 1 - poly	µm	0.800
Metal 1 - well	µm	1.450
Metal 2 - active	µm	2.750
Metal 2 - poly	µm	2.300
Metal 2 - well	µm	2.950
Metal 2 - metal 1	µm	0.900

Dielectric Thicknesses (continued)

Description	Unit	Typical
Metal 3 - active	µm	4.370
Metal 3 - poly	µm	3.920
Metal 3 - well	µm	4.570
Metal 3 - metal 1	µm	2.520
Metal 3 - metal 2	µm	0.900
Metal 4 - active	µm	5.990
Metal 4 - poly	µm	5.540
Metal 4 - well	µm	6.120
Metal 4 - metal 1	µm	4.140
Metal 4 - metal 2	µm	2.520
Metal 4 - metal 3	µm	0.900
Metal 5 - active	µm	7.610
Metal 5 - poly	µm	7.160
Metal 5 - well	µm	7.810
Metal 5 - metal 1	µm	5.760
Metal 5 - metal 2	µm	4.140
Metal 5 - metal 3	µm	2.520
Metal 5 - metal 4	µm	0.900

11.8.2 Conductor Thicknesses

The conductor thicknesses, as deposited, are as follows:

Layer	Unit	Minimum	Typical	Maximum
Poly	µm	0.225	0.250	0.275
Metal 1 total	µm	0.567	0.630	0.693
Ti/TiN glue layer	nm		20/80	
Al-alloy	µm		0.50	
Ti/TiN ARC [i]	nm		30	
Metal 2 total	µm	0.648	0.72	0.792
Ti/TiN glue layer	nm		20/80	
Al-alloy	µm		0.59	
Ti/TiN ARC	nm		30	
Metal 3 total	µm	0.648	0.72	0.792
Ti/TiN glue layer	nm		20/80	
Al-alloy	µm		0.59	
Ti/TiN ARC	nm		30	
Metal 4 total	µm	0.648	0.72	0.792
Ti/TiN glue layer	nm		20/80	
Al-alloy	µm		0.59	
Ti/TiN ARC	nm		30	
Metal 5 total	µm	0.918	1.020	1.122
Ti/TiN glue layer	nm		20/80	
Al-alloy	µm		0.89	
Ti/TiN ARC	nm		30	

[i] ARC = Anti Reflective Coating

11.8.3 Dielectric Permittivity

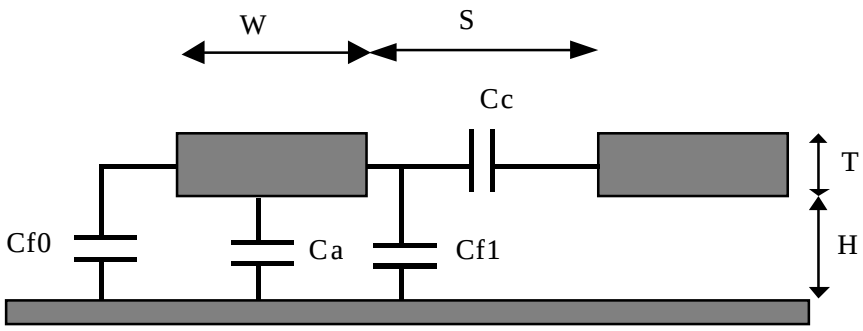
The physical nature of the different dielectrics used in the process can differ greatly from one process step to another. It is especially true for the isolation between transistors (locos, oxide thermally grown), and isolation between metal lines (a sandwich of gap filling oxide and PECVD oxide).

The relative dielectric permittivities to be used are summarized in the table below.

Layer	Unit	Minimum	Typical	Maximum
LOCOS	N/A	3.8	3.9	4.0
Metal(i) to metal(i)	N/A	3.8	4.0	4.2
Metal(i) to metal(i+1)	N/A	3.8	4.1	4.4

11.8.4 Interconnect capacitance calculation

11.8.4.1 Schematic and description



W = conductor width
S = conductor spacing
T = conductor thickness
H = dielectric thickness
C = total capacitance per unit length
C_a = area capacitance
C_f0 = fringing capacitance to underlying conductor for single line
C_f1 = fringing capacitance to underlying conductor in case of adjacent line
C_c = coupling capacitance in case of adjacent line

11.8.4.2 Capacitance calculation

a) case of single line:

$$C = W * C_a + 2 * C_f0$$

b) case of two lines

$$C = W * C_a + C_f0 + C_f1 + C_c$$

c) case of three lines

$$C = W * C_a + 2 * C_f1 + 2 * C_c$$

In the following tables, C_c is given for the minimum spacing, corresponding to the worst case.

11.8.4.3 Strategy

The strategy for determining typical, minimum and maximum interconnect capacitance's is illustrated in the table below

Case	H	T	W	S
Typical	Typical	Typical	Typical	Typical
Minimum	Maximum	Minimum	Minimum	Maximum
Maximum	Minimum	Maximum	Maximum	Minimum

11.8.5 Interconnect capacitance's

11.8.5.1 Typical interconnect capacitance's

Structure	C_a [fF/µm^2]	C_f0 [fF/µm]	C_f1 [fF/µm]	C_c [fF/µm]
Poly - well	0.0909	0.0464	0.0208	0.0363
Metal 1 - active	0.0276	0.0421	0.0082	0.0663
Metal 1 - poly	0.0432	0.0470	0.0134	0.0628
Metal 1 - well	0.0238	0.0406	0.0069	0.0671
Metal 2 - active	0.0126	0.0366	0.0038	0.0701
Metal 2 - poly	0.0150	0.0381	0.0048	0.0699
Metal 2 - well	0.0117	0.0360	0.0035	0.0701
Metal 2 - Metal 1	0.0384	0.0480	0.0141	0.0640
Metal 3 - active	0.0079	0.0328	0.0021	0.0688
Metal 3 - poly	0.0088	0.0336	0.0024	0.0694
Metal 3 - well	0.0076	0.0325	0.0020	0.0685
Metal 3 - Metal 1	0.0137	0.0373	0.0043	0.0701
Metal 3 - Metal 2	0.0384	0.0480	0.0141	0.0640

11.8.5.2 Typical interconnect capacitance's (continued)

Structure	C_a [fF/µm^2]	C_f0 [fF/µm]	C_f1 [fF/µm]	C_c [fF/µm]
Metal 4 - active	0.0058	0.0305	0.0013	0.0657
Metal 4 - poly	0.0062	0.0311	0.0015	0.0666
Metal 4 - well	0.0056	0.0303	0.0013	0.0652
Metal 4 - Metal 1	0.0081	0.0332	0.0022	0.0691
Metal 4 - Metal 2	0.0137	0.0373	0.0043	0.0701
Metal 4 - Metal 3	0.0384	0.0480	0.0141	0.0640
Metal 5 - active	0.0045	0.0312	0.0034	0.0423
Metal 5 - poly	0.0048	0.0317	0.0036	0.0426
Metal 5 - well	0.0044	0.0310	0.0033	0.0421
Metal 5 - Metal 1	0.0060	0.0333	0.0048	0.0433
Metal 5 - Metal 2	0.0081	0.0359	0.0070	0.0435
Metal 5 - Metal 3	0.0137	0.0404	0.0120	0.0419
Metal 5 - Metal 4	0.0384	0.0520	0.0292	0.0334

11.8.5.3 Minimum interconnect capacitance's

Structure	C_a [$fF/\mu m^2$]	C_f0 [$fF/\mu m$]	C_f1 [$fF/\mu m$]	C_c [$fF/\mu m$]
Poly - well	0.0826	0.0441	0.0198	0.0329
Metal 1 - active	0.0251	0.0401	0.0078	0.0581
Metal 1 - poly	0.0392	0.0447	0.0127	0.0554
Metal 1 - well	0.0216	0.0387	0.0066	0.0586
Metal 2 - active	0.0114	0.0349	0.0036	0.0603
Metal 2 - poly	0.0136	0.0364	0.0046	0.0604
Metal 2 - well	0.0106	0.0343	0.0033	0.0601
Metal 2 - Metal 1	0.0349	0.0457	0.0134	0.0564
Metal 3 - active	0.0072	0.0313	0.0020	0.0579
Metal 3 - poly	0.0080	0.0321	0.0023	0.0587
Metal 3 - well	0.0069	0.0310	0.0019	0.0574
Metal 3 - Metal 1	0.0125	0.0356	0.0041	0.0604
Metal 3 - Metal 2	0.0349	0.0457	0.0134	0.0564

11.8.5.4 Minimum interconnect capacitance's (continued)

Structure	C_a [$fF/\mu m^2$]	C_f0 [$fF/\mu m$]	C_f1 [$fF/\mu m$]	C_c [$fF/\mu m$]
Metal 4 - active	0.0052	0.0291	0.0013	0.0540
Metal 4 - poly	0.0057	0.0297	0.0014	0.0552
Metal 4 - well	0.0051	0.0289	0.0012	0.0535
Metal 4 - Metal 1	0.0076	0.0317	0.0021	0.0581
Metal 4 - Metal 2	0.0125	0.0356	0.0041	0.0604
Metal 4 - Metal 3	0.0349	0.0457	0.0134	0.0564
Metal 5 - active	0.0040	0.0296	0.0031	0.0369
Metal 5 - poly	0.0044	0.0302	0.0035	0.0375
Metal 5 - well	0.0041	0.0298	0.0032	0.0371
Metal 5 - Metal 1	0.0055	0.0318	0.0045	0.0384
Metal 5 - Metal 2	0.0076	0.0343	0.0067	0.0388
Metal 5 - Metal 3	0.0125	0.0385	0.0115	0.0378
Metal 5 - Metal 4	0.0349	0.0494	0.0278	0.0302

11.8.5.5 Maximum interconnect capacitance's

Structure	C_a [$fF/\mu m^2$]	C_f0 [$fF/\mu m$]	C_f1 [$fF/\mu m$]	C_c [$fF/\mu m$]
Poly - well	0.1010	0.0490	0.0220	0.0403
Metal 1 - active	0.0307	0.0442	0.0086	0.0762
Metal 1 - poly	0.0480	0.0494	0.0141	0.0716
Metal 1 - well	0.0265	0.0426	0.0072	0.0774
Metal 2 - active	0.0140	0.0381	0.0040	0.0820
Metal 2 - poly	0.0167	0.0400	0.0050	0.0813
Metal 2 - well	0.0130	0.0377	0.0036	0.0822
Metal 2 - Metal 1	0.0426	0.0506	0.0148	0.0730
Metal 3 - active	0.0088	0.0344	0.0022	0.0820
Metal 3 - poly	0.0098	0.0353	0.0025	0.0823
Metal 3 - well	0.0084	0.0340	0.0020	0.0818
Metal 3 - Metal 1	0.0152	0.0392	0.0045	0.0817
Metal 3 - Metal 2	0.0426	0.0506	0.0148	0.0730

11.8.5.6 Maximum interconnect capacitance's (continued)

Structure	C_a [fF/µm^2]	C_f0 [fF/µm]	C_f1 [fF/µm]	C_c [fF/µm]
Metal 4 - active	0.0064	0.0320	0.0014	0.0799
Metal 4 - poly	0.0069	0.0325	0.0016	0.0806
Metal 4 - well	0.0062	0.0317	0.0013	0.0795
Metal 4 - Metal 1	0.0093	0.0348	0.0023	0.0822
Metal 4 - Metal 2	0.0152	0.0392	0.0045	0.0817
Metal 4 - Metal 3	0.0426	0.0506	0.0148	0.0730
Metal 5 - active	0.0050	0.0327	0.0035	0.0484
Metal 5 - poly	0.0054	0.0331	0.0038	0.0486
Metal 5 - well	0.0049	0.0325	0.0034	0.0483
Metal 5 - Metal 1	0.0067	0.0349	0.0050	0.0491
Metal 5 - Metal 2	0.0093	0.0376	0.0074	0.0489
Metal 5 - Metal 3	0.0152	0.0424	0.0126	0.0486
Metal 5 - Metal 4	0.0426	0.0548	0.0308	0.0371

11.9 Junction Diodes

11.9.1 N^+ Diodes to p-well

Parameter	Unit	Low	Typical	Condition
|VBD|	V	7.0	9.5	V @ I = 1 µA
I_a (T = 30°C)	pA/µm^2		1.2E-5	V = V_{max} = 3.63 V
I_a (T = 80°C)	pA/µm^2		2.5E-4	V = V_{max} = 3.63 V
I_a (T = 150°C)	pA/µm^2		5.6E-2	V = V_{max} = 3.63 V
I_p (T = 30°C)	pA/µm		5.8E-5	V = V_{max} = 3.63 V
I_p (T = 80°C)	pA/µm		7.7E-4	V = V_{max} = 3.63 V
I_p (T = 150°C)	pA/µm		2.8E-2	V = V_{max} = 3.63 V

11.9.2 P^+ Diodes to n-well

Parameter	Unit	Low	Typical	Condition
|VBD|	V	7	10.0	V @ I = 1 µA
I_a (T = 30°C)	pA/µm^2		8.1E-5	V = V_{max} = -3.63 V
I_a (T = 80°C)	pA/µm^2		4.6E-4	V = V_{max} = -3.63 V
I_a (T = 150°C)	pA/µm^2		2.0E-1	V = V_{max} = -3.63 V
I_p (T = 30°C)	pA/µm		3.5E-4	V = V_{max} = -3.63 V
I_p (T = 80°C)	pA/µm		3.3E-3	V = V_{max} = -3.63 V
I_p (T = 150°C)	pA/µm		6.4E-2	V = V_{max} = -3.63 V

11.9.3 N-well to p-well

Parameter	Unit	Low	Typical	High	Condition
I_a (T = 30°C)	pA/µm^2		4.2E-6		V = V_{max} = 3.63 V
I_a (T = 80°C)	pA/µm^2		6.8E-5		V = V_{max} = 3.63 V
I_a (T = 150°C)	pA/µm^2		2.7E-2		V = V_{max} = 3.63 V
I_p (T = 30°C)	pA/µm		7.2E-5		V = V_{max} = 3.63 V
I_p (T = 80°C)	pA/µm		1.1E-3		V = V_{max} = 3.63 V
I_p (T = 150°C)	pA/µm		2.3E-1		V = V_{max} = 3.63 V

11.9.4 P+ Diodes to nldd

Parameter	Unit	Low	Typical	High	Condition
|VBD|	V	5.5	7.0	8.5	V @ I = 1 µA