Embedded System Design on Zynq using Vivado Workshop
ZYBO

COURSE DESCRIPTION

This workshop brings experienced FPGA designers up to speed on the capabilities and characteristics of the Xilinx Zynq All Programmable SoC family and Vivado design environment. Developing embedded systems using ARM Cortex-A9 processor and a set of soft peripherals is also included in the lectures and labs.

1. Install Xilinx software

Professors may submit the online donation request form at http://www.xilinx.com/member/xup/donation/request.htm to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

- Vivado 2015.2 System Edition

2. Setup hardware

Connect ZYBO

a. Set the power supply jumper to USB so the board can be powered up and laboratory assignments can be carried out using single micro-usb cable
b. Connect micro USB cable between PROG UART port of ZYBO and PC

3. Install distribution

Extract the **2015_2_zynq_sources.zip** file in the *c:\xup\embedded* directory. This will create a **2015_2_zynq_sources** folder. Create a *c:\xup\embedded\2015_2_zynq_labs* directory. This is where you will do the labs. The **2015_2_zynq_labdocs_pdf.zip** file consists of lab documents in the PDF format. Extract this zip file in *c:\xup\embedded* directory or any other directory of your choice.

Download the ZYBO.zip file and extract it in the **<Vivado_2015_2_install_dir>\Vivado\2015.2\data\boards\board_parts\zynq.** This directory is the board files directory and having it in the specified directory will allow you to select Zybo board during the design creation.

4. For Professors only

Download the **2015_2_zedboard_labsolution.zip** and **2015_2_zynq_docs_source.zip** files using your membership account. Do not distribute them to students or post them on a web site. The 2015_2_zynq_docs_source.zip file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

5. Get Started

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

COURSE AGENDA

Day 1 Agenda	Day 1 Materials
Class Intro	01_class_intro.pptx
Vivado Overview	11_Vivado_overview.ppt x
Lab 1: Basic Hardware Design	11a_lab1_intro.pptx Lab1.docx
Zynq Architecture	12_zynq_architecture.pptx
Extending Embedded System into PL	13_Extending_Embedded_System_into_PL.pptx
Lab 2: Adding IPs in PL	13a_lab2_intro.pptx Lab2.docx
Creating and Adding Custom IP	14_Creating_and_Adding_Custom_IP.pptx
Lab 3: Adding Custom IP in PL	14a_lab3_intro.pptx Lab3.docx
Day 2 Agenda	**Day 2 Materials**
Software Development Environment	21_ Software_Development_Environment.pptx
Lab 4: Writing Basic Software Application	21a_lab4_intro.pptx Lab4.docx
Software Development and Debug using SDK	22_Software_Development_and_Debug.pptx
Lab 5: Software Writing for Timer and Debugging	23a_lab5_into.pptx Lab5.docx

LAB DESCRIPTIONS

Lab 1 - Basic Hardware Design: Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
Lab 2 - Adding Peripherals in Programmable Logic: Extend the hardware system by adding AXI peripherals from the IP catalog.
Lab 3 - Creating and Adding Your Own Custom Peripheral: Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral.
Lab 4 - Writing Basic Software Application: Write a basic C application to access the peripherals.
Lab 5 - Software Writing for Timer and Debugging Using Software Development Kit (SDK): Use API to drive CPU's timer. Perform software debugging using SDK.

6. Contact XUP

Send an email to xup@xilinx.com for questions or comments