Low Power Digital Synthesis

Synopsys Design Compiler Tutorial

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The objective of this tutorial is to learn to optimise power consumption during digital synthesis.

Learning Outcomes:

At the end of this tutorial you should be able to:

1. Describe the principle of clock gating
2. Setup Design Compiler and define library files
3. Import hdl files into Design Compiler
4. Add design constraints
5. Optimise power consumption of your design
6. Analyse power consumption reports

1. Documentations

You will need the following documents to complete this tutorial

1. Lab instruction (this documents)
2. Hdl file (provided)

2. Create a directory for your design

a. Create a folder called lp and move into it (Linux commands are shown below)

```
mkdir lp

cd lp
```

b. Create a folder called src and copy your design files into it.

```
mkdir src
```

c. Create a folder called syn1 and move into it

```
mkdir syn1
```

d. Inside syn1, create a folder called work

```
mkdir work
```

e. Copy your hdl files into the syn directory

3. Setup Linux Environment in order to use DC

In order to setup your Linux environment in order to use Design Compiler you need to execute the following commands:

```
source /opt/esdcad/scripts/esd_tcshrc  (Do this once only).
```

```
source /opt/esdcad/scripts/synopsys_linux_coreTools_D-
2010.03
```

```
source /opt/esdcad/scripts/license
```

In order to run design vision you need to use the option gui as follows

```
dc_shell –gui
```

4. Setup the technology libraries

For the purpose of this tutorial a 90nm technology library from Synopsys are used. Type the following commands:

```
lappend search_path
/home/esdcad/designkits/synopsys/90/02192010_SAED_EDK90nm/SA
ED_EDK90nm/Digital_Standard_Cell_Library/synopsys/models
```

```
lappend search_path
/home/esdcad/designkits/synopsys/90/02192010_SAED_EDK90nm/SA
ED_EDK90nm/Digital_Standard_Cell_Library/synopsys/icons
```

```
set link_library {saed90nm_max.db saed90nm_typ.db
saed90nm_min.db}
```

```
set target_library saed90nm_max.db
```

```
set symbol_library
/home/esdcad/designkits/synopsys/90/02192010_SAED_EDK90nm/SA
ED_EDK90nm/Digital_Standard_Cell_Library/synopsys/icons/saed
90nm.sdb
```

5. Read and Synthesis an HDL Design

The basic synthesis flow is shown below:

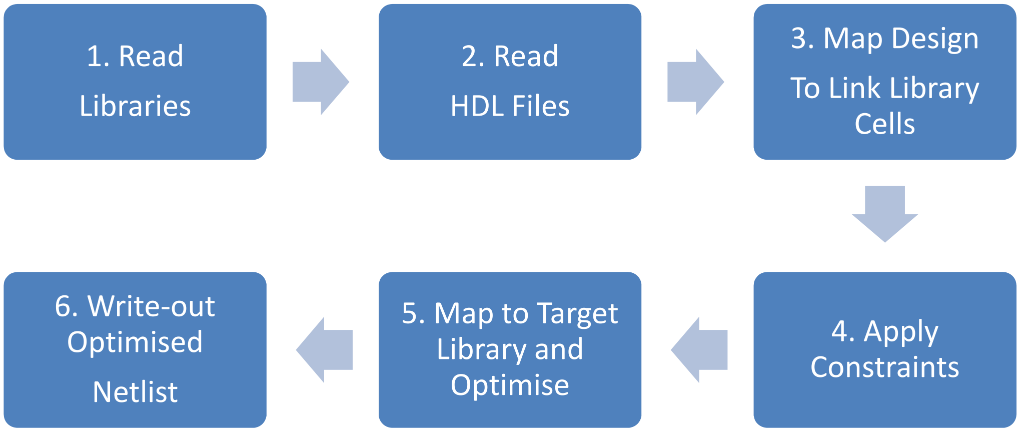
1. Read Libraries
2. Read HDL Files
3. Map Design To Link Library Cells
4. Apply Constraints
5. Map to Target Library and Optimise
6. Write-out Optimised Netlist

Figure 1: Synthesis Flow

Make sure you are in the syn directory; use the following commands to read your design into DC:

```
define_design_lib WORK -path work
analyze -work WORK -f sverilog RingCounter.sv
elaborate RingCounter
```

6. Setup Design Constraints

```
create_clock Clock –name clk -period 4
set_dont_touch_network clk
set_clock_latency 1 clk
set_clock_uncertainty 0.5 clk
set_dont_touch_network [get_ports Clock]
set_dont_touch_network [get_ports Reset]
```

7. Saving constraints

If you wish to save your constraints, which is probably a good idea, use:

```
write_sdc file.sdc
```

8. Implement without power optimization

Just type:

```
compile
```

after the design has compiled successfully we can estimate power consumption using the following commands:

```
report_power
```

Below is an extract of the power report

```
****************************************
Report : power
        -analysis_effort low
Design : RingCounter
Version: C-2009.06-SP4
Date   : Thu Nov 14 13:30:15 2013
****************************************


Library(s) Used:

    saed90nm_max (File:
/home/esdcad/designkits/synopsys/90/02192010_SAED_EDK90nm/SAED
_EDK90nm/Digital_Standard_Cell_Library/synopsys/models/saed90n
m_max.db)


Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
RingCounter            8000              saed90nm_max


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  56.9695 uW   (99%)
  Net Switching Power  = 839.6688 nW    (1%)
                         ---------
Total Dynamic Power    =  57.8091 uW  (100%)

Cell Leakage Power     =   1.9401 uW
```

It is also useful at this stage to record the area of the design, type

```
report_area
```

Below is the area report

```
****************************************
Report : area
Design : RingCounter
Version: C-2009.06-SP4
Date   : Thu Nov 14 14:00:54 2013
****************************************

Library(s) Used:

    saed90nm_max (File:
/home/esdcad/designkits/synopsys/90/02192010_SAED_EDK90nm/SAED
_EDK90nm/Digital_Standard_Cell_Library/synopsys/models/saed90n
m_max.db)

Number of ports:               21
Number of nets:                61
Number of cells:               42
Number of references:          11

Combinational area:        315.089005
Noncombinational area:     257.126003
Net Interconnect area:      23.950469

Total cell area:           572.215009
Total area:                596.165478
```

9. Set power constraints

Power optimization process is driven by power constraints; you can constrain dynamic and leakage power independently.

```
set_max_leakage_power 0 mw
set_max_dynamic_power 0 mw
```

10.Perform gate level power optimization

To do so, type the following command:

```
compile_ultra
```

after the design has compiled successfully we can estimate power consumption using the following commands:

```
report_power
```

Below is an extract of the power report

```
****************************************
Report : power
        -analysis_effort low
Design : RingCounter
Version: C-2009.06-SP4
Date   : Thu Nov 14 14:05:55 2013
****************************************

Library(s) Used:

    saed90nm_max (File:
/home/esdcad/designkits/synopsys/90/02192010_SAED_ED
K90nm/SAED_EDK90nm/Digital_Standard_Cell_Library/syn
opsys/models/saed90nm_max.db)


Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
RingCounter            8000
saed90nm_max


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T
units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  39.6335 uW   (98%)
  Net Switching Power  = 909.0126 nW    (2%)
                         ---------
Total Dynamic Power    =  40.5425 uW  (100%)

   Cell Leakage Power     =   2.3283 uW
```

Check how this optimization has affected the area of your design, by typing

```
report_area
```

Record the area values

Close down design vision and exit design compiler before you proceed to the next section.

11.Perform Optimization using Operand isolation and Clock gating

Design compiler can automatically insert clock gating and power optimization structure, however you need to enable these features prior to optimization. In order to compare the different power optimisation methods, we will need to start again from an RTL design. To do so you need to:

a. Create a new synthesis folder inside the lp directory, by typing :

```
mkdir syn2
```

b. move into syn2

c. Inside syn2, create a folder called work

```
mkdir work
```

d. Copy your hdl files into the syn1 directory
e. Start design compiler and setup design library as explain in section s 3 and 4
f. Read in the hdl design and apply timing constraints as explained in sections 5 and 6.
g. Set power constraints as explained in section 9
h. Enable operand isolation: Operand Optimization is performed during the standard compile process , however we need to enable this feature. To do so, you need to type:

```
set do_operand_isolation true
set_operand_isolation_style -logic adaptive -verbose
```

The option –adaptive in the above commend will allow the compile to choose between different implementation of the operand isolation (“and/or” or “latch” based) Operand isolation will now be performed during the next compile command.

i. Implement the design with clock gating:

```
compile –gate_clock
```

j. Analyse the design: the purpose of this step is analyse how successful the power optimization has been, and to review whether or not clock-gating elements have been inserted and to see if any operand isolation elements have been used. For this type:

```
report_clock_gating
```

Record the following value:

Number of Gated Register

Then type:

```
report_operand_isolation
```

Record the following value:

Number of isolation objects:

Then use the following command to estimate power consumption after optimization:

```
report_power
```

Below is an extract of the power report

```
****************************************
Report : power
        -analysis_effort low
Design : RingCounter
Version: C-2009.06-SP4
Date   : Thu Nov 14 13:33:27 2013
****************************************


Library(s) Used:

    saed90nm_max (File:
/home/esdcad/designkits/synopsys/90/02192010_SAED_EDK90nm
/SAED_EDK90nm/Digital_Standard_Cell_Library/synopsys/mode
ls/saed90nm_max.db)


Operating Conditions: WORST   Library: saed90nm_max
Wire Load Model Mode: enclosed

Design        Wire Load Model           Library
------------------------------------------------
```

```
RingCounter            8000             saed90nm_max
SNPS_CLOCK_GATE_HIGH_RingCounter_0
                       ForQA            saed90nm_max


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T
units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  33.3317 uW   (96%)
  Net Switching Power  =   1.4919 uW    (4%)
                         ---------
Total Dynamic Power    =  34.8236 uW  (100%)

Cell Leakage Power     =   2.8601 uW
```

By comparing the power consumption figures, it can be seen that dynamic power consumption has been reduced by around 60% in this case,

Notice that the leakage power has increased, Can you explain why?

Check how this optimization has affected the area of your design, by typing

```
report_area
```

Record the area values

12. Compare the area and power results using the different optimisation methods and answer the following questions:

1) Which of power optimization techniques has achieved the highest reduction in power?
2) How did power optimization affect the design area?