Digital Simulations

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Digital Simulation Lab Instructions

- In this lab, you will be simulating a digital design at different stages, namely:

1. Behavioural simulations
2. Post Synthesis simulations
3. Post Layout Simulations

Full instructions are given below

Digital Simulation Lab Instructions

For Behavioural simulation

1. HDL model of the design (qmults.v) (this is provided)
2. A test bench (test.v) (this is provided)

Behavioural Simulations

1. Create a working directory called BehaviouralSim.
2. Save the qmults HDL file and the test bench in this folder.
3. Open the test bench in a text editor and investigate it.
4. Set the clock period in the test to 2 ns.
5. Create a Modelsim Project.
6. Compile all files.
7. Run the simulations and verify the design function correctly.
8. Does the design simulate correctly if you reduce clock period to 0.5 ns? Why?.
9. Save a printout of your simulations.

Digital Simulation Lab Instructions

For post Synthesis simulation you will need:

1. A synthesised Verilog net list of the design (this is obtained from the synthesis stage)
2. A test bench (test.v) (this is provided)
3. Your timing constraints file “design.sdf” (this is obtained from the synthesis stage)
4. HDL models of all cells in technology library (this is provided)

Post Synthesis Simulations

1. Create a working directory called PostSynSim.
2. Save the qmults HDL file, the test bench, HDL models of the technology library and SDF timing file in this folder.
3. Open the test bench in a text editor and set the clock frequency in the test to your maximum achievable frequency (from the synthesis stage).
4. Open the SDF file in a text editor and comment out all lines that begin with the word "*Removal*".
5. Create a second Modelsim Project.
6. Compile all files.
7. Run the simulations and verify the design function correctly.
8. Does the design simulate correctly if you reduce clock period to 0.5 ns? Why?
9. Save a printout of your simulations.

Digital Simulation Lab Instructions

For post Layout simulation you will need:

1. Post layout netlist (this is obtained from the layout stage)
2. A test bench (this is provided)
3. Your timing constraints file “design.sdf” (this is obtained from the layout stage)
4. HDL models of all cells in technology library (this is provided)

Post Layout Simulations

1. Create a working directory called PostLaySim
2. Save the qmults HDL file, the test bench, HDL models of the technology library and SDF timing file in this folder.
3. Open the test bench in a text editor and set the clock frequency in the test to your maximum achievable frequency (from the synthesis stage).
4. Open the SDF file in a text editor and comment out all lines that begin with the word "*Removal*"
5. Create a third Modelsim Project
6. Compile all files
7. Run the simulations and verify the design function correctly.
8. Does the design simulate correctly if you reduce clock period to 0.5 ns? Why?
9. Save a printout of your simulations.