Extraction, LVS and Post-layout simulation

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Custom Design Flow



The post layout process

- So far we have worked through three steps in a typical full custom flow
- After layout there are a number of mandatory steps before fabrication
 - Layout versus schematic checks that the extracted layout netlist matches the schematic
 - Extract the layout, this time with parasitics
 - Post-layout simulation using the extracted (with parasitics) netlist



Learning Outcomes Outcomes

After completing this unit, you should be able to:

- Use layout versus schematic (LVS) tools
- Perform an extraction with parasitics
- Use the hierarchy editor
- Run a post-layout simulation

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Where we left off

- In the last lecture, you saw how to use Virtuoso to create a basic layout cell.
- Your layout much be free from all DRC errors before you do LVS checking
 Layout L Editing: Library1 Inverter_layout *_02 layout _____X
 Launch Elle Edit View Create Verify Connectivity Options Tools Window ** addence



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Extraction

- The extraction tool is invoked from within the Layout window
- This bring up the extract form (Run Assura LVS)

2	Run Assura LVS
Schematic Design Sc	urce DFII 🔽 Use Existing Netlist 🗌 Netlisting Options
Library Library1	Cell nverter_layout_02 View schematic Browse
Layout Design Sourc	e DFII 🔽 Use Existing Extracted Netlist
Library Library1	Cell nverter_layout_02 View layout Browse
Run Name 🛛 🕶 rerter	:_layout_02 Run Directory ./Assura
Run Location	local
View Rules Files	Technology C35b4 Rule Set default
Extract Rules	s/ams/v400/assura/c35b4/c35b4/extract.rul View Reloa
Compare Rules	bsignkits/ams/v400/assura/c35b4/c35b4/compare.rul View
Switch Names	resimulate_extracted Set Switches
Binding File(s)	l/designkits/ams/v400/assura/c35b4/c35b4/bind.rul View
RSF Include	nkits/ams/v400/assura/c35b4/c35b4/LVSinclude.rsf View
Variable	Value Default Description
None 🔽	
View avParameters	Modify avParameters 2 avParameters are set.
View avCompareRule	28 Modify avCompareRules 13 avCompare rules are set.
View Additional Fund	ctions 🗌 No additional functions are set.
ОК	Cancel Apply Defaults Load State Save State View RSF Helt





Layout versus schematic (LVS)

- Layout versus schematic compares the extracted netlist to the schematic
- You can invoke the LVS tool from the Layout view window

Ass <u>u</u> ra	QRC	Opti <u>m</u> ize	<u>H</u> e
Open	Bun		
Open	Cell		
Techr	nology.		
R <u>u</u> le :	Sets		
<u>S</u> etup			•
Run <u>E</u>	<u>)</u> RC		
Run <u>a</u>	ltPSM.		
Run <u>L</u>	VS		
Run <u>E</u>	RC		
Open	<u>E</u> LW		
Open	<u>V</u> LW		
LVSI	Debug	Env	
Vjew	Netlist.		
LVS E	Err <u>o</u> r Re	eport	
<u>P</u> robir	ng		
S <u>h</u> ort	Locato	r	
ERC I	Browse	r	
Run G	RC		
Close	Ru <u>n</u>		
Subst	rate AC	C Analysis.	



Layout versus schematic (LVS)

- Here we will perform the circuit extraction, that is, all the parasitics resulting the layout of the devices (capacitances, diodes, and other components that can exist due to the interaction between different layers). The layout view will also be compared with the schematic (Layout versus Schematic, or simply LVS)
- Without any DRC error, select Assura → Run LVS. In the main form press Set Switches, select the resimulate_extracted option and press OK. This ensures the use of this LVS run for RCX.

Running the LVS check

		Schematic Design So	ource DFII 🔽 Use Existing Natlist
	In the <i>RUN Assura LVS</i> window:	Library Library	Coll marting lower Provide Brown
1.	The Cell name should be the same as your Run name.	Lavout Design Source	
2.	Technology should be chosen by c35b4.	Library Library1	Cell nverter_layout_02 View layout Brow
3.	The extract rule should be:	Ra Name verter	r_layout_02 Run Dectory ./Assura
/hoi	me/esdcad/designkits/ams/v400/assura/c35b4/c35b4/extract.rul	Run Location	local
4.	The Compare rules should be home/designkits/ams/v400/assura/c35b4/c35b4/compare.rul	View Rules Files	Technology C35b4 Rule Set default :s/ams/v400/assura/c35b4/c35b4/extract.rul View
5.	The binding files should be /home/esdcad/designkits/ams/v400/assura/c35b4/c35b4/bind.rul	Compare Rules Switch Names	ssignkits/ams/v400/assura/c35b4/c35b4/compare.rul View resimulate_extracted Set Switches
6.	RSF include should be	 Binding File(s) RSF Include 	1/designkits/ams/v400/assura/c35b4/c35b4/LVSinclude.rsf View
/hoi	me/esdcad/designkits/ams/v400/assura/c35b4/c35b4/LVSinclude.rsf	Variable None	Value Default Description
7.	Select the switches option <i>resimulate_extracted</i> to ensure ensures the use of this LVS run for RCX.	View avParameters	Modify avParameters 2 avParameters are set.
		View avCompareRule	es 🗌 Modify avCompareRules 13 avCompare rules are set.
		View Additional Func	ctions 🔲 No additional functions are set.

Run Assura LVS

OK Cancel Apply

Defaults | Load State

Save State

Help

х

Browse.

Browse..

Reload

Set Switches

View RSF

Layout versus schematic (LVS)

In the main form press OK to start LVS. Then you will see the progress window.

E F	Progress X				
Assura LVS Run in progress					
Run Name:	inverter_layout_02				
Run Dir:	./Assura				
Process Id:	16477 (ipc:15)				
Start Time:	Mar 4 15:00:49 2015				
Stop Run					
Watch Log F	ile				
OK	Cancel Help				

Checking the LVS output

If there is nothing wrong, you will receive this message.

	Run: "inverter_layout_02"
	Run: "inverter_layout_02" from /home/tz1g12/6097/zty_demo_new_cadence/Assura
	Schematic and Layout Match. You currently have an open run (project).
	Do you want to close current project and view the results of new run?
	Summary of LVS Issues
/ %	Extraction Information:
~	O cells have O mal-formed device problems O cells have O label short problems O cells have O label open problems
	Comparison Information:
	0 cells have 0 Net mismatches
	0 cells have 0 Device mismatches
	o cells have o Parameter mismatches
	Yes No Help

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Layout versus schematic (LVS)

Click Yes. You will see the Schematic and Layout Match.

LVS Debug - inverter_layout_02	
File View Options Tools <u>H</u> elp	cādence
Cell List (sch lay)	Summary (sch lay)
*** Schematic and Layout Match	
Open Schematic Cell Open Layout Cell	Open Tool
13	

- In our case you should get at least one error the terminals don't all match
- Reading further on, it is clear that the problem is with the Z terminal in the layout
- Clearly, I have labelled the output Z in the layout and Y in the schematic – an easy fix.

Typical LVS errors

So of you have LVS errors you will receive the following message which lists all errors. Click ok to go to Debug Window

	Run: "inverter_layout_02" has completed SUCCESSFULLY!
DeviceTyp	Device
1 110	avn70 ⁻¹
1 devices	filtered
The L∀S ru	m "inverter_layout_02" has completed successfully.
Compare pr	roblems were detected in 1 cells.
1 cells	s had pins mismatches.
0 cells	s matched
No Extract	tion Problems were detected.
You curren	ntly have an open run (project).
Press "OK"	' to close this run and enter the LVS Debug Environment.
Press "Can	ncel" to leave this run open and close this Dialog box.
LVS Run "i	inverter_layout_02"
is located	d in /home/tz1g12/6097/zty_demo_new_cadence/Assura
-	
	Prev. Error Prev. Warn. Next Warn. Next Error
MARNING	(ANTINENDI 10050) , mean and a call income Marrie , not found
WARNING	(AVLVSNN-10050) : mosDevice - cell 'PMOSNL_WAFFLE' not found.
WARNING	(AVLVSNN-10050) : mosDevice - cell 'NMOSML_WAFFLE' not found.
WARNING	(AVLVSNN-10050) : mosDevice - cell 'NMOSL_WAFFLE' not found.
WARNING	(AVLVSNN-10050) : mosDevice - cell 'PMOSM_WAFFLE' not found.
WARNING	(AVLVSNN-10050) : mosDevice - cell 'PMOS_WAFFLE' not found.
WARNING	(AVLVENN-10050) : mosDevice - cell 'NMUSM WAFFLE' not found.
WARNING	(AVLVSNR-10050) : MUSDEVICE - CEII NNUS WAFFLE NOC FOUND.
WAENING	(AVLVSNN-IUUSU) : MOSDEVICE - CELL 'PMUSML_WARFLE' not found.
C.C.	
n	
r	OK Cancel / Hr

15

Typical LVS errors

LVS Debug Window gives more details on each error in the summary box

Double click the Pins

LVS Debug - inverter_layout_02	_ _ ×
File View Options Tools <u>H</u> elp	cādence
Cell List (sch lay) 💿 Extract 💿 Compare	Summary (sch lay)
inverter_layout_02{Library1} inverter_layout_02{Libra	Rewires O Nets O Devices O Pins 1 1 Parameters O
Open Schematic Cell Open Layout Cell	Open Tool

Typical LVS errors

You can find the mismatch detail and fix it.

Č F	ins Mismatch Tool	
File Options View Tools	<u>H</u> elp	cādence
Sch Lay Cells inverter_ Message Unbound Pin	layout_02{Library1} in	verter_layout_02{Librar
Schematic Info (/)	Layout Info (/))
Name	Name	
Y Probe Zoom	Remove Probe	Zoom Remove
16 HelpAction		

Learning Outcomes Outcomes

After completing this unit, you should be able to:

- Use layout versus schematic (LVS) tools
- Perform an extraction with parasitics
- Use the hierarchy editor
- Run a post-layout simulation

- You need to ensure that your design is free LVS errors you can proceed with the extraction b
- The extraction tool is invoked from within the Layout window: as follows: Assura → Run QRC and to choose Extraction tab.
- For the reference node (Ref Node) write gnd!. Proceed with OK.

Ass<u>u</u>ra QRC Opti<u>m</u>ize Open Run... Open Cell... Technology... Rule Sets... Setup Run DRC... Run altPSM... Run LVS... Run ERC ... Open ELW Open VLW LVS Debug Env... Open Schematic Cell... LVS Error Report... Probing... Short Locator... ERC Browser... Run QRC.. Close Run Substrate AC Analysis...

Setup tap

- The Technology in Setup page should be c35b4.
- Ruleset Typical
- Output should be

Extracted view

You should pick a good view name to make it easy to differentiate between extraction versions.

Technology C35b4		PuleSet Typical	
p2lvsSet		UseMultRuleSets	
Setup Dir /home/e.u	cad/designkits/a	ams/v400/assura/c35b4,	/c35b4,
Include command File	d =		
Rule Command File Inclu			Vie
Tech Cmd File			
Output Extracted View	Lib Libr	arv1 Cel lavout 02	View inv ex
Enable CellView Check			1
Parasitic Res Component	presistor	Prop Id	r
Parasitic Cap Component	pcapacitor	Prop Id	c
Parasitic Ind Component	pindactor	Prop Id	1
Parasitic M Component	pmind	Prop Id	k
Inductance L1 Prop Id	ind1	Inductance L2 Prop Id	ind2
Call Procedure			
Substrate Extract		Extract MOS Diffu	sion Res 🛛 📝
Extract MOS Diffusion AP		Add LVS MOS Di	ffusion Res 📃
Substrate Profile	NONE	Extract MOS Diffu	sion High 🛛 🛛 🔍
Library Prefix			
Library Directory			
	I		
&	y a unrectory r	OF WITCHNY LOCAL LIDE	arres createu
uring the hierarchical s	vtraction of an	extracted view	
oring die interatoritat e	sector of all	CARLOCCU VIEW.	

Extraction Tap

- Extraction Type should be C Only, the other options can be used in further developing.
- Cap Coupling Mode is Coupled(i.e. into account coupling capacitances).
- Ref Node is gnd!.

0	RC (Assura) P	arasitic Extr	action Run F	orm	
Setup Extraction	Filtering	Netlisting	Run Details	Substrate	
Extraction Type	C Only		Name Space	Schematic N	ames 🔽
Max fracture length	infinite	microns	Temperature	25.0	CEdit
Cap Coupling Mode	Coupled		Ref Node	gnd!	
Mult Factor 1.0					
PEEC Mode 📃 🛛 Lac	lder Network 🛛 📃	Global Frequen	су	MHz	
Select Use	r Region]	Uiew	/) (Edit
Net Selection Type	Full Chip All Nets	🔽 QRC	FS Extraction M	ode NONE	
Resistance Mesh	🗆 🔁 Edit	Exclu	ude Via Capacita	ance 📃	
Layer Setup Customi	zation 📃 🔄 Edit		QRCFS	High 🔛	
	From File SelFromSch				
Litho Config File				Viev	v) Edit
Contour Directory					
Enable HRCX		Split Pins 📃	Split Pin Dis	tance 5 I	Microns
2	Enter HRCX Cells				
& CX Cells: Specify	a list of cello	which appear	in the output	hierarchu -	emuires
ll name, with opti	onal view and li	b names (cell	L, view, lib).		.0401100
OK Cancel D	ofaulte	Load State	Saue State	View Command	File

Netlisting Tap

 Design Capacitor Models, Parasitic Capacitor Models, Design Resistor Models and Parasitic Resistor
 Models are all chosen Do not include.

Setup Extraction	Filtering Netlistin	g Run Details Substrate	
			-
Design Capacitor Models	Do Not Include		
Parasitic Capacitor Models	Do Not Include		
Design Resistor Models	Do Not Include		
Parasitic Resistor Models	Do Not Include		
Netlist With Names From	Schematic -		
Enable Virtual Metal Fill	🔄 Fine Shape 🕞	Save Fill Shapes	
Sub Node Character	#	Bus Bit	1
Hierarchy Delimiter		Device Finger Delimiter	
Import Globals		Force Globals	
Parasitic Resistance Width	Off	Parasitic Resistance Length 🛛 📃	
Parasitic Resistance Tempe	erature Coefficient		
XY Coordinates	R C r	c D M Q	
Ignore Vias	Layer	Nets	
Auto Substrate Stamping O	ff 📃		
Add Explicit Vias			
Via Effect Off			
Gate Diffusion Fringing Ca	pOff 📃		
Instance Off			5
to substrate stamping of yers. This command enabl amping is defined in the	n: Disavie the Saus Les the "Ignore Via: e p2lvs file.	strate stamping reature for an s" option even though layer	La construction of the second s

Run the extraction

Click OK to run the extraction

- Extraction can take a while on a large circuit
- Check for no errors
- Errors are rare typically just 'check and save' errors



The extracted view

This has created a new cell view called 'inv_ex_C_only02'

Library Manager:	Directory1g12/6097/zty_demo_	new_cadence _ 🗆 🗙
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
Show Categories Show Files Library Library1 IOLIB_3B_4M IOLIB_ANA_3B_4M IOLIB_ANA_3B_4M IOLIB_ANA_4M LEADFRAMES Library1 Library1	Cell inverter_layout_02 TEST_RC TESTinverter TESTinverter_1X TESTinverter_layout2 inverter inverter_1X inverter_1X	View inv_ex_C_only02 View Lock inv_ex_C_only inv_ex_C_only02 iz1g12@hind.ecs.sot Alayout tz1g12@hind.ecs.sot symbol symbol
Library2 Library3 PACKAGES PRIMLIB PRIMLIBRF SPIRALS_4M	inverter_layout_02	
Log file is "/home/tz1g12/6097/zty_demo_n Warning: ddUpdateLibList: It appears that yc Created new library "Library3" at /home/tz1 Warning: ddUpdateLibList: It appears that yc Warning: ddUpdateLibList: It appears that yc Generated 5 thumbnail(s) Beginning simple copy to library "Library3". Processing files to be copied Warning: ddUpdateLibList: It appears that yc Warning: ddUpdateLibList: It appears that yc	ew_cadence/libManager.log". ou are trying to run an OA executable on CDB g12/6097/zty_demo_new_cadence/Library3. ou are trying to run an OA executable on CDB ou are trying to run an OA executable on CDB ou are trying to run an OA executable on CDB ou are trying to run an OA executable on CDB	data. Library 'amsc35_exa data. Library 'amsc35_exa data. Library 'amsc35_exa data. Library 'amsc35_exa data. Library 'amsc35_exa
		Lib: Library1 Free: 1.71T



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The extracted view

- Looks a bit like the layout
- It is a layout view, but with extracted devices and parasitic shown



Extracting with parasitics

- The extraction will take longer than before, due to the extra rules it needs to run
- Check the CIW (main ICFB window) for any errors
- Open the extracted view
- Spot the extra capacitances
- AMS uses a lumped model i.e. total capacitance from one node to another.





Learning Outcomes Outcomes



After completing this unit, you should be able to:

- Use layout versus schematic (LVS) tools
- Perform an extraction with parasitics
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Extracting with parasitics

We want to simulate the parasitic components in the layout to see their effect on the performance

• E.g. rise time, fall time

Parasitic components consist of Rs and Cs

- Resistance of interconnect
- Capacitance between layers

The AMS kit allows us to extract the parasitic capacitances only

Post-layout simulation

- The schematic you have drawn is not realistic
- The extracted layout, containing parasitic capacitances is far more realistic and it is useful to simulate this to increase confidence in your design
- First we need a test circuit for our inverter, then we need to tell the simulator to use the extracted view, not the schematic view



Post-layout simulation

- 1. For this simulation you need to use the inverter cell which has the following views (schematic, layout, extracted and symbol)
- 2. Create a new test schematic called *Test_Inverter_layout* as shown below using your fixed dimension inverter in it



- We need to create a config view for the Test_Inverter_layout cell, to tell the simulator which view to use
- From Library Manager, go to File -> New cell view
- Choose the name of the cell Test_Inverter_layout
- Choose Type to be config
- Click ok and the Hierarchy Editor will appear

	New File
File	
Library	Library1 🔽
Cell	TESTinverter_layout02
View	config
Туре	config 🔽
Application	
Open with	Hierarchy Editor 🧧
📄 Always use	e this application for this type of file
Library path fil	le

Click 'Use template' and choose a template name 'spectre'

Click 'Ok'	New Configuration	×
	Top Cell]
	Library: Library1 Cell: TESTinverter_layout02 View: Gli Template	
	Lit Vi Sta Cc Cc Ck Cancel Apply Help	
	OK Cancel Use Template Help	

- From the View Tap, Switch to the tree view in the hierarchy editor
- You can see the two inverter instances there
- Right click the 'Set Instance View' column to select the view
- Choose Schematic for one inverter and choose extracted view for the other



Update the instance by ' Virtuoso® Hierarchy Editor Editing; (Library1 TESTinverter layout02 config) (Save 🗕 🗖 🗙 clicking File Edit View Plugins Help cadence Update Needed 6 🕞 🔰 🕹 Update Needed Top Cell ? 🗗 🗙 **Global Bindings** ? 🗗 🗙 Library List: myLib Library: Library1 Cell: TESTinverter_layout02 schematic veriloga ahdl View List: View: schematic Stop List: spectre Constraint List: Edit (Open) (Table View Tree View Target: Instance Instance Inherited View Li-🖻 🟯 (Library1 TESTinverter_lay.. 💿 CO (analogLib cap spec... spectre cmos_sch schematic verilo.. 💿 C1 (analogLib cap spec.. spectre cmos_sch schematic verilo.. 🖶 🧰 16 (Library1 inverter_lay... schematic spectre cmos_sch schematic verilo... ⊕ ≦ I9 (Library1 inverter_lay... inv_ex_C_only02) spectre cmos sch schematic verilo... O (analogLib vdc spec... spectre cmos_sch schematic verilo... 0 V1 (analogLib vpulse s... spectre cmos_sch schematic verilo.. 🝈 V2 (analogLib vpulse s... spectre cmos_sch schematic verilo... Namespace: CDBA Filters: OFF Update: Needed 19(32) >

Open your test from Schematic Config mode

🐕 Virtuoso® Hierarchy Editor Editing: (Library1 TESTi	nverter_layo	ut02 config) (Save	
<u>Eile E</u> dit <u>V</u> iew <u>P</u> lugins <u>H</u> elp	le <u>E</u> dit <u>V</u> iew <u>P</u> lugins <u>H</u> elp cāden		lence
🗅 🍋 🔒 🕼 🚸 🥱 🦿 🕕 🗐 📼 🛁 🗎 🥥	Update Neede	ad	
Top Cell ? 5 ×	Global Bindin	gs	78
Library: Library1	Library List:	myLib	
Cell: TESTinverter_layout02	View List:	schematic veriloga ahdl	
View: schematic	Stop List:	spectre	
Open Edit	Constraint List:		
Table View Tree View Target: Instance View To Use Instance View To Use C0 (analogLib cap spec C0 (analogLib cap spec Image: C1 (analogLib cap spec) Image: C1 (analogLib cap spec) Image: C1 (analogLib verter_lay) schematic Image: C1 (analogLib verter_lay) schematic Image: C1 (analogLib verter_lay) image: C_only02 Image: C1 (analogLib verter_lay) image: C_only02	spectre spectre spectre spectre spectre spectre	Inherited View List cmos_sch schematic veri cmos_sch schematic veri cmos_sch schematic veri cmos_sch schematic veri cmos_sch schematic veri cmos_sch schematic veri	Io Io Io Io Io Io
Image: Image: Namespace: CDBA Filters: OFF Update: Needed 19(32)			

Post-layout simulation

- Now, whenever you want to use the config view in your simulations, you must open the config view to open the schematic, not just open the schematic
- This will give you the option of opening the hierarchy editor and/or schematic
 Open Configuration or Top CellView

Open Configuration or Top CellViev	N X
Open for editing	
Configuration "Library1 TESTinverter_layout02 config"	🖲 yes 🔾 no
Top Cell View "Library1 TESTinverter_layout02 schematic"	🔾 yes 💿 no
ОК	Cancel Help

- Normally you just want to open the schematic
- Try descending into each of the inverters in the schematic
 - One will descent into the schematic, and one into the layout
- Start ADE as usual.
 - ADE will have loaded the config view as it initialised

Post-layout simulation

- Set up a simulation as before
- Run the simulation
- Plot the output of both inverters in the schematic
- Slight difference









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Summary

- Extraction creates a netlist from your layout
- LVS compares the extracted netlist with your schematic
- Extraction can extract parasitic components
- The hierarchy editor can be used to configure which view to use for schematic instances
- Post layout simulation is important for increased confidence in your design



Lab: Layout



Objective: Extract your layout, run LVS, use the hierarchy editor and run a post layout simulation

