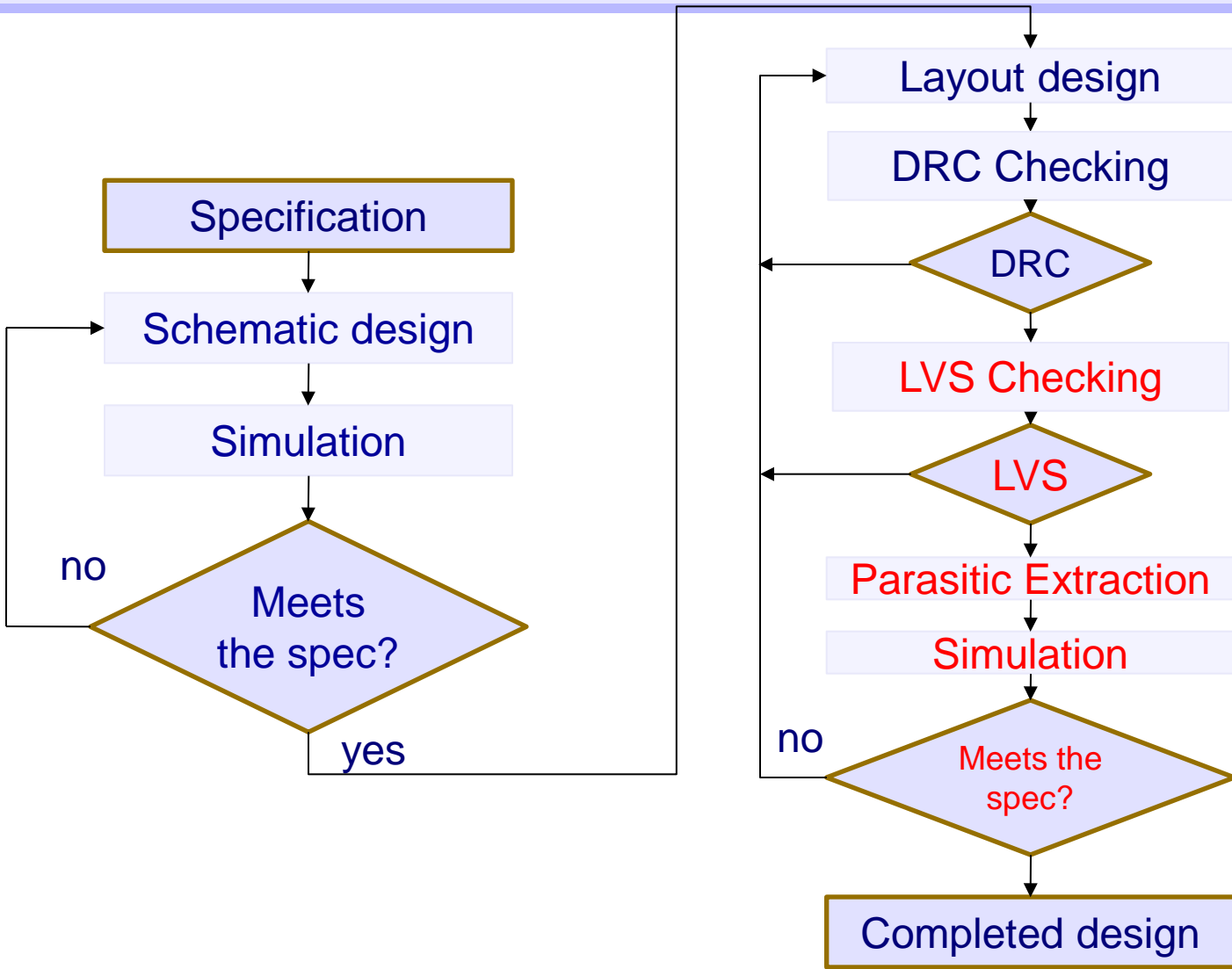


Extraction, LVS and Post-layout simulation

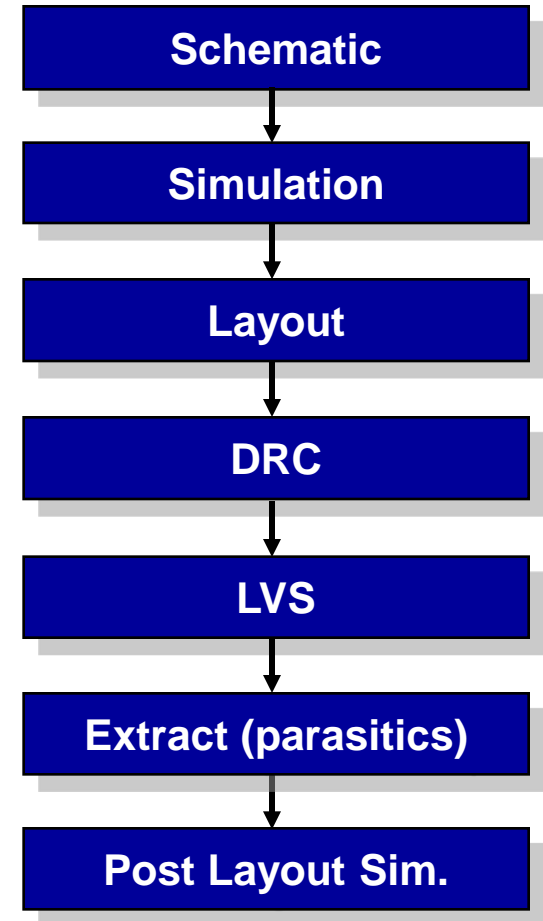
Dr Basel Halak

Custom Design Flow



The post layout process

- So far we have worked through three steps in a typical full custom flow
- After layout there are a number of mandatory steps before fabrication
 - Layout versus schematic – checks that the extracted layout netlist matches the schematic
 - Extract the layout, this time with parasitics
 - Post-layout simulation using the extracted (with parasitics) netlist



Learning Outcomes

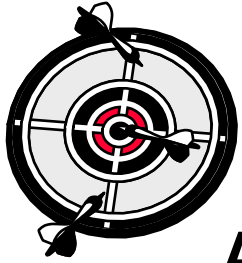


After completing this unit, you should be able to:

- **Use layout versus schematic (LVS) tools**
- **Perform an extraction with parasitics**
- **Use the hierarchy editor**
- **Run a post-layout simulation**



Learning Outcomes



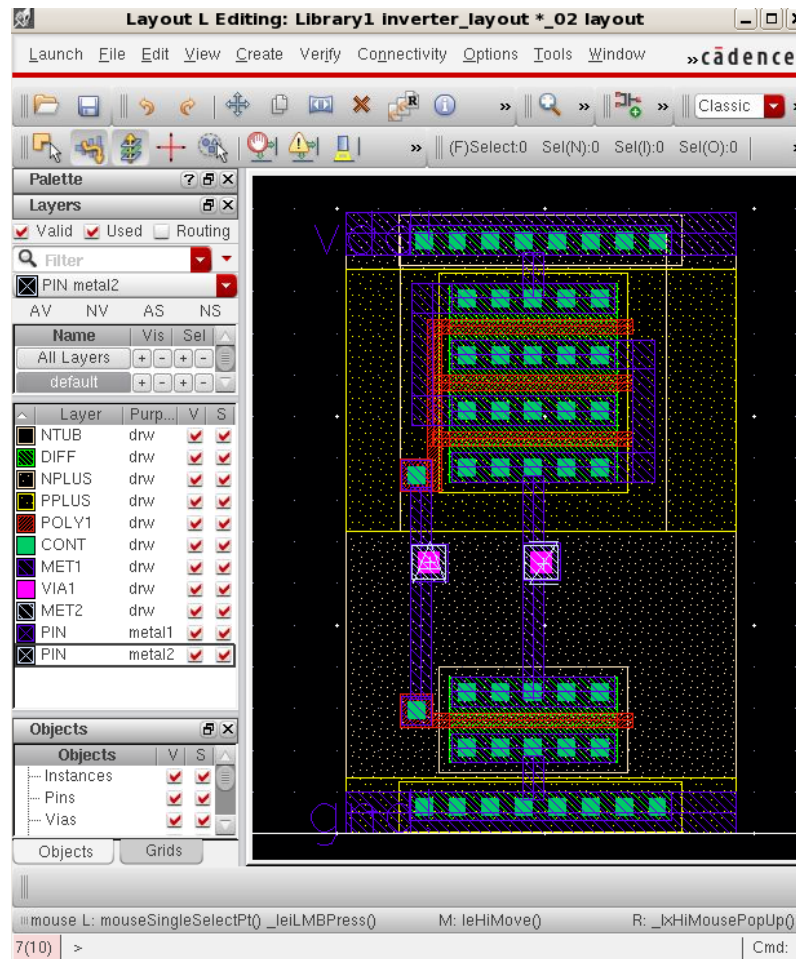
After completing this unit, you should be able to:

- **Use layout versus schematic (LVS) tools**
- **Perform an extraction with parasitics**
- **Use the hierarchy editor**
- **Run a post-layout simulation**



Where we left off

- In the last lecture, you saw how to use Virtuoso to create a basic layout cell.
- Your layout much be free from all DRC errors before you do LVS checking



Extraction

- The extraction tool is invoked from within the Layout window
- This brings up the extract form (Run Assura LVS)

Run Assura LVS

Schematic Design Source: DFII, Use Existing Netlist, Netlisting Options...

Library: Library1, Cell: nverter_layout_02, View: schematic, Browse...

Layout Design Source: DFII, Use Existing Extracted Netlist

Library: Library1, Cell: nverter_layout_02, View: layout, Browse...

Run Name: verter_layout_02, Run Directory: ./Assura

Run Location: local

View Rules Files: Technology: c35b4, Rule Set: default

Extract Rules: /s/ans/v400/assura/c35b4/c35b4/extract.rul, View..., Reload

Compare Rules: /designkits/ans/v400/assura/c35b4/c35b4/compare.rul, View...

Switch Names: resimulate_extracted, Set Switches

Binding File(s): /designkits/ans/v400/assura/c35b4/c35b4/bind.rul, View...

RSF Include: /designkits/ans/v400/assura/c35b4/c35b4/LVSinclude.rsf, View...

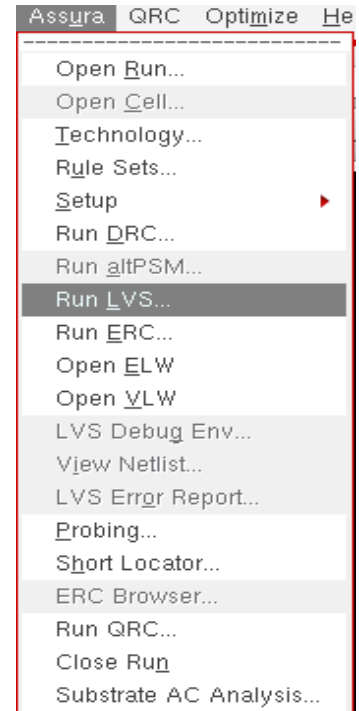
Variable	Value	Default	Description
None			

View avParameters: Modify avParameters... 2 avParameters are set

View avCompareRules: Modify avCompareRules... 13 avCompare rules are set

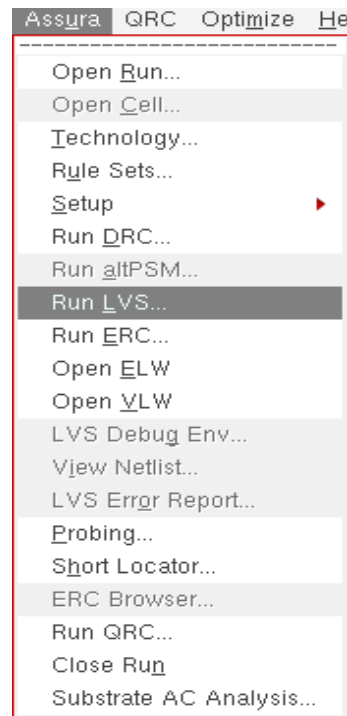
View Additional Functions: No additional functions are set

OK Cancel Apply Defaults Load State Save State View RSF Help



Layout versus schematic (LVS)

- **Layout versus schematic compares the extracted netlist to the schematic**
- **You can invoke the LVS tool from the Layout view window**



Layout versus schematic (LVS)

- Here we will perform the circuit extraction, that is, all the parasitics resulting the layout of the devices (capacitances, diodes, and other components that can exist due to the interaction between different layers). The layout view will also be compared with the schematic (Layout versus Schematic, or simply LVS)
- Without any DRC error, select Assura → Run LVS. In the main form press **Set Switches**, select the `resimulate_extracted` option and press **OK**. This ensures the use of this LVS run for RCX.

Running the LVS check

■ In the *RUN Assura LVS* window:

1. The Cell name should be the same as your Run name.

2. Technology should be chosen by c35b4.

3. The extract rule should be:

`/home/esdcad/designkits/ams/v400/assura/c35b4/c35b4/extract.rul`

4. The Compare rules should be

`home/designkits/ams/v400/assura/c35b4/c35b4/compare.rul`

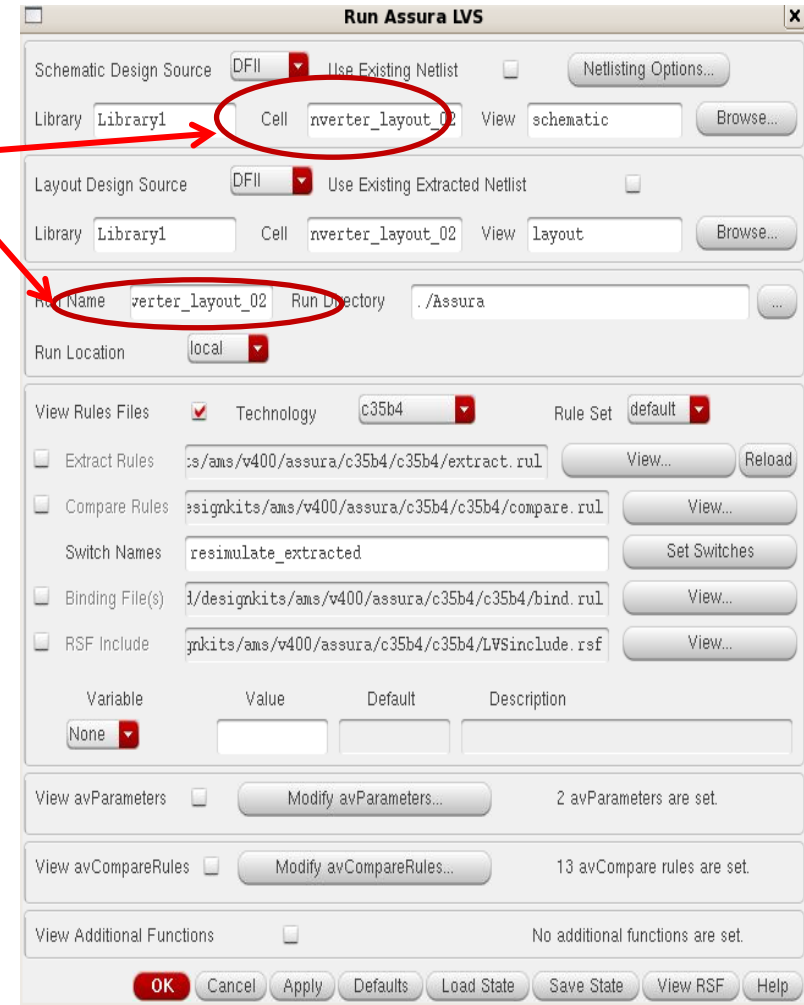
5. The binding files should be

`/home/esdcad/designkits/ams/v400/assura/c35b4/c35b4/bind.rul`

6. RSF include should be

`/home/esdcad/designkits/ams/v400/assura/c35b4/c35b4/LVSinclude.rsf`

7. Select the switches option `resimulate_extracted` to ensure ensures the use of this LVS run for RCX.



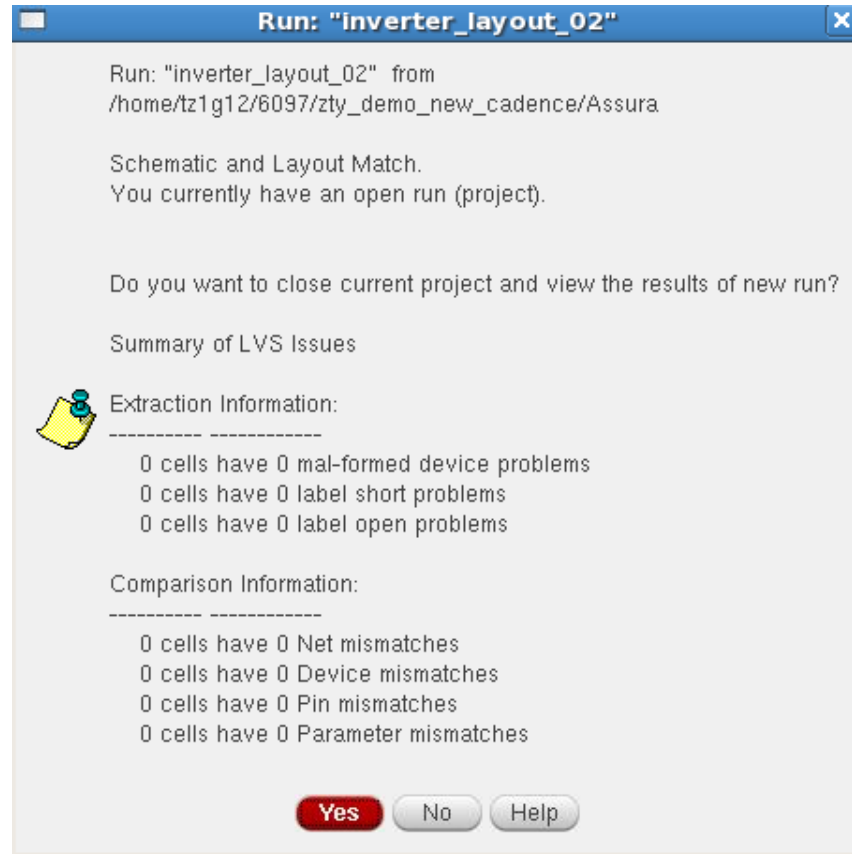
Layout versus schematic (LVS)

- In the main form press OK to start LVS. Then you will see the progress window.



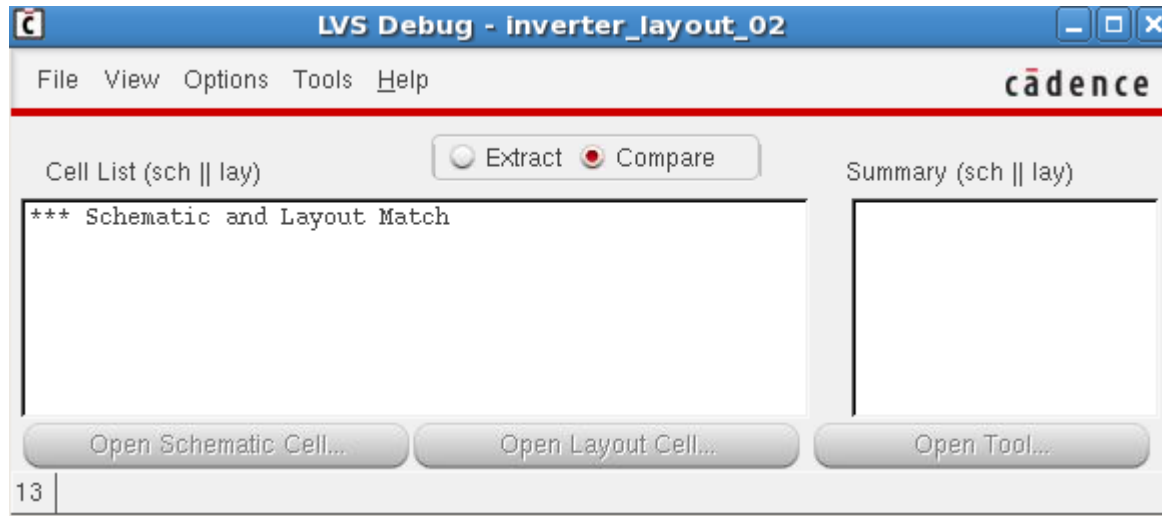
Checking the LVS output

- If there is nothing wrong, you will receive this message.



Layout versus schematic (LVS)

- **Click Yes. You will see the Schematic and Layout Match.**

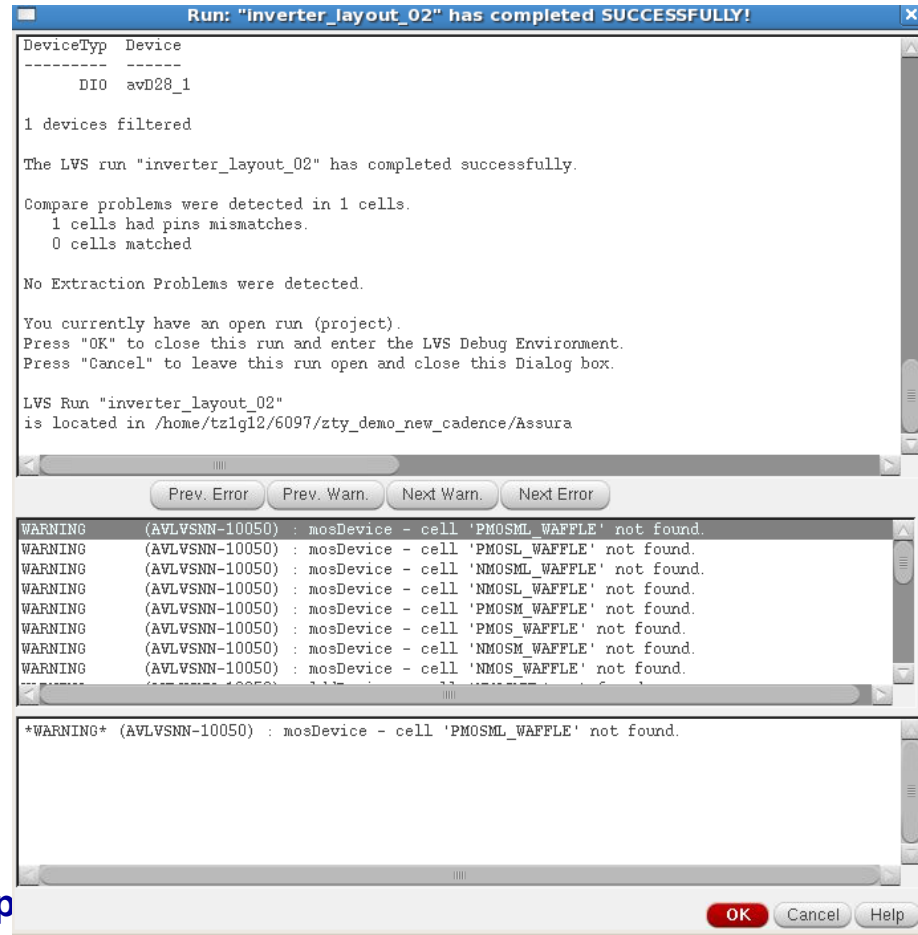


Typical LVS errors

- In our case you should get at least one error – the terminals don't all match
- Reading further on, it is clear that the problem is with the Z terminal in the layout
- Clearly, I have labelled the output Z in the layout and Y in the schematic – an easy fix.

Typical LVS errors

- So if you have LVS errors you will receive the following message which lists all errors. Click ok to go to Debug Window



The screenshot shows a terminal window titled "Run: 'inverter_layout_02' has completed SUCCESSFULLY!". The window displays the following text:

```
DeviceTyp Device
-----
DIO avD28_1

1 devices filtered

The LVS run "inverter_layout_02" has completed successfully.

Compare problems were detected in 1 cells.
  1 cells had pins mismatches.
  0 cells matched

No Extraction Problems were detected.

You currently have an open run (project).
Press "OK" to close this run and enter the LVS Debug Environment.
Press "Cancel" to leave this run open and close this Dialog box.

LVS Run "inverter_layout_02"
is located in /home/tz1q12/6097/zty_demo_new_cadence/Assura
```

Below the text, there are four buttons: "Prev. Error", "Prev. Warn.", "Next Warn.", and "Next Error".

The terminal also shows a list of warning messages:

```
WARNING (AVLSNN-10050) : mosDevice - cell 'PMOSML_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'PMOSL_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'NMOSML_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'NMOSL_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'PMOSM_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'PMOSM_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'NMOSM_WAFFLE' not found.
WARNING (AVLSNN-10050) : mosDevice - cell 'NMOSM_WAFFLE' not found.
```

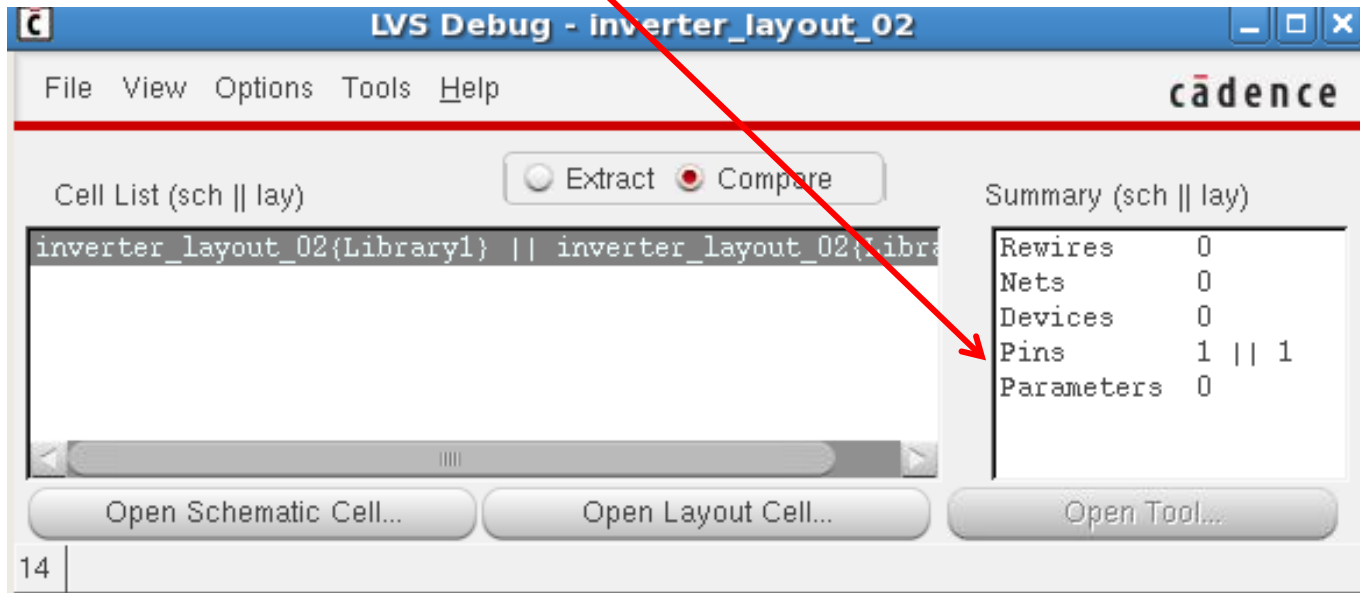
At the bottom of the terminal, there is a summary line:

```
*WARNING* (AVLSNN-10050) : mosDevice - cell 'PMOSML_WAFFLE' not found.
```

At the bottom of the window, there are three buttons: "OK", "Cancel", and "Help".

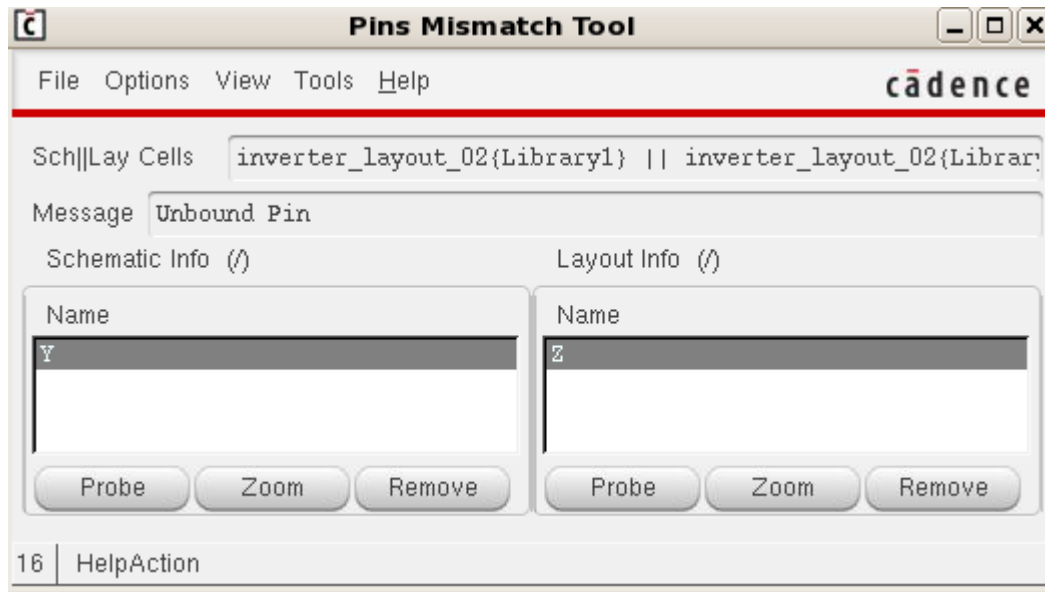
Typical LVS errors

- LVS Debug Window gives more details on each error in the summary box
- Double click the Pins

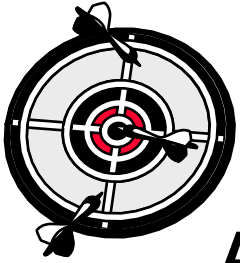


Typical LVS errors

- You can find the mismatch detail and fix it.



Learning Outcomes



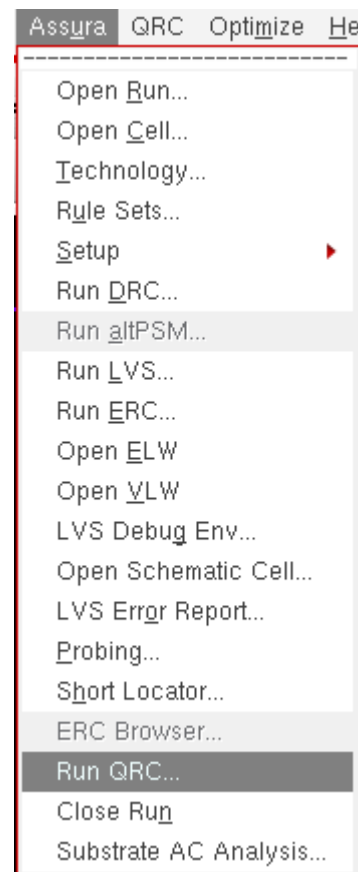
After completing this unit, you should be able to:

- Use layout versus schematic (LVS) tools
- **Perform an extraction with parasitics**
- Use the hierarchy editor
- Run a post-layout simulation



Extraction

- You need to ensure that your design is free LVS errors you can proceed with the extraction b
- The extraction tool is invoked from within the Layout window: as follows: Assura → Run QRC and to choose Extraction tab.
- For the reference node (Ref Node) write gnd!. Proceed with OK.



Setup tap

- The Technology in Setup page should be c35b4.
- Ruleset Typical
- Output should be *Extracted view*
- You should pick a good view name to make it easy to differentiate between extraction versions.

QRC (Assura) Parasitic Extraction Run Form

Setup Extraction Filtering Netlisting Run Details Substrate

Technology c35b4 RuleSet Typical

p2lvsSet NONE UseMultRuleSets

Setup Dir /home/assura/designkits/ams/v400/assura/c35b4/c35b4, ... View Edit

Include Command File ... View Edit

Rule Command File Include ... View Edit

Tech Cmd File User ... View Edit

Output Extracted View Lib Library1 Cel layout_02 View inv_ex_c_onl

Enable CellView Check

Parasitic Res Component presistor Prop Id r

Parasitic Cap Component pcapacitor Prop Id c

Parasitic Ind Component pinductor Prop Id l

Parasitic M Component pmind Prop Id k

Inductance L1 Prop Id ind1 Inductance L2 Prop Id ind2

Call Procedure

Substrate Extract Extract MOS Diffusion Res

Extract MOS Diffusion AP Add LVS MOS Diffusion Res

Substrate Profile NONE Extract MOS Diffusion High NONE

Library Prefix

Library Directory

Library Directory: Specify a directory for writing local libraries created during the hierarchical extraction of an extracted view.

OK Cancel Defaults Apply Load State Save State View Command File Help

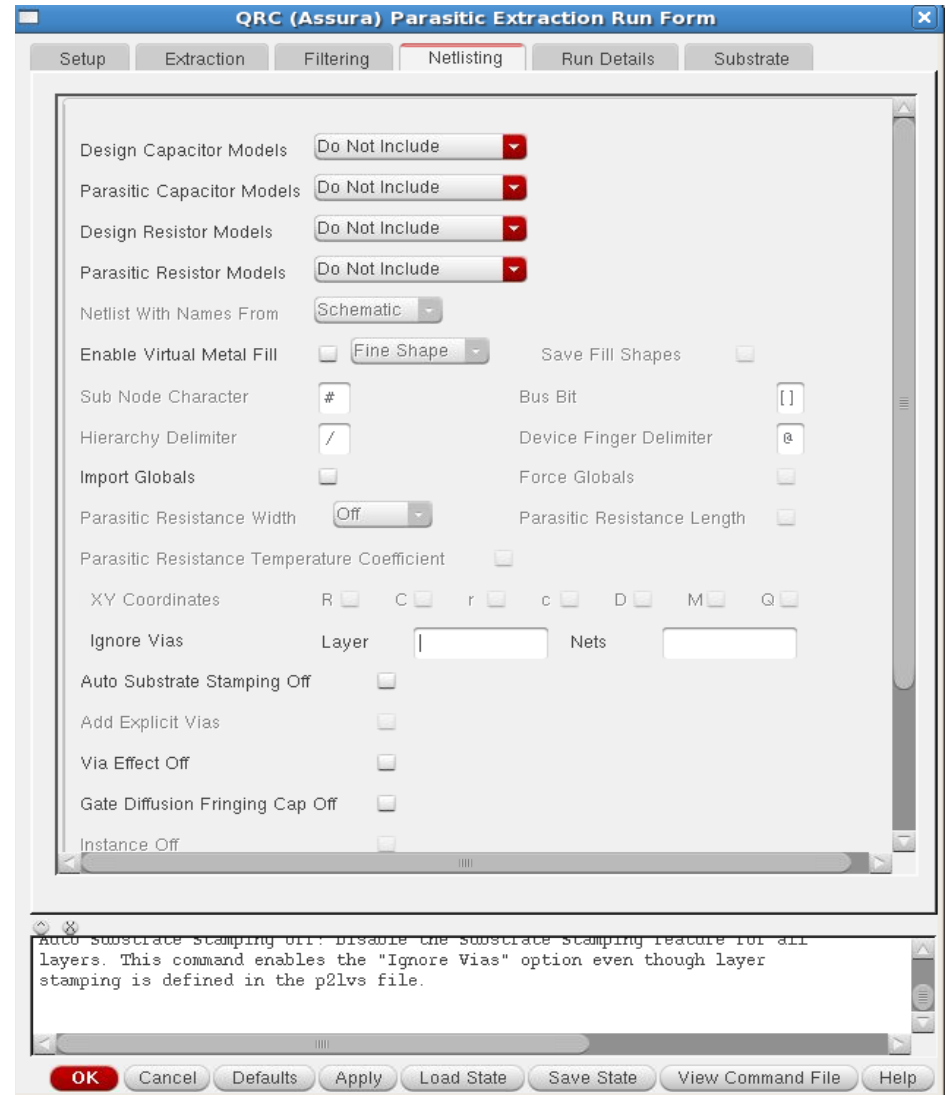
Extraction Tap

- **Extraction Type** should be C Only, the other options can be used in further developing.
- **Cap Coupling Mode** is Coupled (i.e. into account coupling capacitances).
- **Ref Node** is gnd!.

The screenshot shows the 'QRC (Assura) Parasitic Extraction Run Form' dialog box. The 'Extraction' tab is selected. The 'Extraction Type' is set to 'C Only'. The 'Name Space' is 'Schematic Names'. The 'Max fracture length' is 'infinite' in 'microns'. The 'Temperature' is '25.0'. The 'Cap Coupling Mode' is 'Coupled'. The 'Ref Node' is 'gnd!'. The 'Mult Factor' is '1.0'. The 'PEEC Mode' is unchecked. The 'Ladder Network' is unchecked. The 'Global Frequency' is 'MHz'. The 'User Region' is empty. The 'Net Selection Type' is 'Full Chip All Nets'. The 'QRCFS Extraction Mode' is 'NONE'. The 'Resistance Mesh' is unchecked. The 'Exclude Via Capacitance' is unchecked. The 'Layer Setup Customization' is unchecked. The 'QRCFS High' is unchecked. The 'Litho Config File' is empty. The 'Contour Directory' is empty. The 'Enable HRCX' is unchecked. The 'Split Pins' is unchecked. The 'Split Pin Distance' is '5' in 'Microns'. The 'Enter HRCX Cells' field is empty. The 'OK' button is highlighted in red. The bottom of the dialog box contains a text area with the following text: 'HRCX Cells: Specify a list of cells which appear in the output hierarchy, requires cell name, with optional view and lib names (cell, view, lib).'

Netlisting Tap

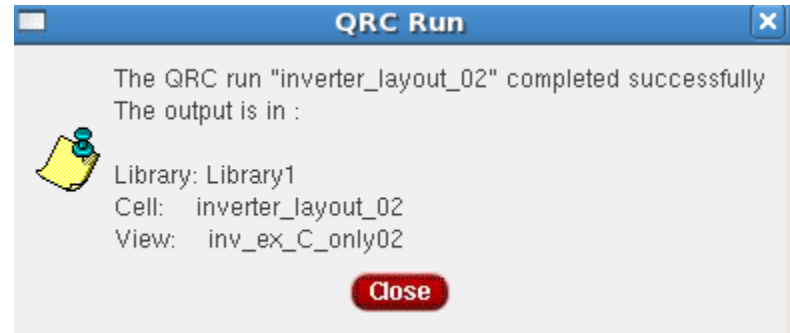
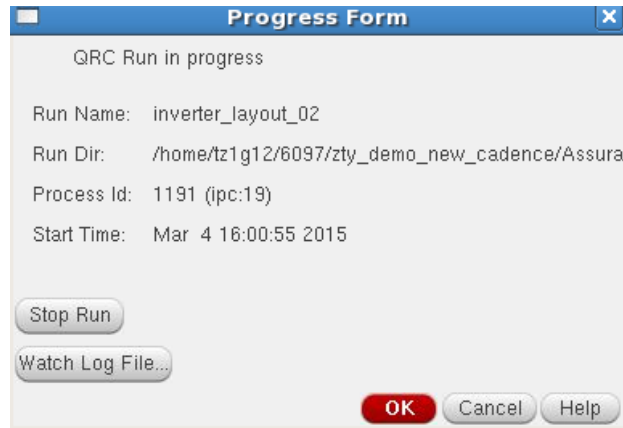
- **Design Capacitor Models, Parasitic Capacitor Models, Design Resistor Models and Parasitic Resistor Models are all chosen Do not include.**



Run the extraction

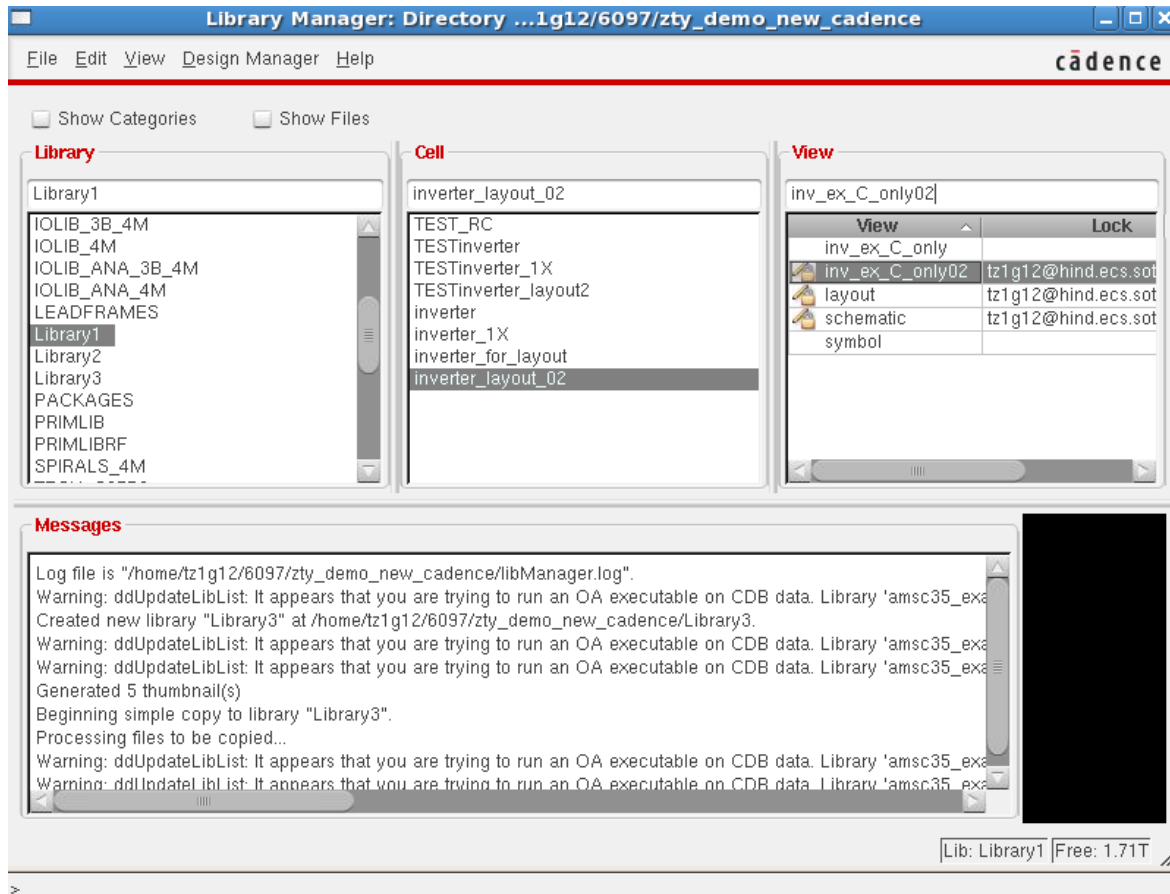
■ Click OK to run the extraction

- Extraction can take a while on a large circuit
- Check for no errors
- Errors are rare – typically just ‘check and save’ errors



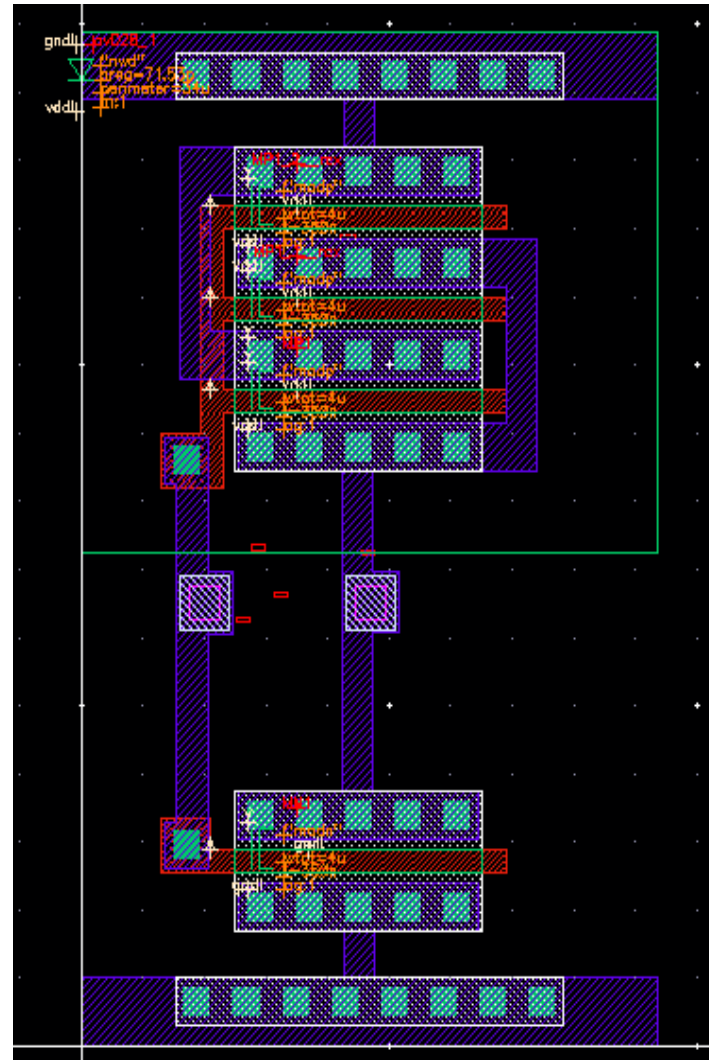
The extracted view

- This has created a new cell view called 'inv_ex_C_only02'

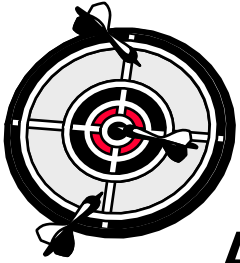


The extracted view

- Looks a bit like the layout
- It is a layout view, but with extracted devices and parasitic shown



Learning Outcomes



After completing this unit, you should be able to:

- Use layout versus schematic (LVS) tools
- Perform an extraction with parasitics
- Use the hierarchy editor
- Run a post-layout simulation



Extracting with parasitics

- **We want to simulate the parasitic components in the layout to see their effect on the performance**
 - E.g. rise time, fall time
- **Parasitic components consist of Rs and Cs**
 - Resistance of interconnect
 - Capacitance between layers
- **The AMS kit allows us to extract the parasitic capacitances only**



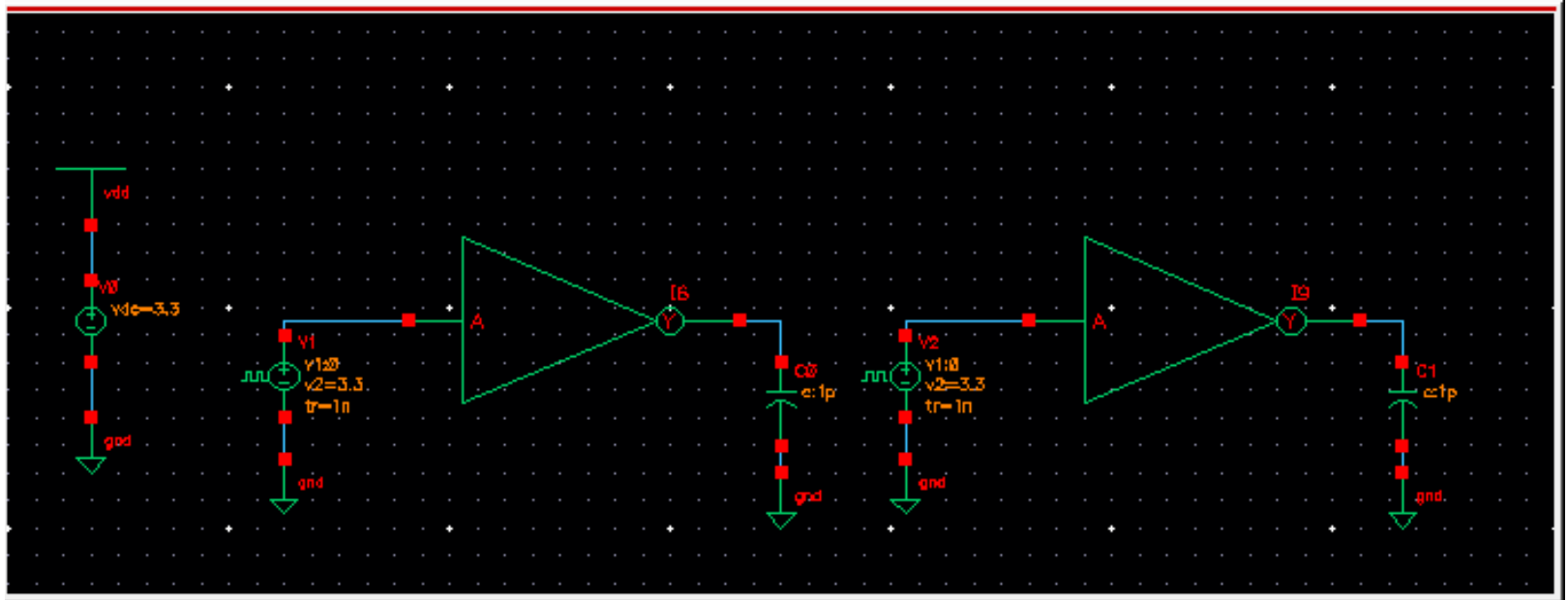
Post-layout simulation

- **The schematic you have drawn is not realistic**
- **The extracted layout, containing parasitic capacitances is far more realistic and it is useful to simulate this to increase confidence in your design**
- **First we need a test circuit for our inverter, then we need to tell the simulator to use the extracted view, not the schematic view**



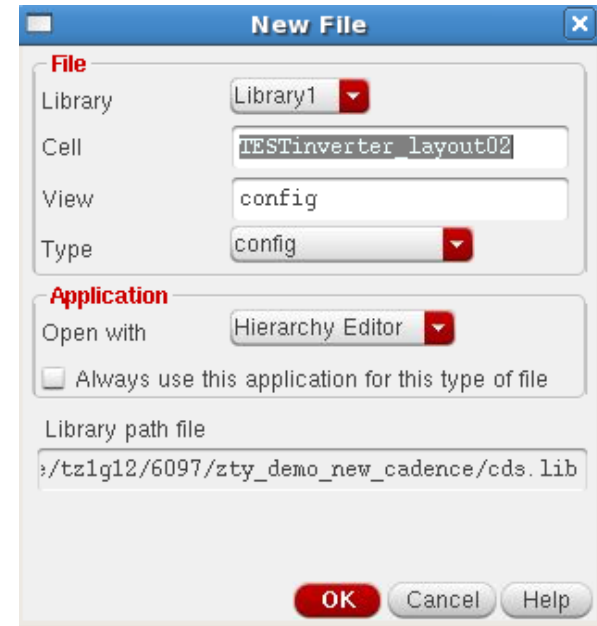
Post-layout simulation

1. For this simulation you need to use the inverter cell which has the following views (schematic, layout, extracted and symbol)
2. Create a new test schematic called *Test_Inverter_layout* as shown below using your fixed dimension inverter in it



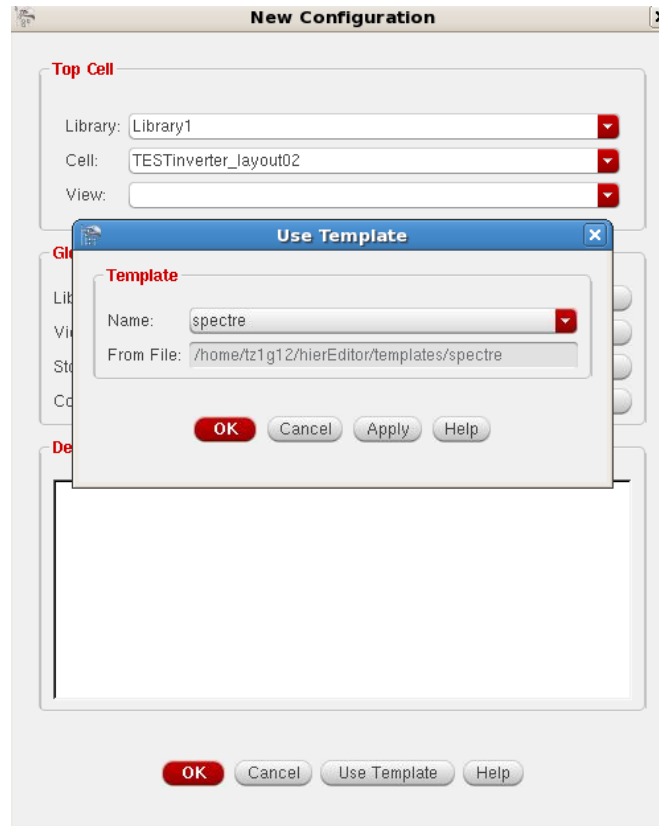
How to use the Hierarchy Editor

- We need to create a config view for the *Test_Inverter_layout* cell, to tell the simulator which view to use
- From Library Manager, go to File -> New cell view
- Choose the name of the cell *Test_Inverter_layout*
- Choose Type to be *config*
- *Click ok* and the Hierarchy Editor will appear



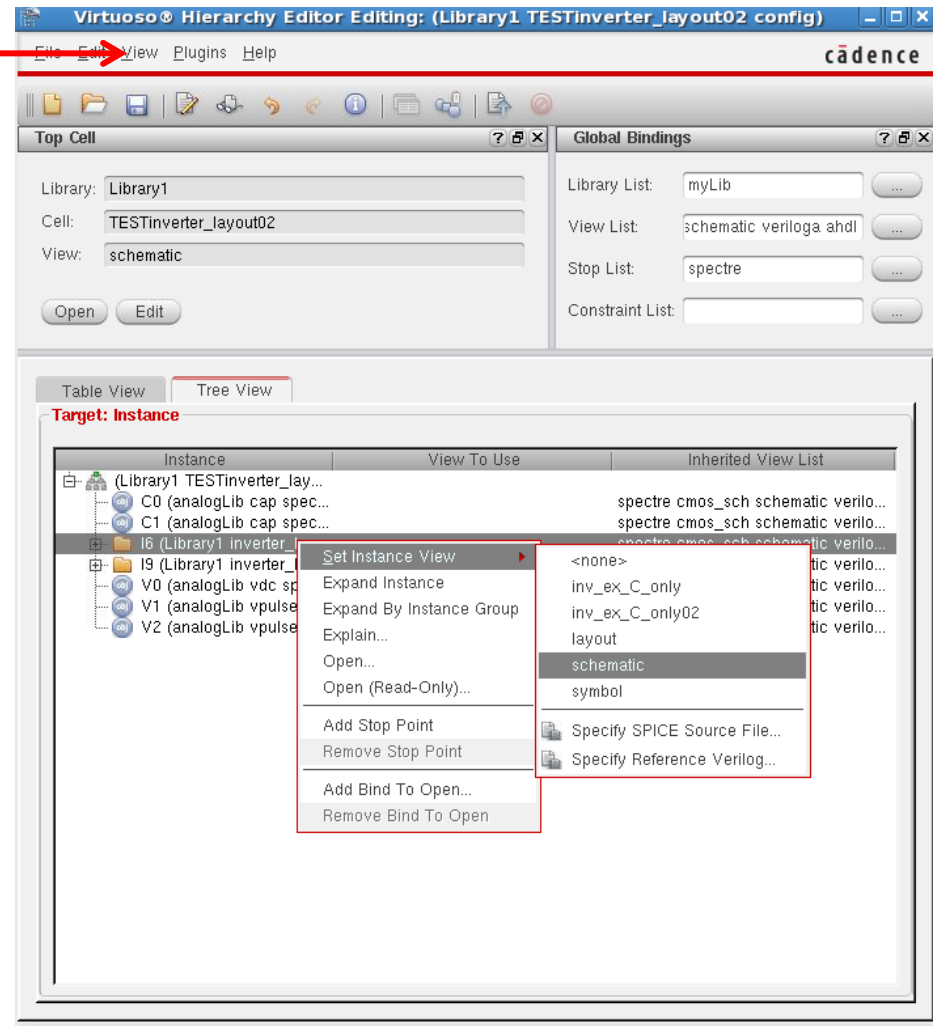
How to use the Hierarchy Editor

- Click 'Use template' and choose a template name 'spectre'
- Click 'Ok'



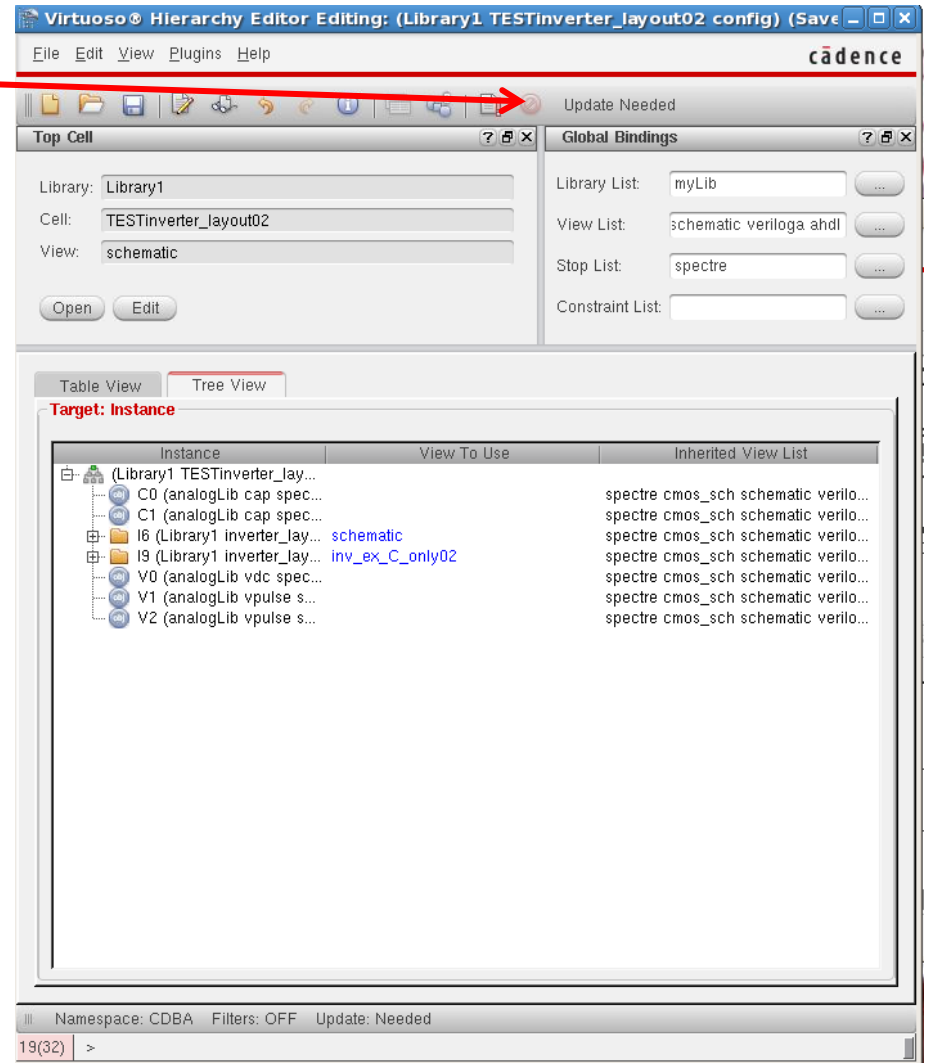
How to use the Hierarchy Editor

- From the View Tap, Switch to the tree view in the hierarchy editor
- You can see the two inverter instances there
- Right click the 'Set Instance View' column to select the view
- Choose Schematic for one inverter and choose extracted view for the other



How to use the Hierarchy Editor

■ Update the instance by clicking



How to use the Hierarchy Editor

- Open your test from Schematic Config mode

The screenshot shows the Virtuoso Hierarchy Editor interface. The title bar reads "Virtuoso Hierarchy Editor Editing: (Library1 TESTInverter_layout02 config) (Save)". The menu bar includes "File", "Edit", "View", "Plugins", and "Help". The "Top Cell" panel displays the following information:

- Library: Library1
- Cell: TESTInverter_layout02
- View: schematic

Below the "Top Cell" panel are "Open" and "Edit" buttons. A red arrow points from the text "Open your test from Schematic Config mode" to the "Open" button. To the right is the "Global Bindings" panel, which includes:

- Library List: myLib
- View List: schematic verilog ahdl
- Stop List: spectre
- Constraint List:

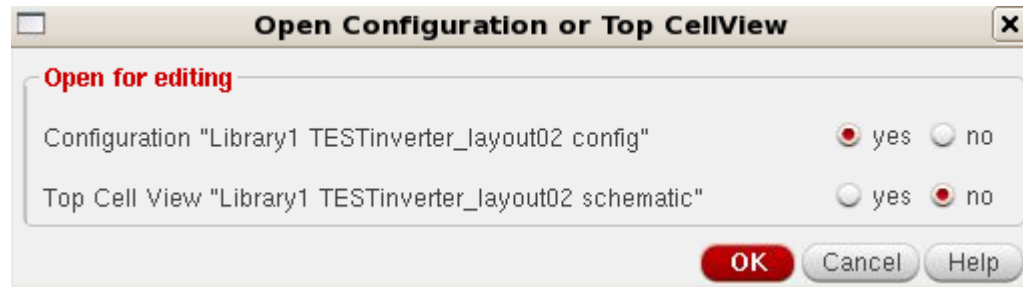
The main area shows a tree view of the hierarchy. The "Target: Instance" panel is active, displaying a table with the following columns: "Instance", "View To Use", and "Inherited View List".

Instance	View To Use	Inherited View List
(Library1 TESTInverter_lay...		
C0 (analogLib cap spec...		spectre cmos_sch schematic verilo...
C1 (analogLib cap spec...		spectre cmos_sch schematic verilo...
I6 (Library1 inverter_lay...	schematic	spectre cmos_sch schematic verilo...
I9 (Library1 inverter_lay...	inv_ex_C_only02	spectre cmos_sch schematic verilo...
V0 (analogLib vdc spec...		spectre cmos_sch schematic verilo...
V1 (analogLib vpulse s...		spectre cmos_sch schematic verilo...
V2 (analogLib vpulse s...		spectre cmos_sch schematic verilo...

The status bar at the bottom shows "Namespace: CDBA", "Filters: OFF", "Update: Needed", and "19(32) >".

Post-layout simulation

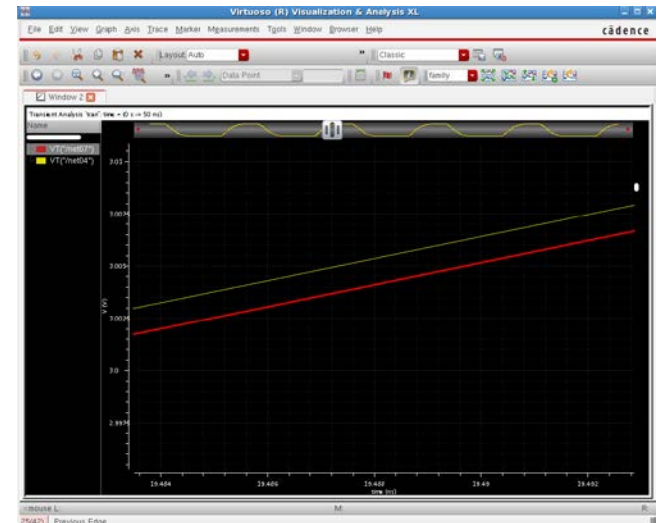
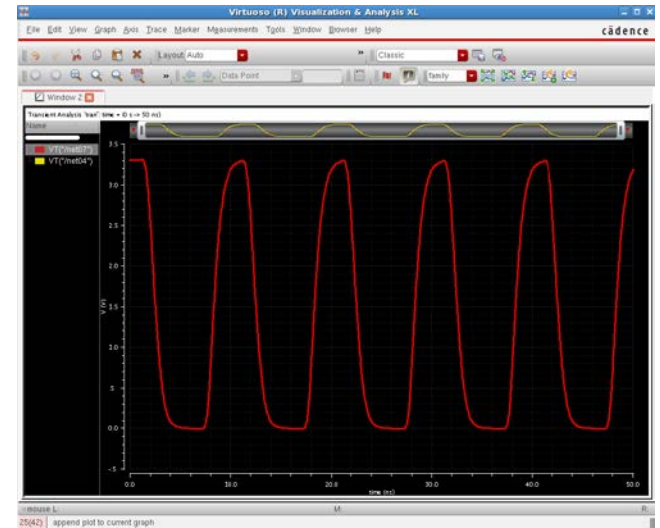
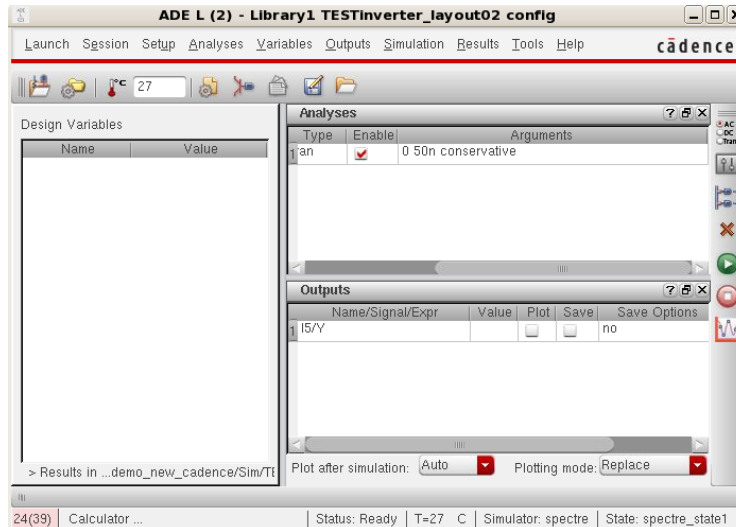
- Now, whenever you want to use the config view in your simulations, you must open the config view to open the schematic, not just open the schematic
- This will give you the option of opening the hierarchy editor and/or schematic



- Normally you just want to open the schematic
- Try descending into each of the inverters in the schematic
 - One will descend into the schematic, and one into the layout
- Start ADE as usual.
 - ADE will have loaded the config view as it initialised

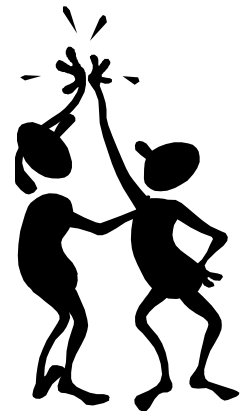
Post-layout simulation

- Set up a simulation as before
- Run the simulation
- Plot the output of both inverters in the schematic
- Slight difference



Summary

- **Extraction creates a netlist from your layout**
- **LVS compares the extracted netlist with your schematic**
- **Extraction can extract parasitic components**
- **The hierarchy editor can be used to configure which view to use for schematic instances**
- **Post layout simulation is important for increased confidence in your design**



Lab: Layout



Objective: Extract your layout, run LVS, use the hierarchy editor and run a post layout simulation

