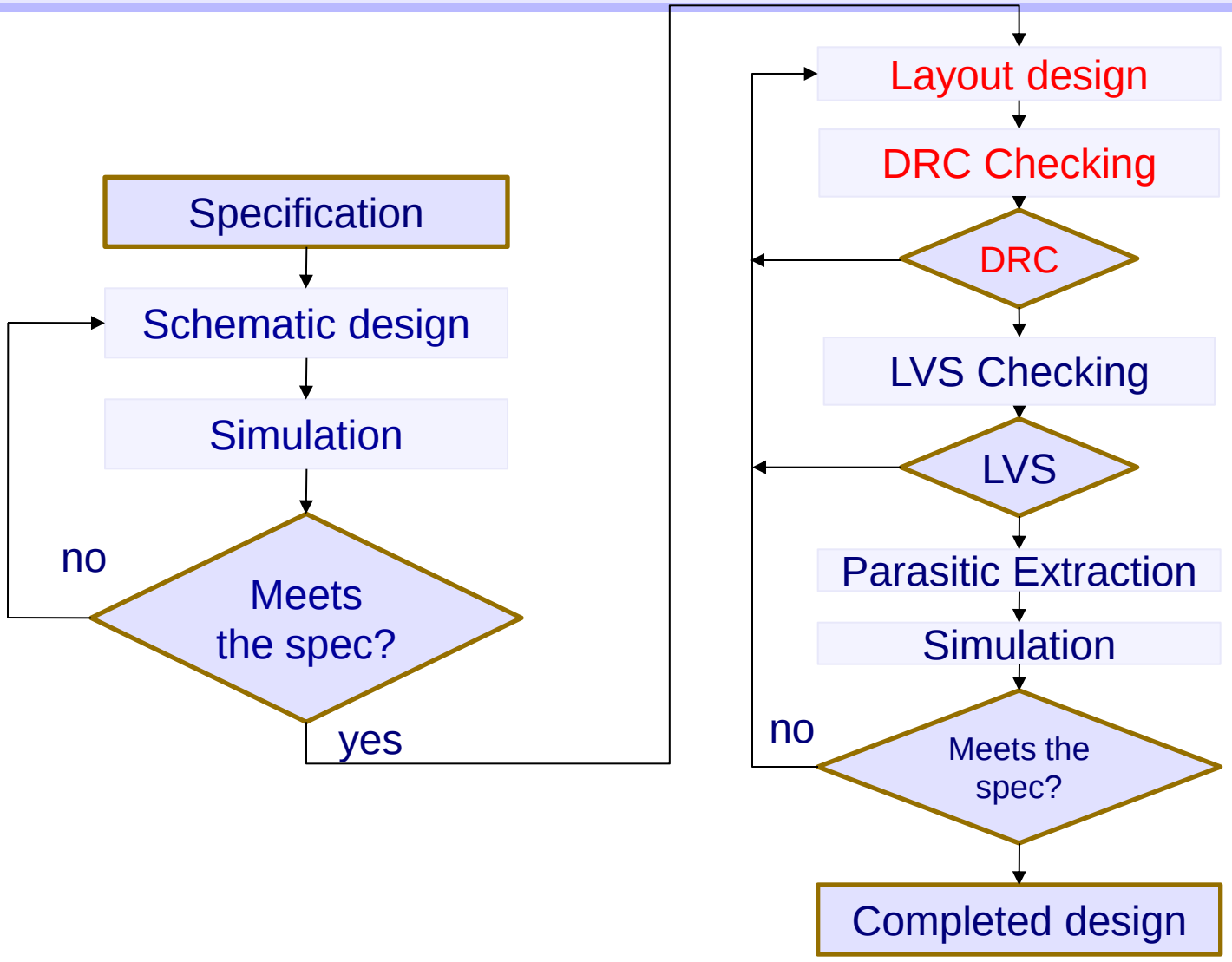
Inverter Layout In Cadence

Dr Basel Halak

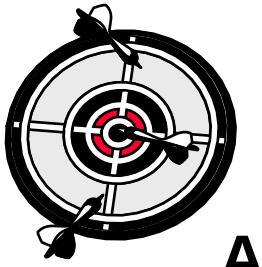
Custom Design Flow



Manual and semi-automated layout

- **There are two main ways to create a layout**
  - Standard design Flow (Automated) e.g. (Digital Design Flow)
  - Full custom layout – placing transistors and interconnects manually
- **Today we will learn about custom layout, but there are a number of ways of approaching this**
  - Pcells are parameterised layout cells, typically of transistors and vias, which do the hard work for you
  - Pcells create the transistor features automatically
  - LayoutL allows you to place the transistors in your layout from the schematic dimensions, saving time

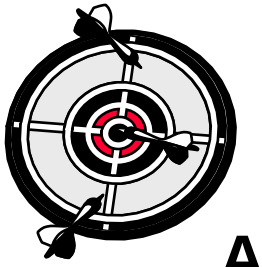
Learning Outcomes



After completing this unit, you should be able to:

1. **Use LayoutL to place transistors in a layout**
2. **Construct a simple layout, step by step**
3. **Use the DRC checking tool**
4. **Search and explain errors**

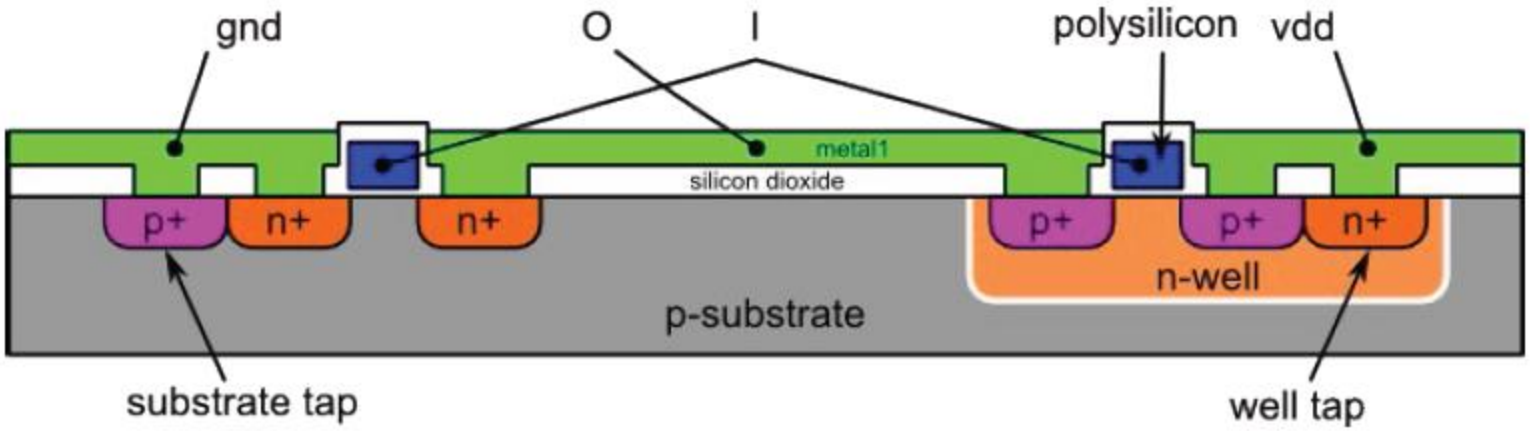
Learning Outcomes



After completing this unit, you should be able to:

1. **Use LayoutL to place transistors in a layout**
2. **Construct a simple layout, step by step**
3. **Use the DRC checking tool**
4. **Search and explain errors**

Inverter Layout



Set up the current working directory

1. Create aa folder for this lab and move into it

2. Copy the display.drf file to your working directory or alternatively

   you can copy this file from the following location:

   /home/esdcad/designkits/ams/v400/cds/HK_ALL/env

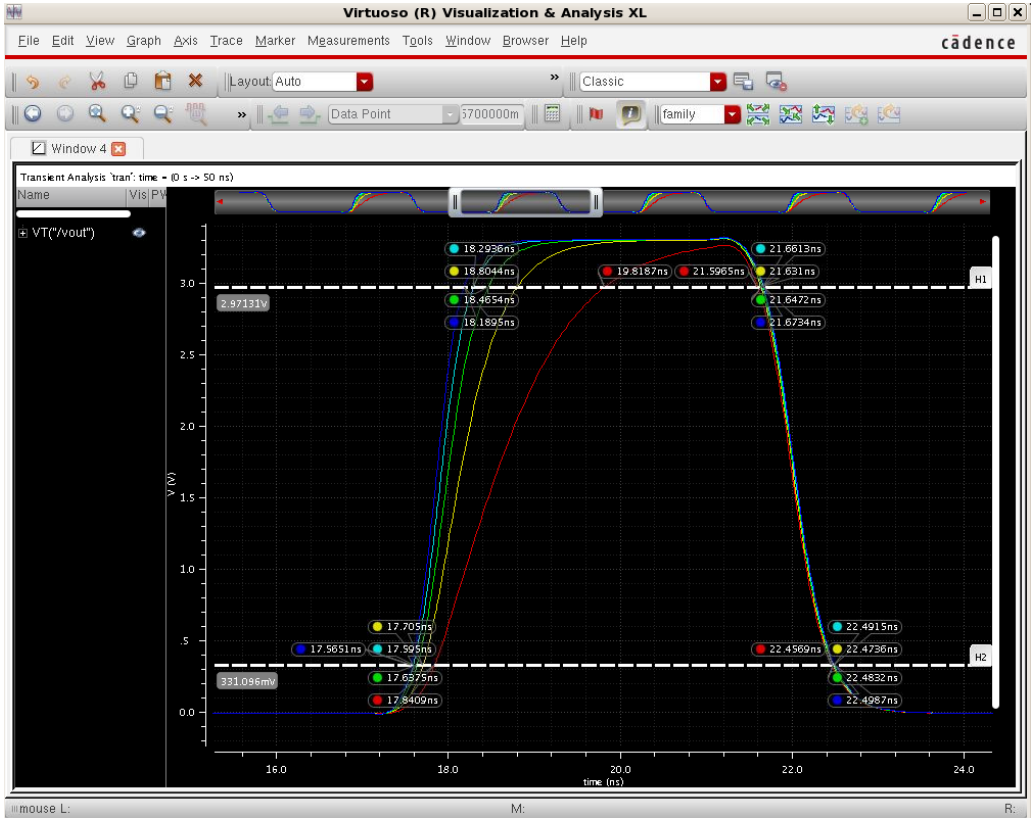
3. Type the following:

   tcsh

   source /opt/esdcad/scripts/ams_v400_tcshrc

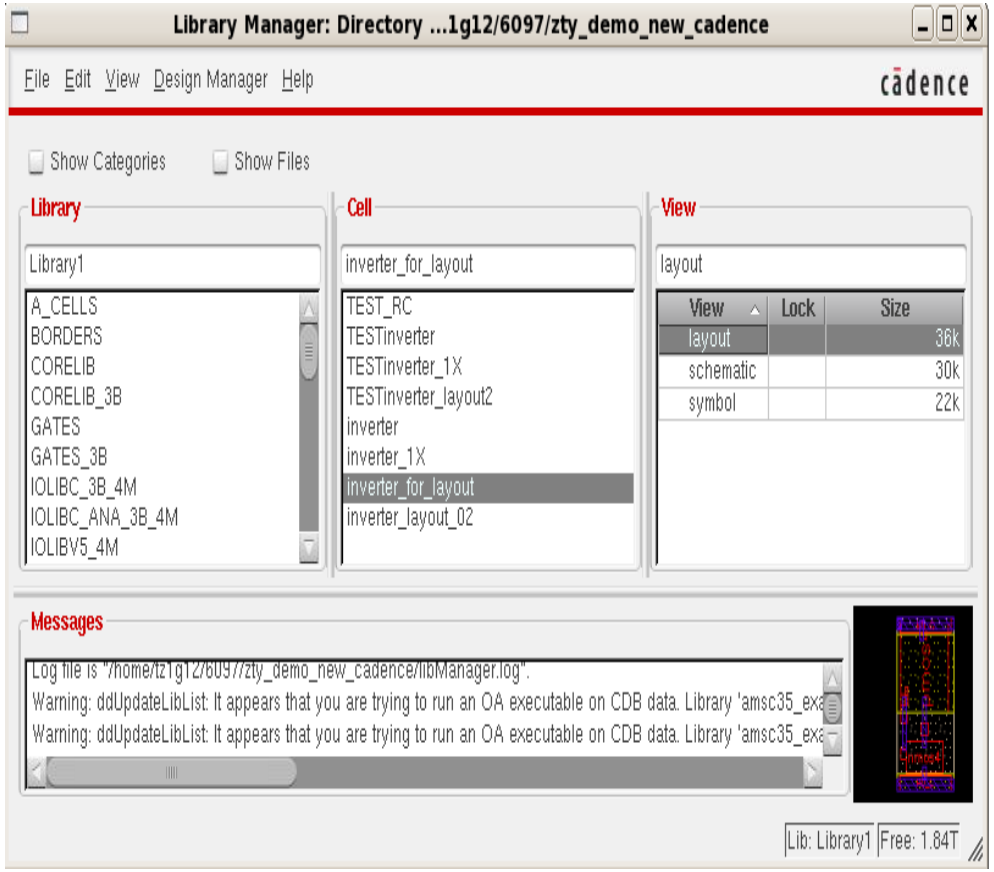
Where we left off

- **In the last lecture, you saw how to simulate your inverter test circuit.**



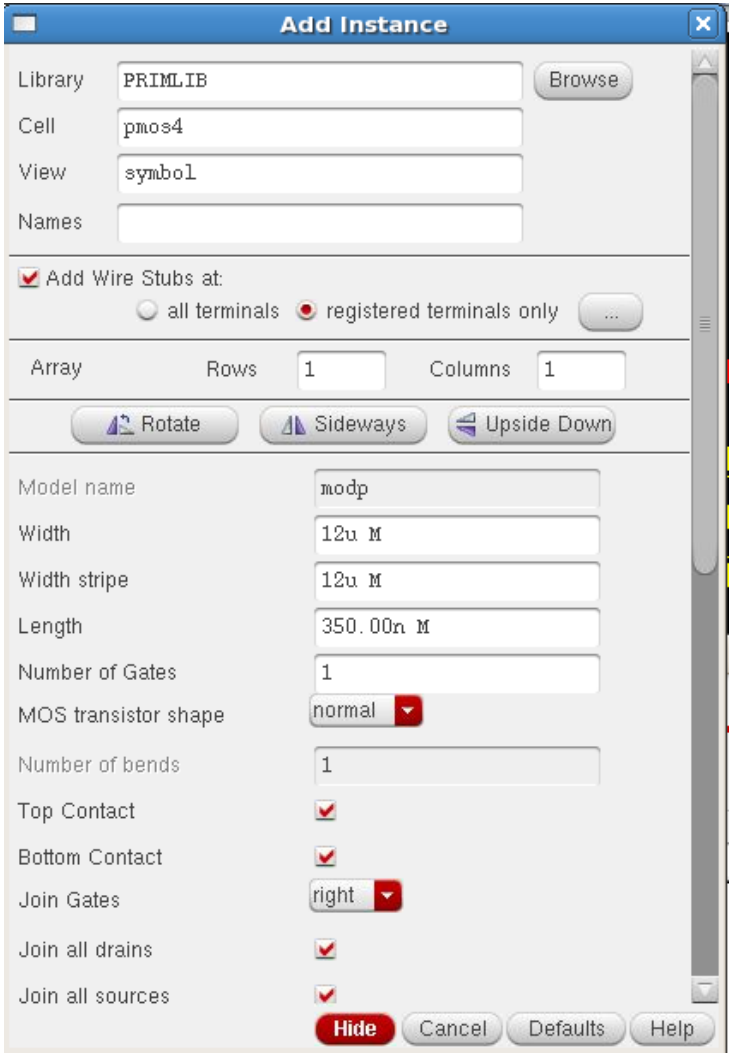
Layout in Cadence

- **In this lecture you will learn how to use the Cadence layout editor, called Virtuoso**
- **A cell has multiple cell views**
  - You have already created a schematic view and a symbol view
  - Today we will create the layout view
- **All the views can be seen in Library Manager**



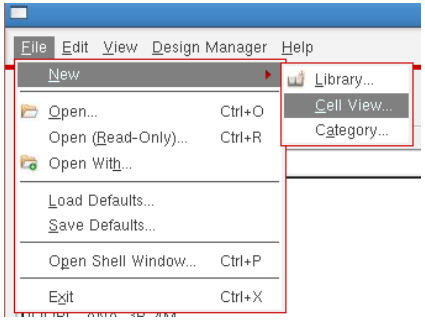
Create a new inverter cell with fixed dimensions

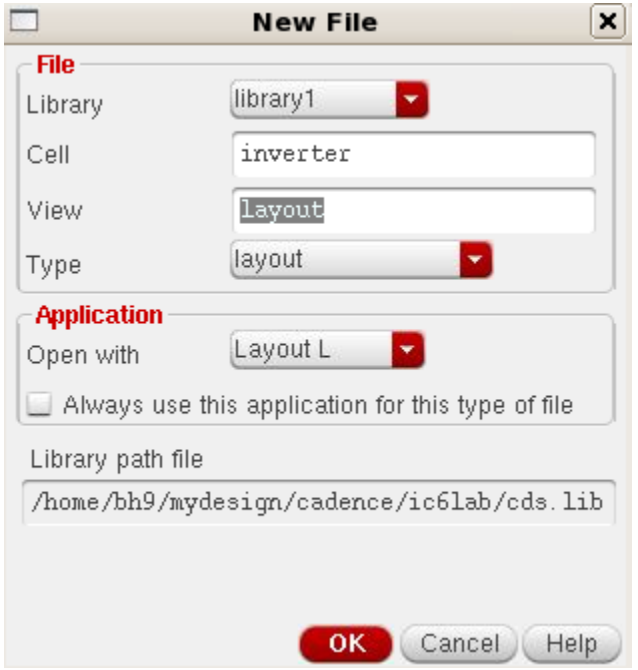
- For layout, we need a fully defined schematic
- The inverter schematic from the last lecture does not have fixed dimensions (we used pPar(“”))
- We must create a new inverter schematic with fixed dimension as follows :
  - NMOS 4u/0.35u
  - PMOS 12u/0.35u
- Create a symbol view for your new schematic



Create a layout view fro your inverter

- From the Library Manager, start LayoutL
- Choose New - Cell View
- You need to create a layout view from your schematic

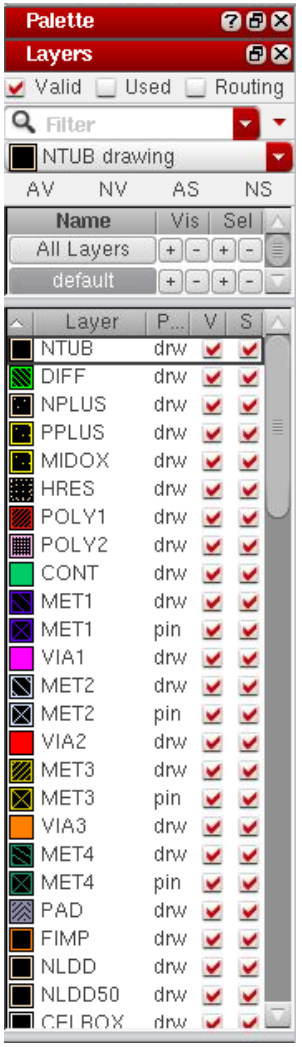




- Two windows will open, the LSW and the empty layout view

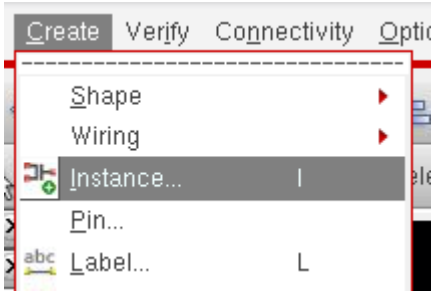
About the LSW

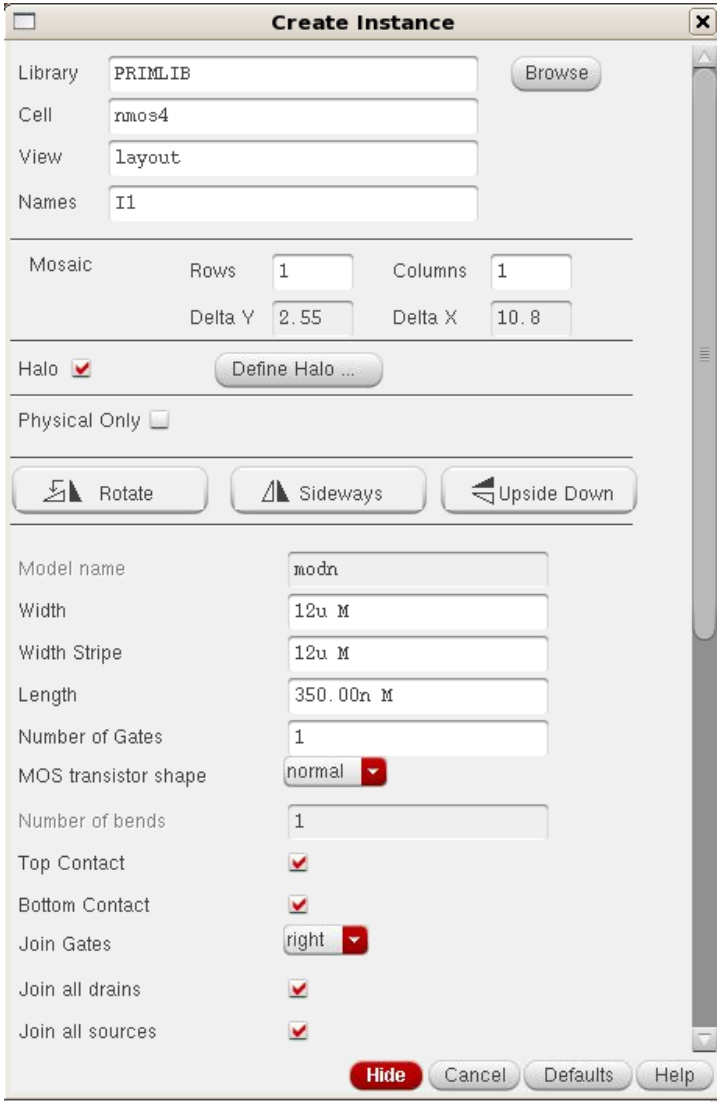
- **The layer selection window (LSW) shows all the layers you can use in the layout**
- **There are LOTS, however you will only need to use the ones towards the top (MET1, POLY1, NTUB, NPLUS, PPLUS)**
- **Each layer has a number of entries in the LSW, the one you need to use is the 'drawing' layer 'dg'**
- **The buttons at the top are useful:**
  - AV: all visible, NV: none visible
  - AS: all selectable, NS: none selectable



Placing the transistors

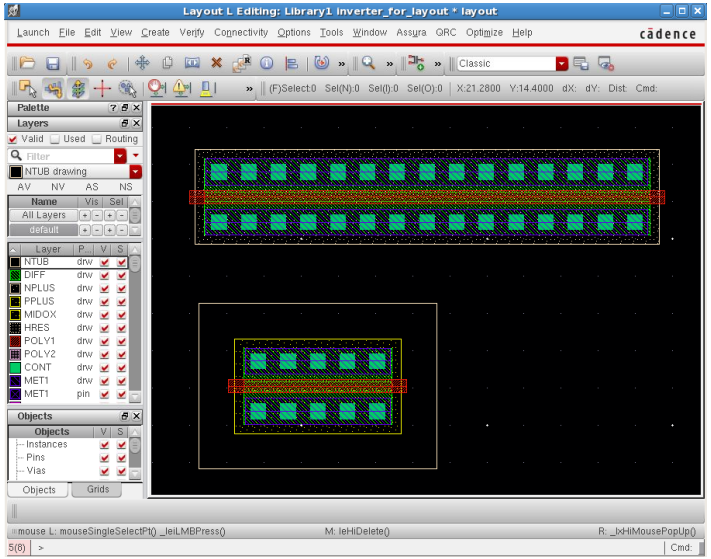
- **Add Instance from the Create menu**
- **You need two transistor from PRIBM lib with the following dimensions**
  - NMOS 4u/0.35u
  - PMOS 12u/0.35u

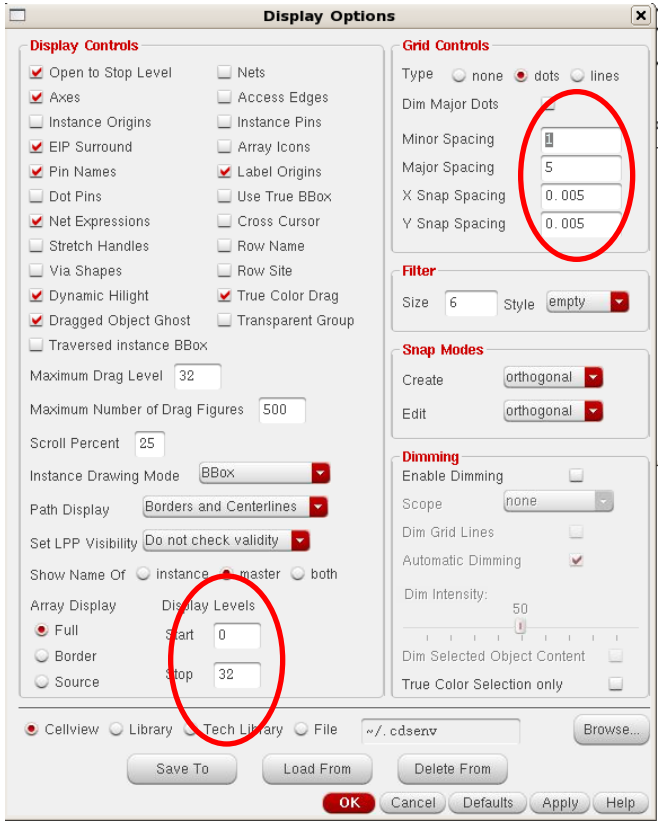




Selecting the display layers

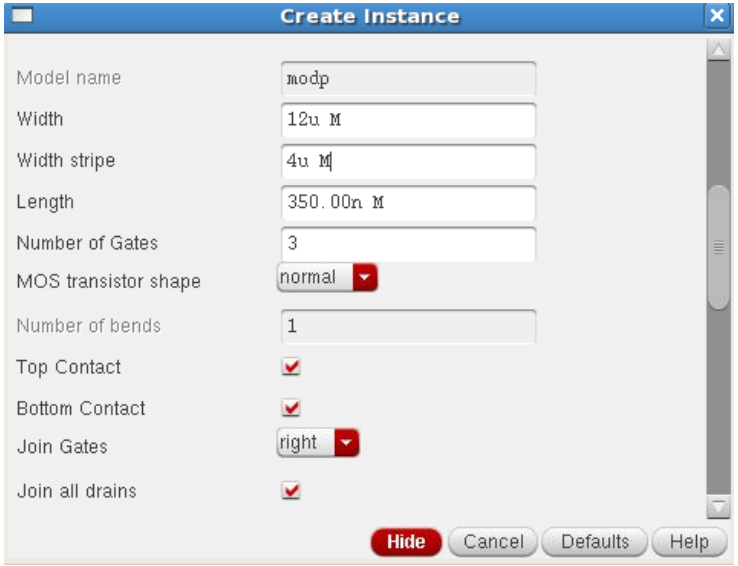
- If you cannot see the transistors, you may not have enough layers selected.
- Go to display->options
- Change settings as below





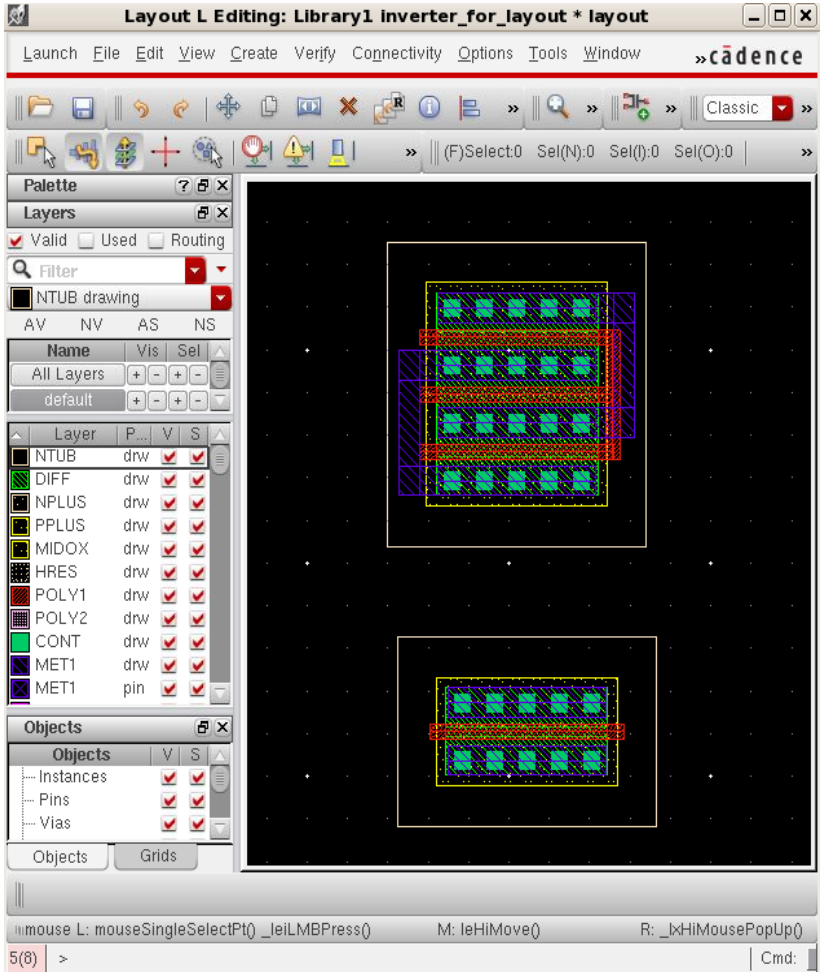
Customising the pcells

- **LayoutL has traversed our schematic and figured out that we have two transistors**
  - NMOS 4u/0.35u
  - PMOS 12u/0.35u
- **It has saved us a huge amount of time by creating the transistor structures for us using pcells**
- **We can customise the way the transistors have been generated by looking at the properties**
- **Change the number of gates to '3'**



Customising the pcells

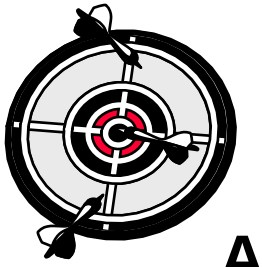
- The pcell has been regenerated with three gate strips.
- Play around with the properties of the pcell, to see how it affects the generated transistor
- You can see that the PMOS has an nwell around it



Basic layout operations

- Move items using ‘m’
- Stretch using ‘s’
- Move around layout with arrow keys
- Right click zooms as usual
- Shift ‘z’ zooms out
- Fit the layout with ‘f’
- Control ‘d’ deselects everything (very useful)
- Create a rectangle with ‘r’
- Create a via with ‘o’
- Create instance with ‘i’
- Create a path with ‘p’
- Create a pin with control ‘p’
- Chop with shift ‘c’
- Split with control ‘s’
- Add ruler with ‘k’
- Delete all rulers with shift ‘k’
- For options press F3

Learning Outcomes

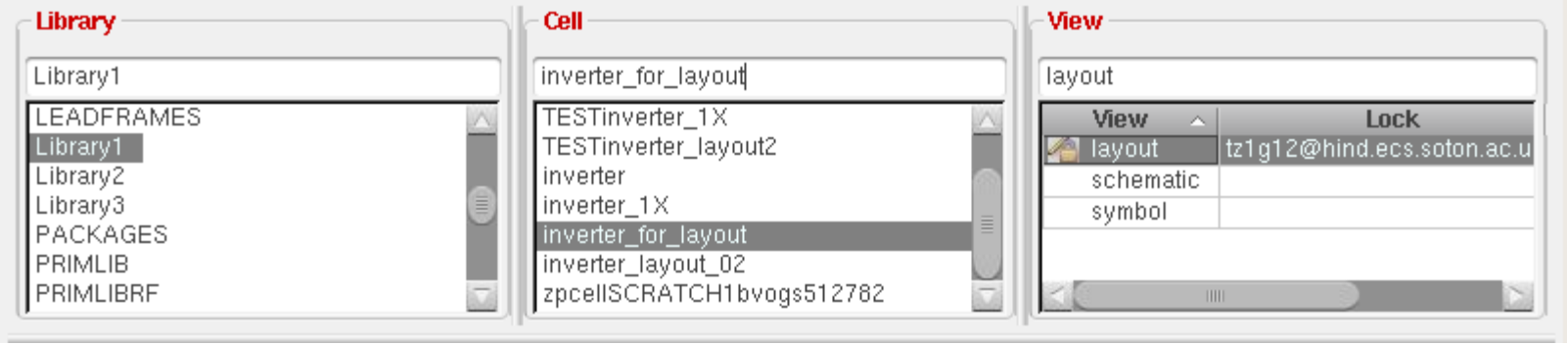


After completing this unit, you should be able to:

1. **Use LayoutL to place transistors in a layout**
2. **Construct a simple layout, step by step**
3. **Use the DRC checking tool**
4. **Search and explain errors**

Back to manual layout

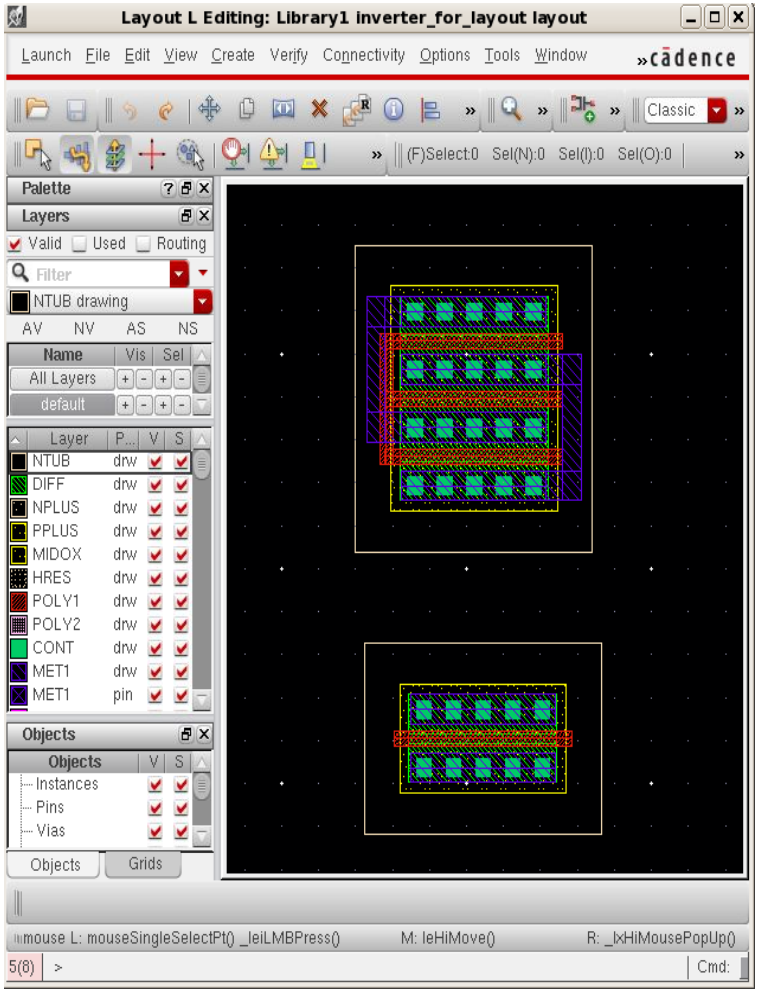
- Now we have used LayoutL to create the transistors, we will do the rest manually.
- Stop LayoutL by saving the layout, then closing it and opening from Library Manager



- In the case of an inverter, it is probably just as easy to create the transistors manually.
- LayoutL is useful for large schematics

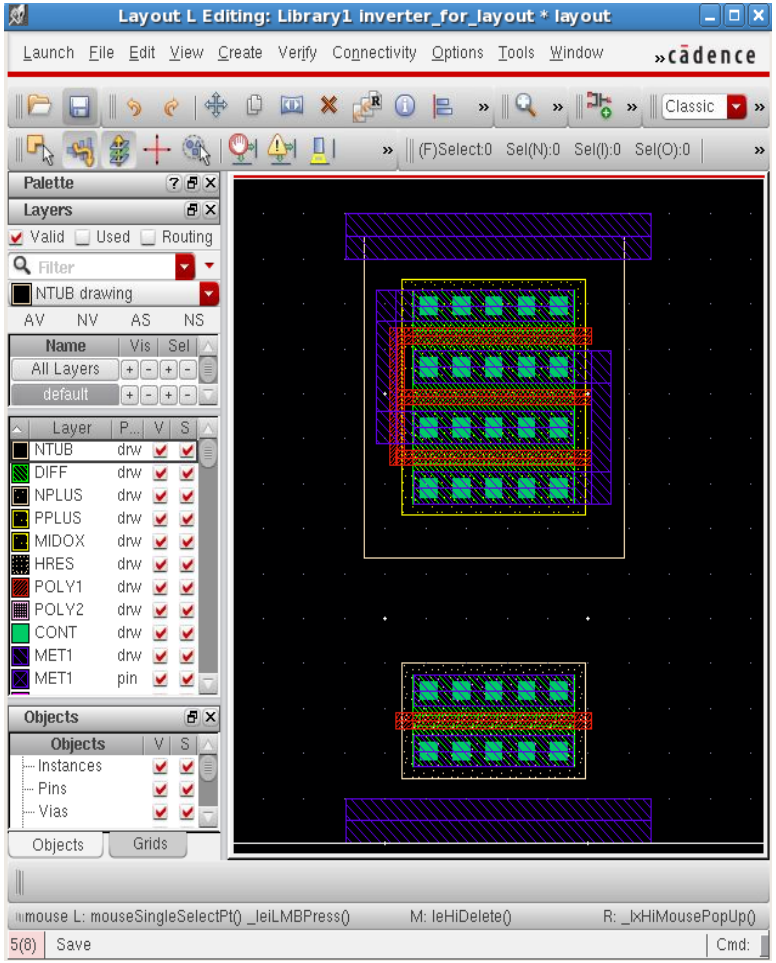
Creating the inverter layout, step by step

- To begin with we have the PMOS and NMOS transistors
- Make sure they are in line, and 3.3um apart
- Use rulers ‘k’ to measure
- If you need to flip the PMOS, use ‘m’ for move, then press F3 and in the options form press the ‘sideways’ button



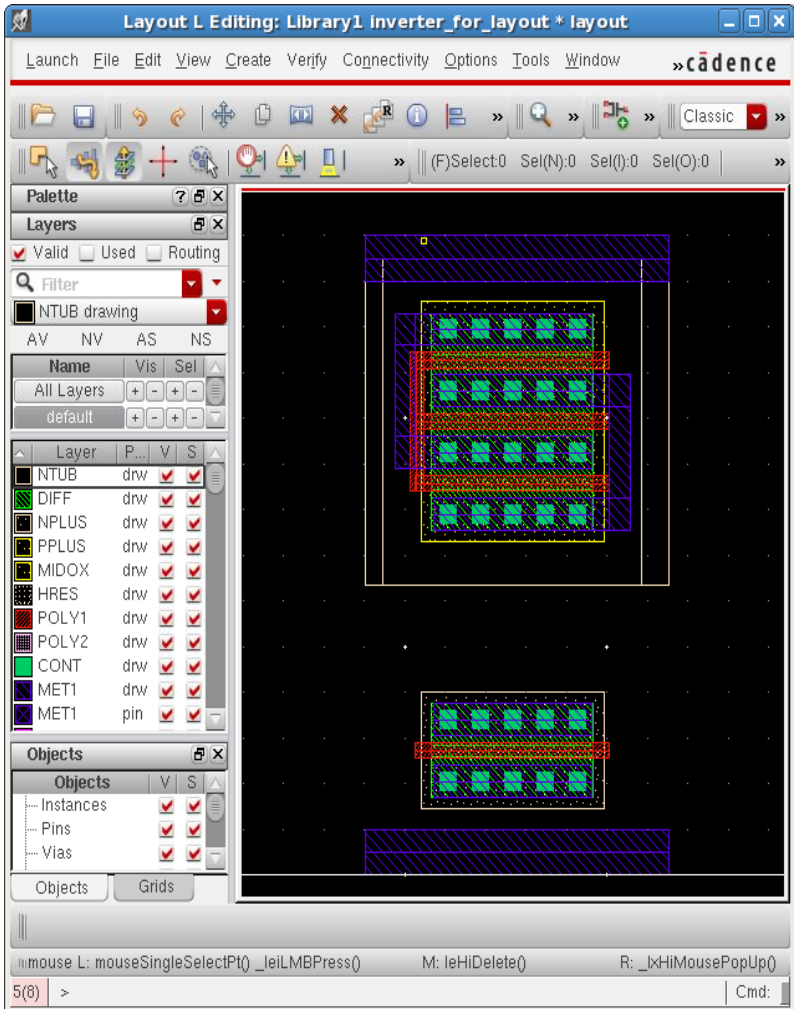
Creating the inverter layout, step by step

- Draw the metal vdd and gnd paths
- Make sure that MET1 dg is selected in the LSW
- Use the path command ‘p’ to start the path, and press F3 to bring up the options
- Set the width to 1um
- Make the paths 0.7um above/below the other MET1



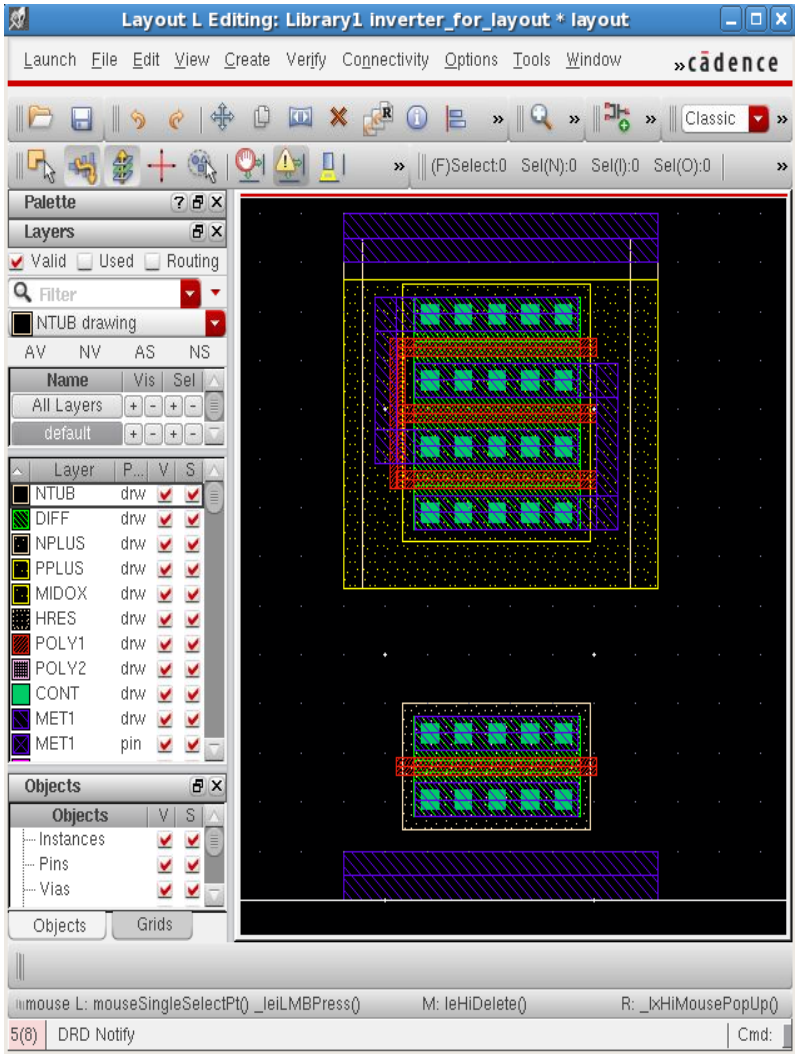
Creating the inverter layout, step by step

- Extend the N tub
- Select NTUB in the LSW
- Draw a rectangle with ‘r’
- Draw the N tub from the top left of the vdd MET1 to the bottom of the N tub generated by the PMOS pcell



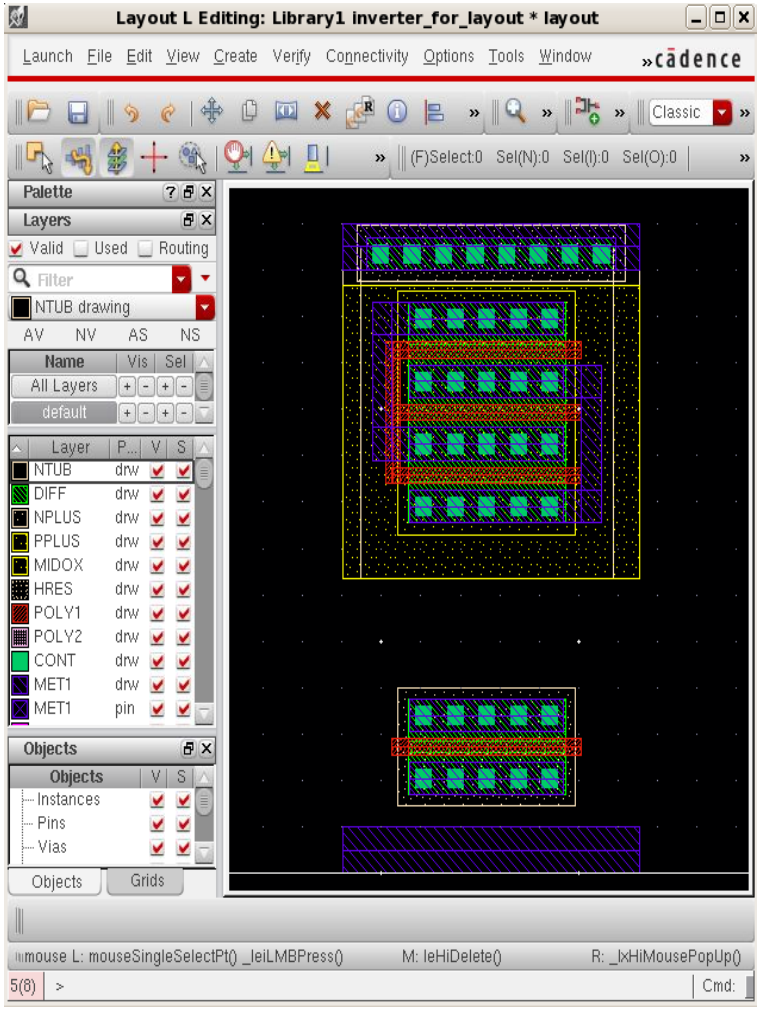
Creating the inverter layout, step by step

- Extend the PPLUS
- Select PPLUS in the LSW
- Use ‘r’ to draw the rectangle shown
- Extend above the PPLUS generated by the PMOS pcell by 0.5um



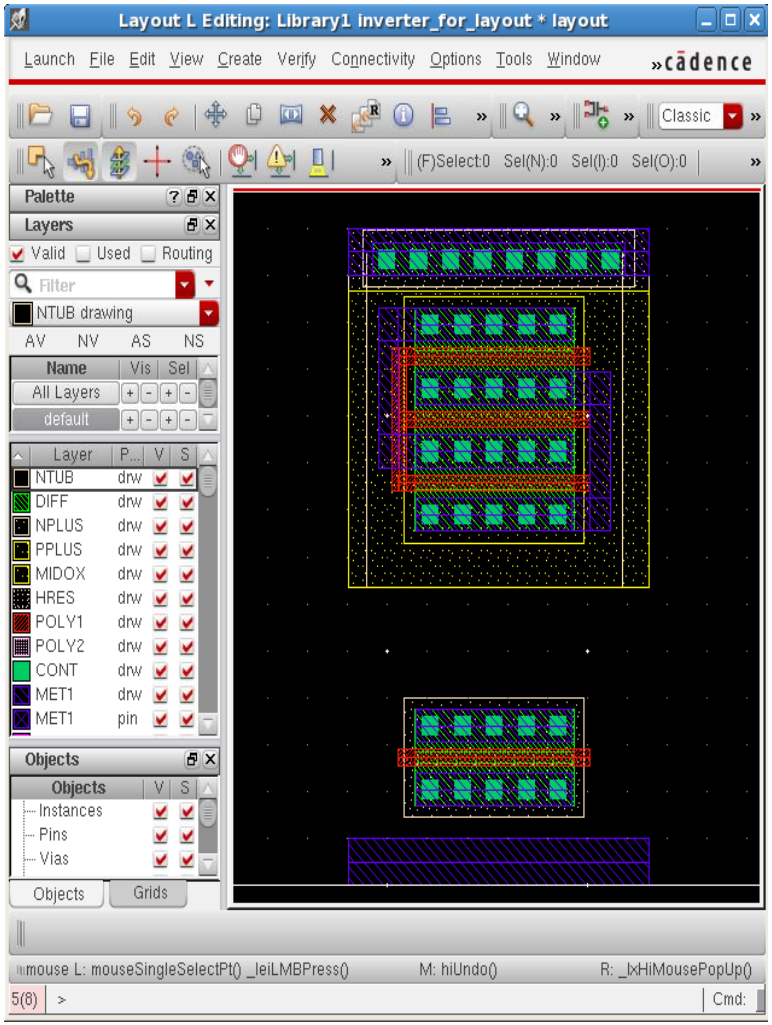
Creating the inverter layout, step by step

- Add taps to the PPLUS
- Press ‘o’ for add contact
- Select the ND contact
- Choose 8 columns
- Place the array centrally above the existing PPLUS by 0.1um



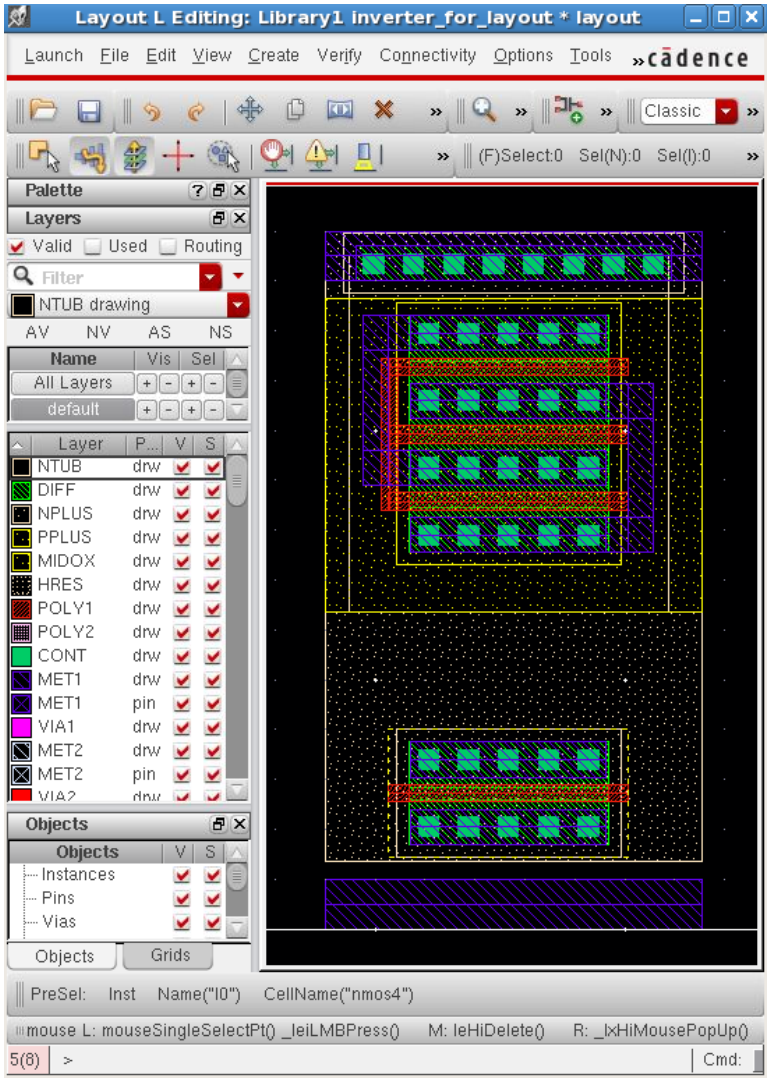
Creating the inverter layout, step by step

- Extend the contact NPLUS
- Select NPLUS in the LSW
- Draw a rectangle ‘r’ from the top left of the vdd MET1 to the top of the PPLUS



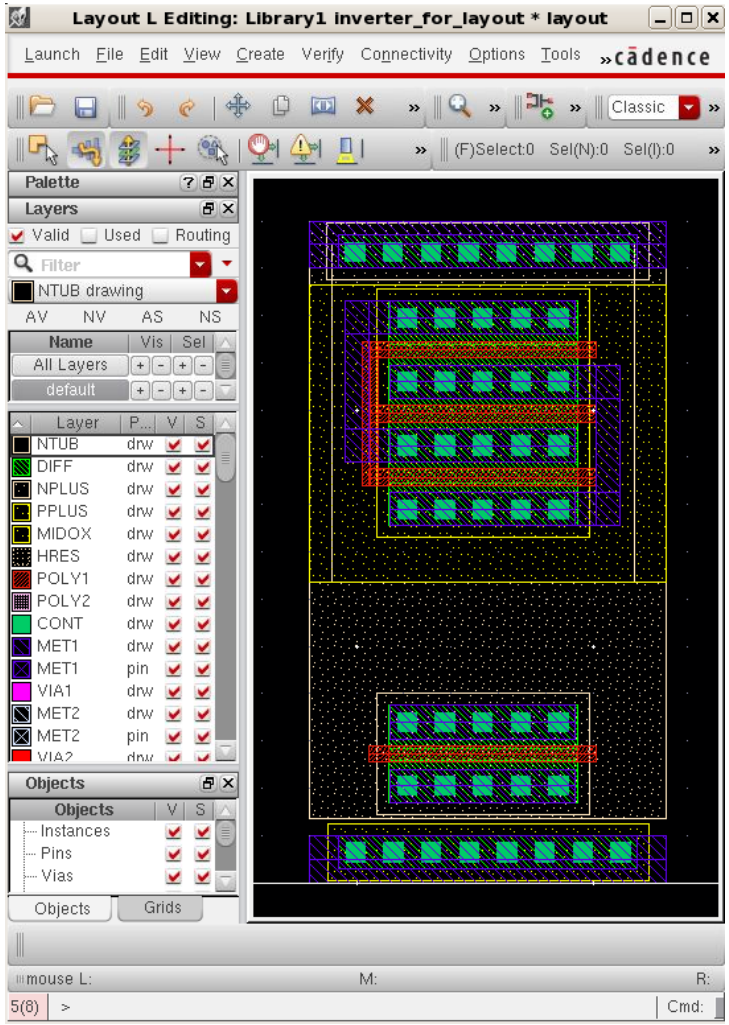
Creating the inverter layout, step by step

- Extend the NPLUS around the NMOS
- Select NPLUS from the LSW
- Draw a rectangle with ‘r’
- Join it to the PPLUS of the PMOS
- Finish 0.1um below the NPLUS generated by the NMOS pcell



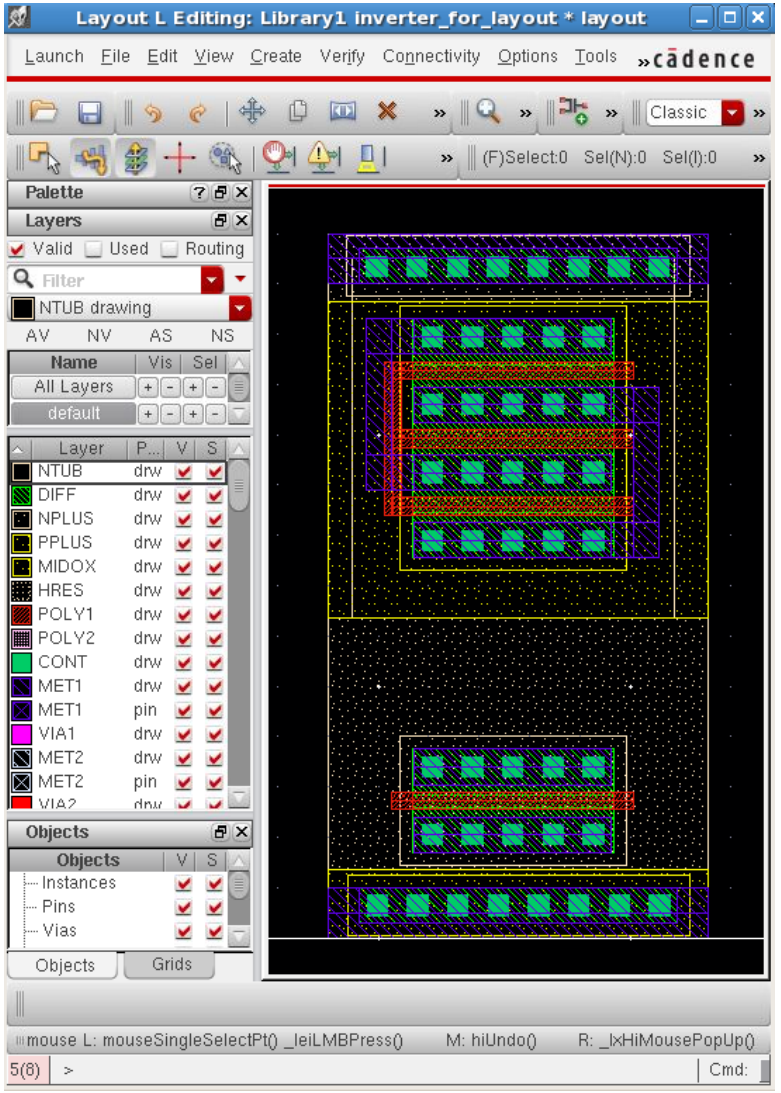
Creating the inverter layout, step by step

- Place the NPLUS contacts
- Press ‘o’ for contact
- Choose the PD contact
- Set columns to 8
- Align the array centrally and 0.1um below the NPLUS



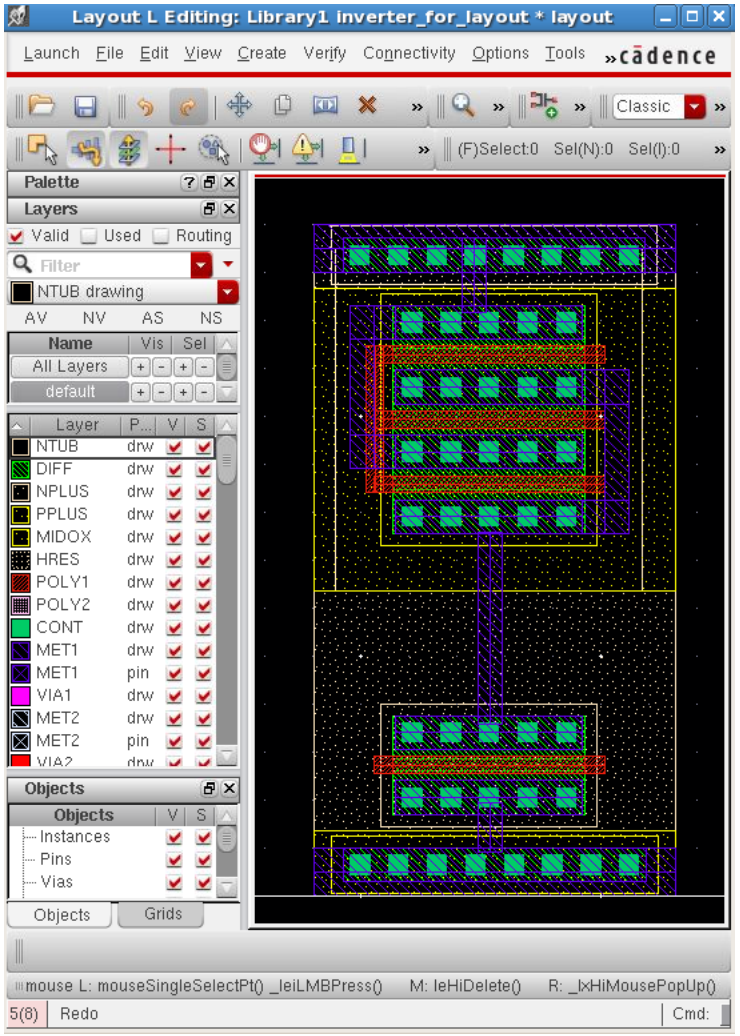
Creating the inverter layout, step by step

- Extend the PPLUS around the contacts
- Select PPLUS from the LSW
- Draw a rectangle with ‘r’
- Start from the bottom right of the gnd MET1 and join to the NMOS NPLUS



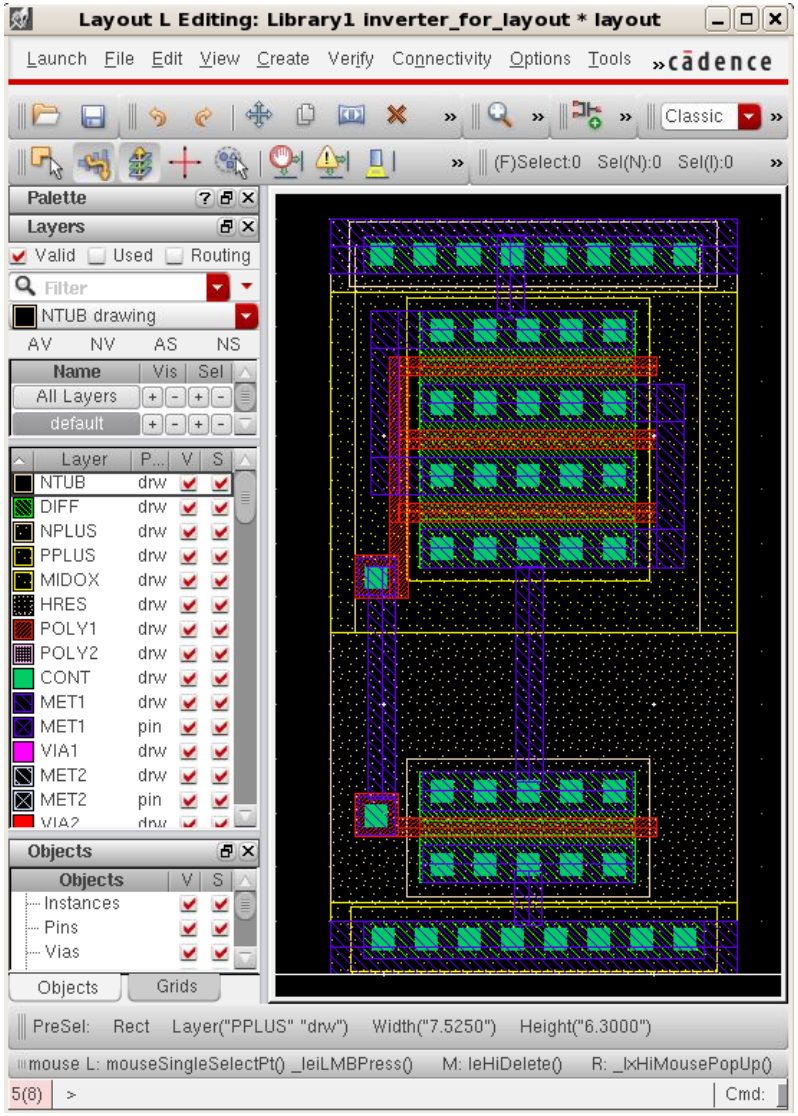
Creating the inverter layout, step by step

- Add metal connections
- Select MET1 dg in the LSW
- Draw path with ‘p’
- Press F3 while drawing the path to get the options box
- Change the width to 0.5um
- Draw the paths as shown



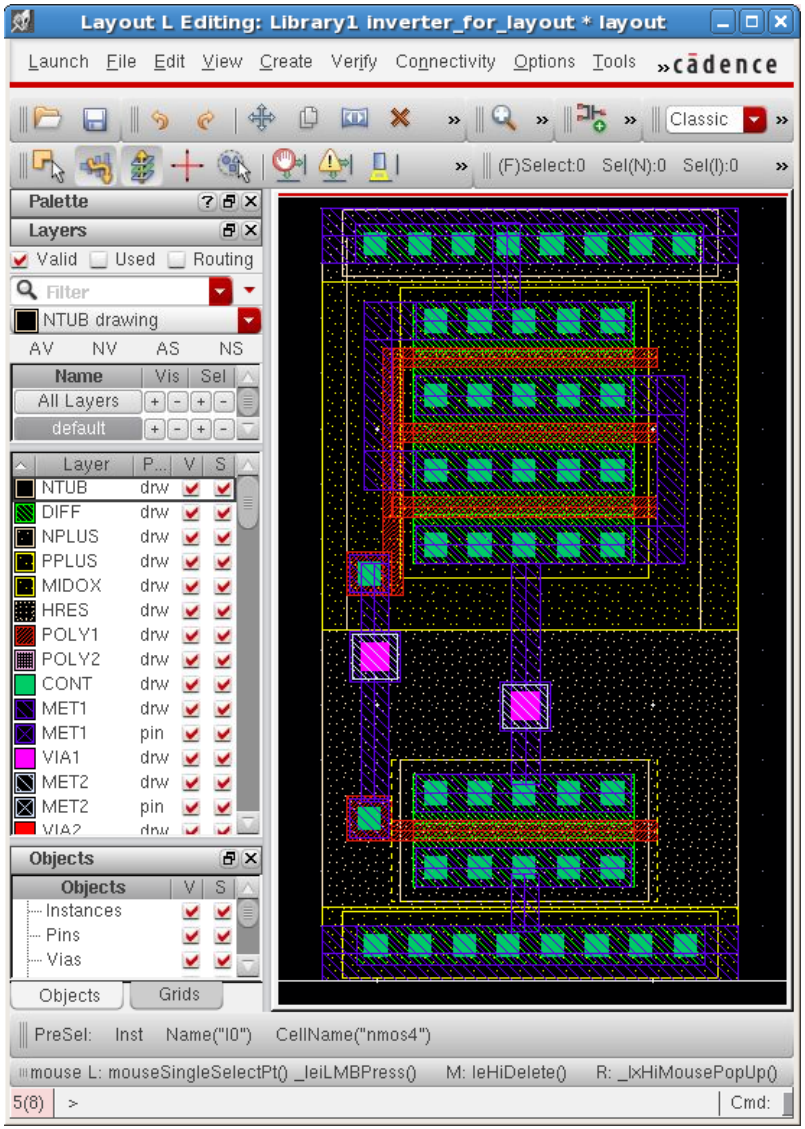
Creating the inverter layout, step by step

- Connect the gates
- Press ‘o’ for contact
- Choose P1 contact
- Place as shown
- Add POLY1 path to connect gates to contacts
- Add MET1 path to connect the contacts together



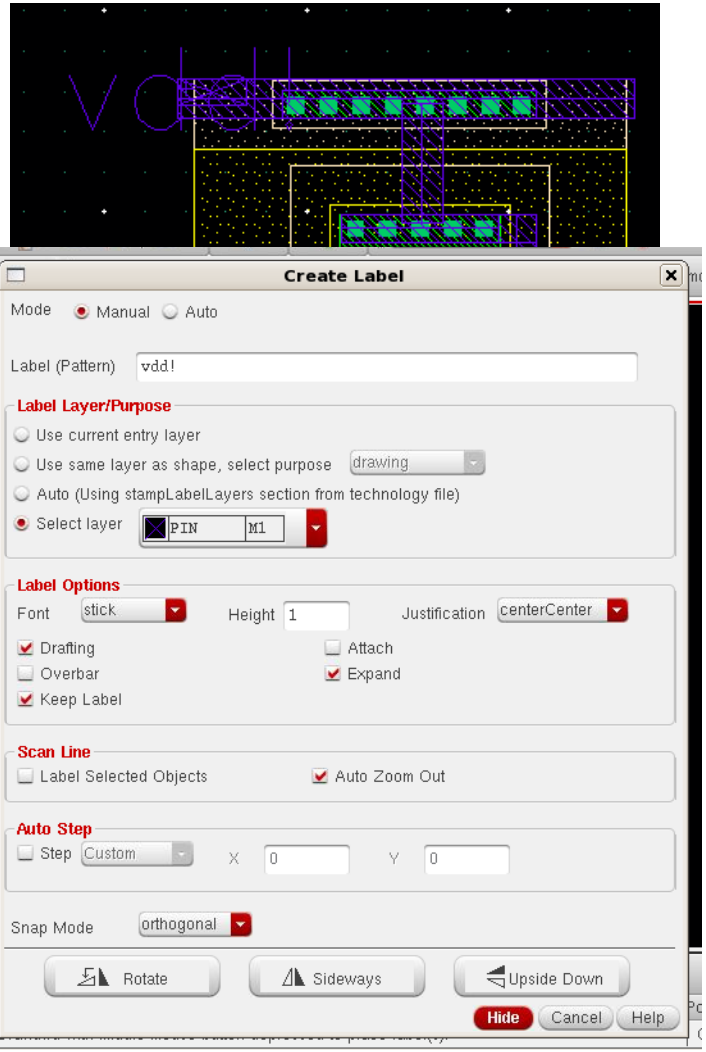
Creating the inverter layout, step by step

- Add MET2 contacts
- Press ‘o’ to add contact
- Choose VIA1 contact
- Place as shown

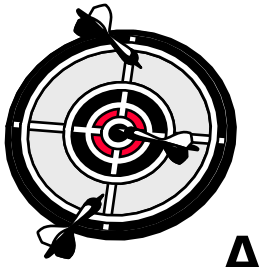


Creating the inverter layout, step by step

- Add LABELs.
- select ‘Create’ → ‘Label’.
- Add ‘vdd!’ first. Make sure MET1 is selected for vdd/gnd, MET2 for A/Y.
- You must name the nodes to match with the schematic view: A, Y, vdd! and gnd!.
- Generally, the labels are created for metal1 layers. In the Layers tab select the layer PIN metal1.
- If you feel necessary, change the Height size to about 0.5.
- Important: Do not forget to select the layer PIN metal1 before you create the label. For instance, in the figure, we have vdd! with metal1. Therefore, we have selected PIN metal1 in the Layers and just after that we have created the label. Note that in the figure, the '+' defines the layer that is associated to the label.



Learning Outcomes



After completing this unit, you should be able to:

1. **Use LayoutL to place transistors in a layout**
2. **Construct a simple layout, step by step**
3. **Use the DRC checking tool**
4. **Search and explain errors**

Running the DRC check

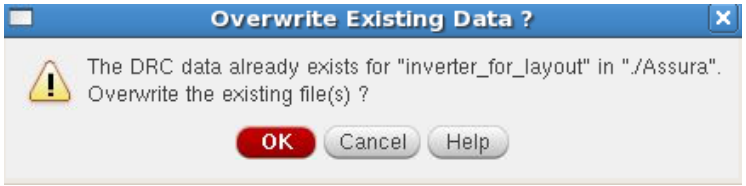
- **Now you must check if there are any errors in your layout, that is, you have to perform the *Design Rule Check* (DRC).**
- **In this tutorial, the** Assura **software will be used. Thus, select** Assura → Run DRC **in the layout editor.**

Running the DRC check

- **For now, just specific rule validations will be checked. A group of rule validations is commonly known as** switches**. You can find them in the window** Run Assura DRC**. To define the switches you should select** Set Switches **and then with the** CTRL **key you can select more than one switch. Some key information about the technology we are using in this tutorial:**
- **Until the final stage of the layout of circuit, one can use the switches:** no_coverage **and** no_generated_layers**.**
- **During the phase that we are more interested in the drawing rules violation, one can use also the switches:** no_erc andno_info**.**
- **All the other DRC parameters must not be changed.**

Running the DRC check

- **If you repeat the DRC and if there is already previous data,** select OK to overwrite and OK to stop seeing the current one. After that, select Yes to display the results.



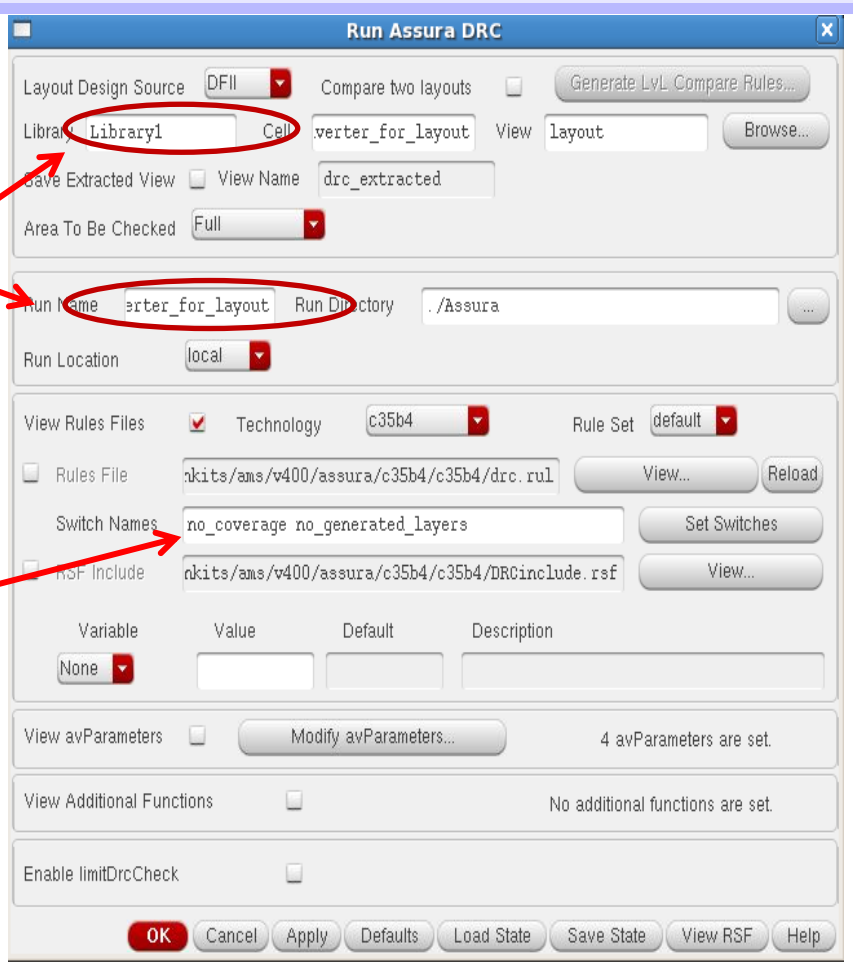
Running the DRC check

- **In the RUN Assura DRC window:**

1. The Cell name should be the same as your Run name.
2. Technology should be chosen by c35b4
3. The design rule file should be

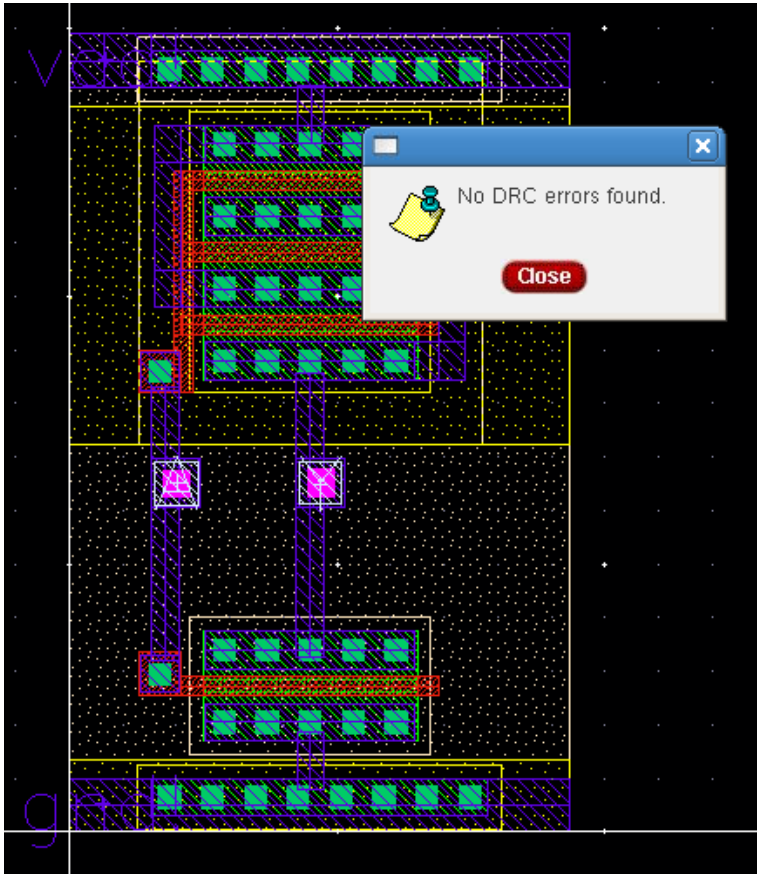
home/designkits/ams/v400/assura/c35b4/c35b4/drc.rul

4. Select the switches no_coverage and no_generated_layers



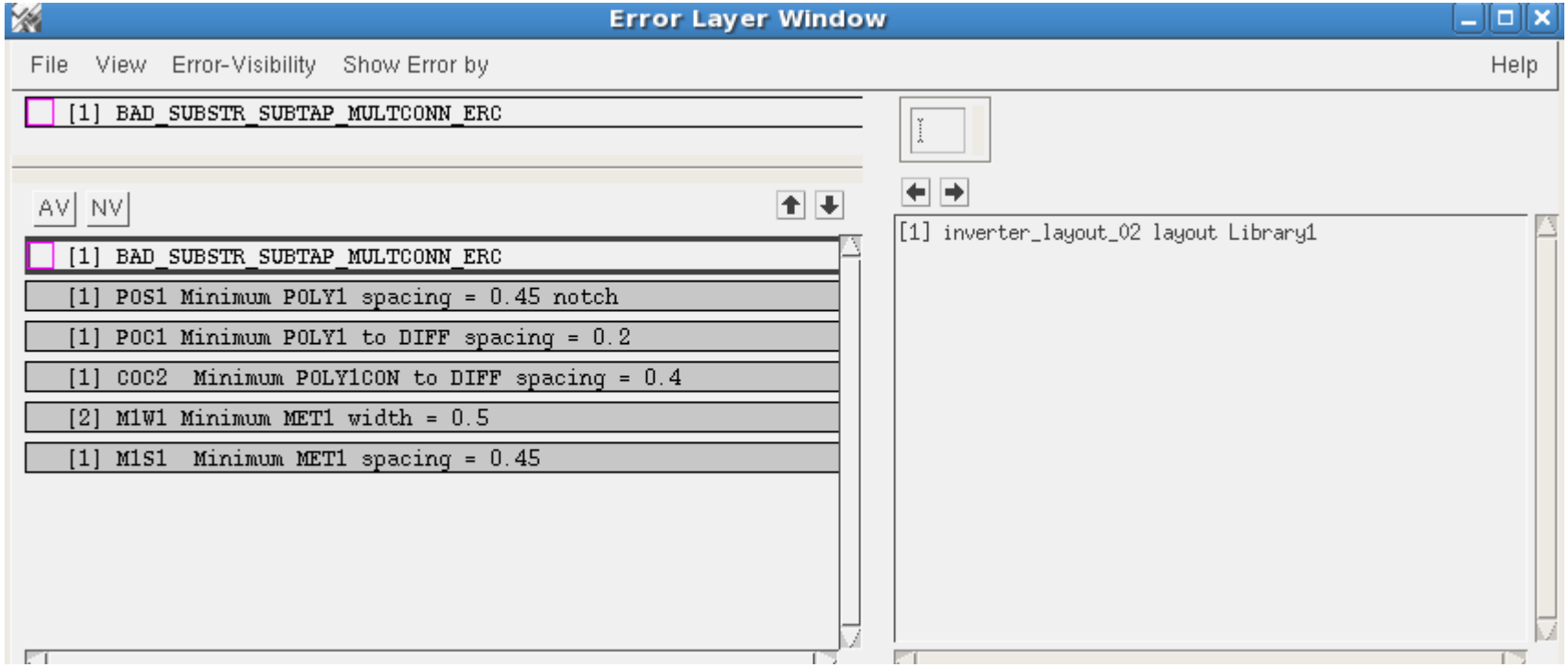
Running the DRC check

- **Ideally you should get no DRC errors!**



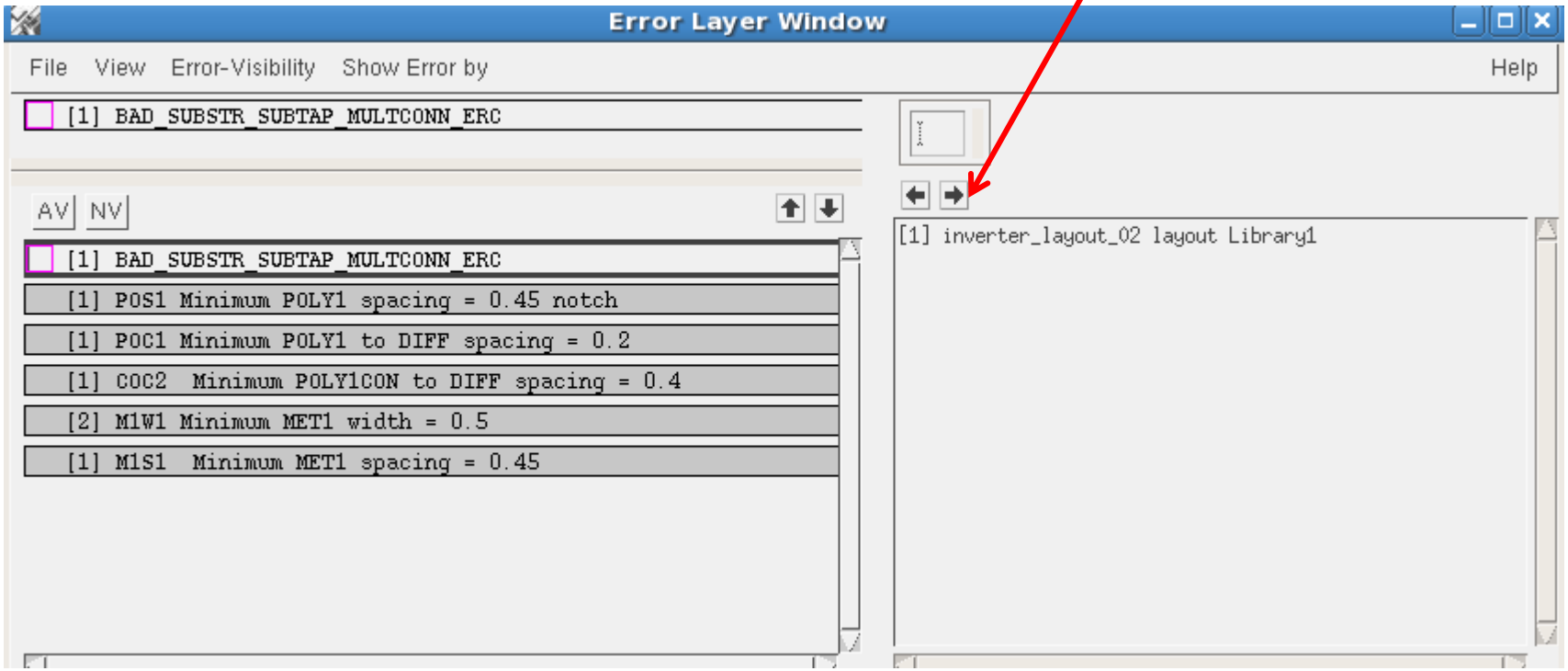
Lots of errors

- But you will typically get many, many errors
- This is normal – one small thing can cause many errors



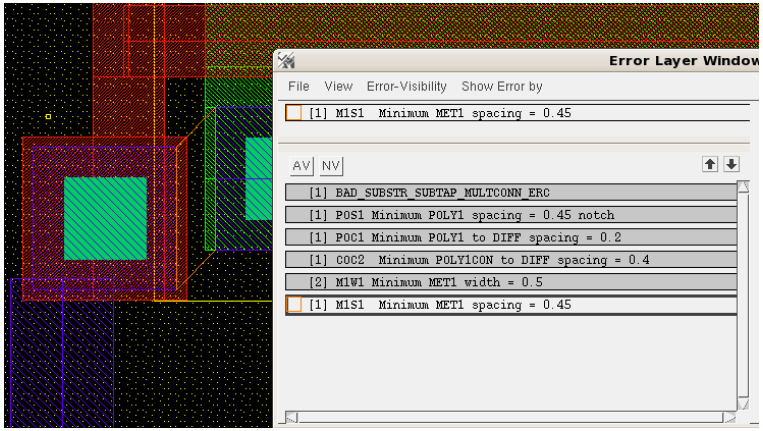
How do we find the errors?

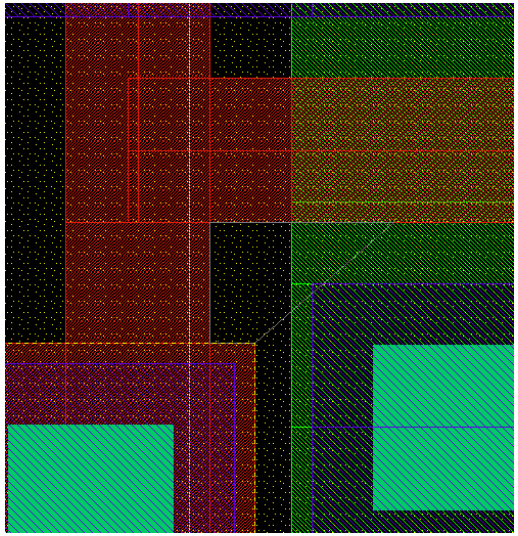
- You can select a fault and click on the arrow and the tool will zoom in to the location of your specific DRC error.



How do we find the errors?

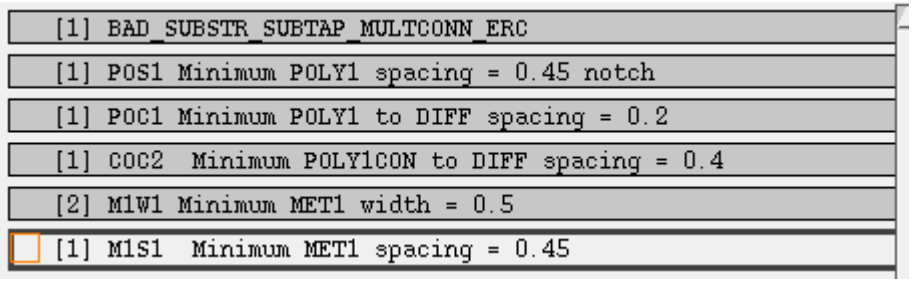
- In this case: contact is too close to the diffusion.
- If we want details on an error, use the explain marker tool then click on the error.





How do we find the errors?

- This will list the reason for all markers which are beneath the place you clicked



- You can check the correct spacings, then using a ruler ‘k’ you can correct the layout

DRC Examples

```
   CPU TIME = 00:00:01  TOTAL TIME = 00:00:04
********* Summary of rule violations for cell "counter4bit layout" *********
 # errors  Violated Rules
       2  INFO: hot nwell
       1  Label/Pin is on a net with a different name
       1  M1R1 Minimum density of MET1 area [%] = 30
       1  M1S1  Minimum MET1 spacing = 0.45
       1  M2R1 Minimum density of MET2 area [%] = 30
      13  M2S1 Minimum MET2 spacing = 0.5
       1  M3R1 Minimum density of MET3 area [%] = 30
       1  M4R1 Minimum density of MET4 area [%] = 30
       5  ODC3 Minimum NDIFF to HOT_NTUB spacing (no PTAP in between) = 2.6
       1  POR1 Minimum density of POLY1 area [%] = 14
      27  Total errors found
```

DRC Examples

- **2 INFO: hot nwell**

  One of the reasons for this errors VDD is not connected to the N-well

  For digital design: the best bet is to create a new layout cell view, that you instantiate the imported cell into, that connects VDD and GND correctly.

DRC Examples

- **Multiple Stamped Connections**

You may have a short through the substrate or nwell

This kind of error might indicate that you have more than one well contact, with the metal connected to different nets. This means you've got a "soft connect" through the well (not quite a short, because the well is resistive). It may be that you're making a connection via the well, which is almost certainly not what you want!

DRC Examples

- **Latchup rule LAT3 distance s/d diff pgate net_welltap > 20**
- This error could be generated if the distance between the s/d region and the welltap is larger than 20. To avoid such an error, keep the distance btween your transistors and VDD or GND less than 20

What about the metal minimum area errors?

- **M1R1 Minimum density of MET1 area**
- This means that the amount of metal1 shapes in your design is less that 30% of the chip area. 30% is the minimum required. Density is very important for planarity and pattern etching. It is important to avoid the dishing/
  erosion in the modern nanotechnologies with Copper BE.
- In fact the vendor will solve this problem by adding 'dummy' MEt1shapes into your layout.
- In our case, use the no_erc switch when you do DRC

Summary

- LayoutL can be used to automatically place the transistors in a layout
- There are many shortcut keys to learn for layout
- The DRC check and error correct cycle takes the majority of your time during layout
- DRC errors can be viewed on the layout directly and then explained, or searched for
- There are many many advanced layout techniques

Lab: Layout

Objective: Create the layout for your inverter design. DRC check the design and correct errors until the design is error free