Symbols & Simulation

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Custom Design Flow



Learning Outcomes



After completing this unit, you should be able to:

- Create a symbol from a schematic
- Set up the simulation environment
- Simulate your design
- Plot the results
- Use parameter passing and design variables
- Use parametric analysis

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Set up the current working directory

- The first step is to set up the local working directory for the AMS 0.35µm process.
- open a new terminal and type the following: tcsh
 - source /opt/esdcad/scripts/ams_v400_tcshrc

Run Cadence Design Manager

This will bring up the Cadence Design Manager:

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Create an inverter schematic

- Add a PMOS and NMOS transistor to a schematic from the PRIMLIB library with the following dimensions:
 - NMOS 4u/0.35u
 - PMOS 12u/0.35u

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View	symbol		
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Create an inverter schematic

Then wire them up using the add wire command



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Connecting things up...

- In Cadence we can add pins for inputs and outputs.
- For Vdd and Ground we use globals.
- Cadence includes symbols which are inherently global e.g. vdd and gnd.

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Adding Pins

Specific pins (inputs and outputs) are added using the <u>Create</u> -> Pins command

Remember to specify the direction

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Creating a symbol from a schematic

To create a symbol from a schematic then we can use the create cell view -> from cell view command in the <u>Create</u> menu

	Cellview From Cellview	X	Library Name	C	ell Name	View Name	
			library1	in	verter	symbol	
Library Name	library1 B	rowse	Pin Specification	ns		Attrit	butes
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From View Name	schematic		Right Pins	ү			ist
To View Name	symbol		Top Pins				ist
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			🖲 None 🔾 A	All 🕥 Only these:			
Display Cellview	✓						
Edit Options	✓		Load/Save 📃	Edit Attributes	Edit Labels	Edit Properties	
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Symbol Generation Options

Symbol Creation

- The symbol will be automatically created as shown
- Use the graphics commands from <u>Edit</u> menu : Move, Delete, Stretch and add to draw the symbol



Symbol Creation

Don't forget to SAVE the symbol

Close it and you will see the new cell view appear in library manager

Library Manag	er: Directoryme/bh9/mydesign/cadence/ic6lab	X
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Library Manag	per: Directoryme/bh9/mydesign/cadence/ic6lab	Aew View Lock Size schematic 31k symbol 23k
TECH_C35B3 TECH_C35B4 US_8ths andILlb analogLib basic basic basic		
functional library1 sbaLib		

- We can now use the new symbol in a hierarchical design or a test circuit
- From the library manager create new cell view, schematic and call it 'test_inverter'
- Use the Create-> instance command
- Place your new symbol

	Add Instance 🛛 🗙
Library	library1 Browse
Cell	inverter
View	symbol
Names	
🗹 Add W	ire Stubs at: Q all terminals e registered terminals only
Array	Rows 1 Columns 1
	🚯 Rotate 💦 🕼 Sideways 🖉 Upside Down
	Hide Cancel Defaults Help

Placing the symbol on a schematic

• We get the schematic looking like this:

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Analog test bench requirements

In an analogue test bench we need:

Inputs

 sources (dc, transient, ac) depending on the analysis to be carried out

Outputs

- Measurement models
- Loads

Supplies

- Vdd, Vpulse
- Ground
- gnd

test_inverter – test bench requirements

Inputs:

• pulse input source between 0 and 3.3V at about 100MHz

Outputs:

• capacitive load of about 1pF

Supplies:

• Vdd = 3.3V

Ground:

• gnd = 0V

Specifying the vpulse instance

analogLib -> vpulse

- v1 = 0
- v2 = 3.3
- delay = 1n
- rise = 1n
- fall = 1n
- pulse width = 5n
- period = 10n

	Add	Instance	×			
Library	analogLib		Browse			
Cell	vpulse					
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Names	[
Add Wire Stubs at:						
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Number of	noise/freq pairs	0				
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AC phase						
XF magnit	ude					
PAC magr	nitude					
PAC phas	e					
Voltage 1		0 ¥				
Voltage 2		3.3 ¥				
Period		10n s				
Delay time		ln s				
Rise time		ln s				
Fall time		1n s				
Pulse widt	h	5n s				
Temperatu	re coefficient 1					
Temperatu	re coefficient 2					
Nominal te	mperature					
Type of ris	ing & falling edge					
	-	lide Cancel Def	aults Heln			

Complete the test circuit

- Wire up the source and load
- Give the wires meaningful names: you can name a wire by selecting it then write click and selcet Add name from the menu



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The Cadence simulator

- Now we want to simulate this circuit using the Cadence simulator: spectre
- The simulator environment in Cadence is called Analog Design Environment (ADE) and allows you to run simulations and plot results
- Although it looks pretty boring(!) it is actually very powerful

How to start Analog Design Environment

Open your test circuit and go to Launch->ADE L.

This starts the ADE interface

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Launch Session Setup <u>A</u> nalyses <u>V</u> ari	ables <u>O</u> utputs <u>S</u> imulation <u>R</u> esults <u>T</u> o	ools <u>H</u> elp cādence
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		~
	Outputs	? # × 🜔
	Name/Signal/Expr Value P	'lot Save Save Options
		<u>No</u>
>	Plot after simulation: Auto	lotting mode: Replace
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You can see here we are using spectre simulator and that it has initialised the environment with our test circuit

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Types of simulation

We can choose from many different types of simulation

Click the choose simulation button

	Choosing	g Analys	ses ADE	L (4) X			
Analysis	🖲 tran	🔾 dc	🔾 ac	🔾 noise			
	🔾 xî	🔘 sens	🔘 dcmatch	🔾 stb			
	🔾 pz	🔾 sp	🔘 envlp	🔘 pss			
	🔾 pac	🔘 pstb	🔘 pnoise	© p×f			
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise			
	🔾 qpxf	🔾 qpsp	🔾 hb	🔘 hbac			
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	OK	Cono	ol Dofoult				
	Carlos Delaans Apply (Telp						

First we will set up a transient (i.e. time domain) simulation



Transient simulation setup

Different simulation accuracies are available

- Conservative is the most accurate but the slowest
- In this example we will run the simulation for 5 cycles (50ns)
 Choosing Analyses -- ADE L (4)

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	🔾 xf	🔘 sens	🔘 dcmatch	🔾 stb		
	🔘 pz	🔾 sp	🔘 envlp	🔾 pss		
	🔘 pac	🔘 pstb	🔾 pnoise	🔘 pxf		
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	🔘 qpxf	🔾 qpsp	🔾 hb	🔾 hbac		
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		Transient /	Analysis			
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✓ conse	rvative 📃 r	noderate	liberal			
Transient Noise						
Dynamic Parameter						
Enabled Options						
OK Cancel Defaults Apply Help						

Running the simulation

You need to add the Model Library before you run the simulation. Go to setup



Running the simulation

Use the 'Netlist and Run' (green arrow) button to run the simulation

ADE L (4) -	ibrary1 test_inverter schematic	_ 🗆 🗙
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	Outputs Name/Signal/Expr Value Plot Save Sa 1 vin Image: Constraint of the same set	ve Options
> Results in /home/bh9/simulation/test_inv	Plot after simulation: Auto Plotting mode: Repla	



A window pops up showing the progress of the simulation [/home/tzlgl2/6097/zty_demo_new_cadence/sim/test_inve_]

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primitives: writing primitives to rawfile. subckts: writing subcircuits to rawfile.	
26	

- There are many ways to plot a signal in ADE
- The easiest is with the Direct Plot option
- Choose Direct Plot -> Transient Signal



- Go to the schematic and choose the signals
 - Click a net for a voltage
 - Click a node for a current

Note the prompt at the bottom of the schematic

> Select nodes or terminals, press <esc> to finish selection

Plotting the signals

Select the input and output nets to plot the input and output voltages





Customise the waveform display

Right click on a waveform to change properties

- Waveform name
- Colour
- Right click and drag to zoom in
- f' to re-fit the graph
- 'H' for horizontal marker, 'V' for vertical



Notice slow rise time

Save your simulation state



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Lets optimise the rise time

- We want to change the size of the PMOS and see the effect on the rise time
- What is the best way of doing this?
- Important points:
 - Hierarchical parameter passing: from the schematic to the symbol
 - Design variables: schematic parameters which can be changed from ADE
 - Parametric simulations: run a set of simulations each with a different value for the design variable

Hierarchical parameter passing

- Open the inverter schematic
- Change the PMOS width and length properties to:
 - pPar("PW")
 - pPar("PL")
- Change the NMOS width and length properties to:
 - pPar("NW")
 - pPar("NL")

	Edit Object Properties	
Apply To Only curr	ent 🔽 instance 🔽	
Show 📃 system	n 🗹 user 🗹 CDF	
Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	PRIMLIB	off 🔽
Cell Name	pmos4	value 🔽
View Name	symbol	off 🔽
Instance Name	MPO	off 🔽
	Add Delete Modi	fy
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Model name	modp	off 🔽
Width	pPar("PW") M	off 🔽
Width stripe	pPar("PW") M	off 🔽
Length	pPar("PL") M	off 🔽
Number of Gates	1	off 🔽
MOS transistor shape	normal 🧧	off 🔽
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Top Contact		off 🔽
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Guard Bar Left	🔾 Diff 🔾 Cont 🖲 None	off 🔽
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Guard Bar Right	🔾 Diff 🔾 Cont 🖲 None	off 🔽
Guard Bar Bottom	🔾 Diff 🔾 Cont 🖲 None	off 🔽
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Drain diffusion area	1 Eo 10	off 📮

Hierarchical parameter passing

Recreate the symbol

This will create a symbol where you can set the widths and lengths for that symbol instance

Hierarchical parameter passing

- Go back to the inverter test schematic
- Re-instantiate the new inverter symbol
- Change the properties of the new symbol as follows Put in 'PWIDTH' for the PMOS width and keep the others the same
- only current 🔽 instance 🔽 Apply To Check and save Show 📃 system 📝 user 📝 CDF Reset Instance Labels Display Browse Property Value Display off Library2 Library Name off Cell Name inverter1X View Name symbol off off Instance Name 19 Add Delete Modify User Property Master Value Local Value Display rfaceLastCh. 17 11:32:31 2015 off 🔽 CDE E Value Display 0.35u off 10u off 0.35u off PWIDTH Previous Apply Defaults Next Help

Importing design variables in to ADE

- Go back to the ADE form
- We need ADE to pick up our PWIDTH design variable from the schematic
- Go to Variables->Copy From Cellview
- Notice that PWIDTH appears in the design variables
- Now double click PWIDTH to bring up the design variable box
- Set PWDITH to 10um initially



corgin + anabico	
Name	Value
PWIDTH	



Importing design variables in to ADE

- Re-run the simulation, to check everything is ok
- Should get the same as before, but now we have the ADE set up and ready to do cool stuff



Running a parametric simulation

- Parametric analysis allows you to run multiple simulations whilst varying design parameters
- We will run a parametric simulation during which PWIDTH will be varied

	Tools <u>H</u> elp Ca	
	<u>P</u> arametric Analysis <u>R</u> F ▶	
x	<u>C</u> alculator Results <u>B</u> rowser <u>W</u> aveform Results <u>D</u> isplay <u>J</u> ob Monitor	

Parametric Analysis - spectre(0): Library2 test_inverter schematic	
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Variable Value Sweep? Range Type From To Step Mode Total Steps Inclusion List Exclusion List PWIDTH Image: Step Mode Auto Auto	
	1
18 Move selected row up in the table	



Setting up the parametric simulation

Put PWIDTH in the parameter box and choose to vary it from 10u to 50u in 5 steps

Parametric Analysis - spectre(0): Library2 test_inverter schematic	
<u>F</u> ile <u>A</u> nalysis <u>H</u> elp	cādence
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Variable Value Sweep? Range Type From To Step Mode Total Steps Inclusion List Exclusion List PWIDTH 10u	
18 Configure what is shown in the table	

Run the parametric simulation

- Choose analysis -> start
- The log window will show progress of the runs
- Plot the output using the direct plot option as before
- Zoom into one cycle to examine the rise/fall times

```
2 parametric simulations remaining.

Info: Running PWIDTH=4e-05 1 remaining

Setting PWIDTH = 4e-05

compose simulator input file...

...successful.

start simulator if needed...

...successful.

simulate...

1 parametric simulation remaining.

Info: Running PWIDTH=5e-05 last run
```

Setting PWIDTH = 5e-05 compose simulator input file...successful. start simulator if needed...successful. simulate... reading simulation data...successful.

Info: Parametric Simulation Completed.

Configure what is shown in the table

Parametric results



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A few ways

- On an individual graph, use the marker facility
- Use the calculator
- Use horizontal markers

Trace marker





- Place a trace marker at 0.33V and 2.97V and read off the times

 Image: the times
 Image: trace marker at 0.33V and 2.97V and read off
- Rise time is 19.8-17.8ns
 =2ns



Use horizontal markets 'H'

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Use the calculator

• Very powerful collection of tools

Wirtuoso (R) Visualization & Analysis XL calculat	or – 🗆 🗙
<u>F</u> ile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: p_new_cadence/Sim/test_inverter/spectr	e/schematic/psf
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Off O Family Wave Cop V Cherrent exp	>> >>
Key 7 8 9 7 4 5 6 *	
	expr pi 1 11 expr pi 1 11 w
Stack	ð ×
VT("/vin") VT("/vin") VT("/vin") VT("/vin") VT("/in") VD("/inet2")	
Function Panel	Ð ×
Special Functions 🧧 🔍	
PN bandwidth compressionVRI dBm dftbb evmQpsk a2d clip convolve delay dnl eyeDiagram abs_jitter compare cross deriv dutyCycle fallTime average compression d2a dft evmQAM flip	fourEval gainE freq gainN freq_jitter getAs frequency group
19	

- Choose vt
- Choose the net on the schematic window
- Select the riseTime from Function Panel
- Choose 'y at x'
- Set initial and final x values (15ns, 20 ns)
- Press apply
- Press Evaluate

W Virtuoso (R) Visualization & An	alysis XL calculator 📃 🗆
<u>F</u> ile <u>T</u> ools <u>V</u> iew <u>O</u> ptions <u>C</u> onstants <u>H</u> elp	cādence
In Context Results DB: /home/bh9/simulation/test_inverter/sp	pectre/schematic/psf
🖩 acos acosh asin asinh atan atanh cos cosh sin	sinh tan tanh
III 1/x 10**x abs dB10 dB20 exp int In log10 sqrt	×**2 y**×
mapp plot erplot	
• vt vf vdc vs op var vn it if idc is opt mp vn2	⊖ sp ⊖ vswr ⊖ hp ⊖ zm ⊖ zp ⊖ yp ⊖ gd ⊖ data
🜔 Off 🔾 Family 🔾 Wave 🔽 Clip 🥼 🐗 Append	🔽 Rectangular 🔽 🍪 📃
riseTime VT("/ dut") 15n t 20n t 10 90 nil "time 7 8 9 / 4 5 6 * 1 2 3 -	a" 🛛
	B
riseTine	
Signal VT("/vout")	•
Final Value Type V at x	Initial Value 15n
Percent Low 10	Parcent High 90
Number of occurrences single	Plot/print vs. time
	QK Apply Defaults Close Help
Function Panel Expression Editor	
Successful evaluation	

Plots the rise time with different values of the PMOS width

Summary

- In this lecture we created a symbol from a schematic
- We made a test schematic containing the symbol
- We learnt how to simulate the design
- We have seen how to plot and measure the results
- We have shown how to set up hierarchical parameter passing in your design
- We have used design variables and parametric simulations to show rise time variation against PMOS width

Lab: Simulation

Objective: Create a symbol and test circuit. Then simulate your test circuit and use parametric simulations and design variables

