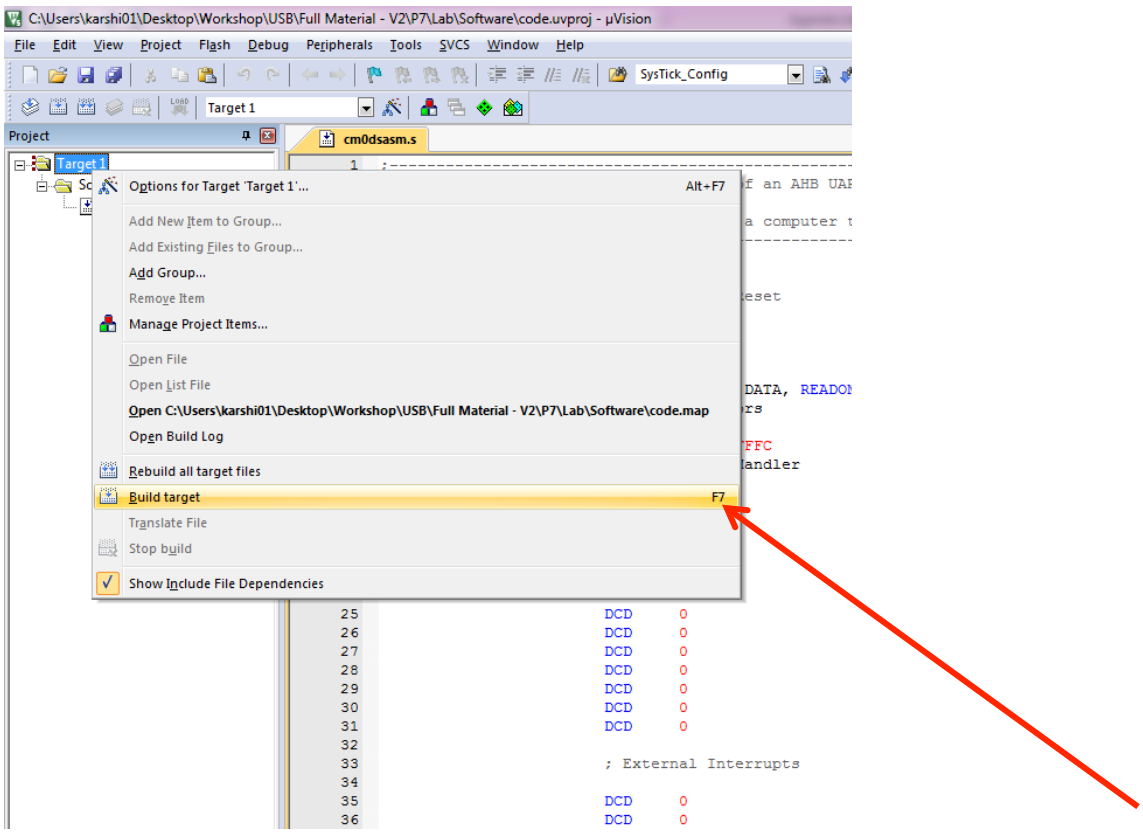
UART and PSRAM Integration

SUMMARY

1. Compile the Software using KEIL MDK ARM and generate code.hex file
2. Download code.hex onto PSRAM
3. Open FPGA project under Vivado and implement the design
4. Use Vivado hardware manager to download the .bit file
5. Communicate with the board using HyperTerminal (or any other serial terminal)

SOFTWARE COMPILATION

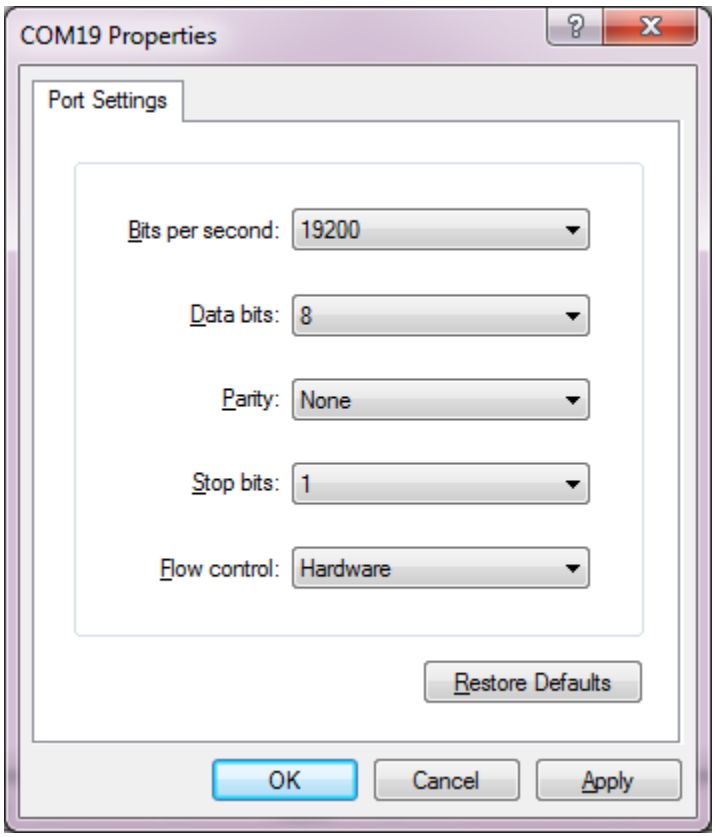
1. Open the software project lab/software/code.uvproj
2. Right click on Target and press “Build Target”



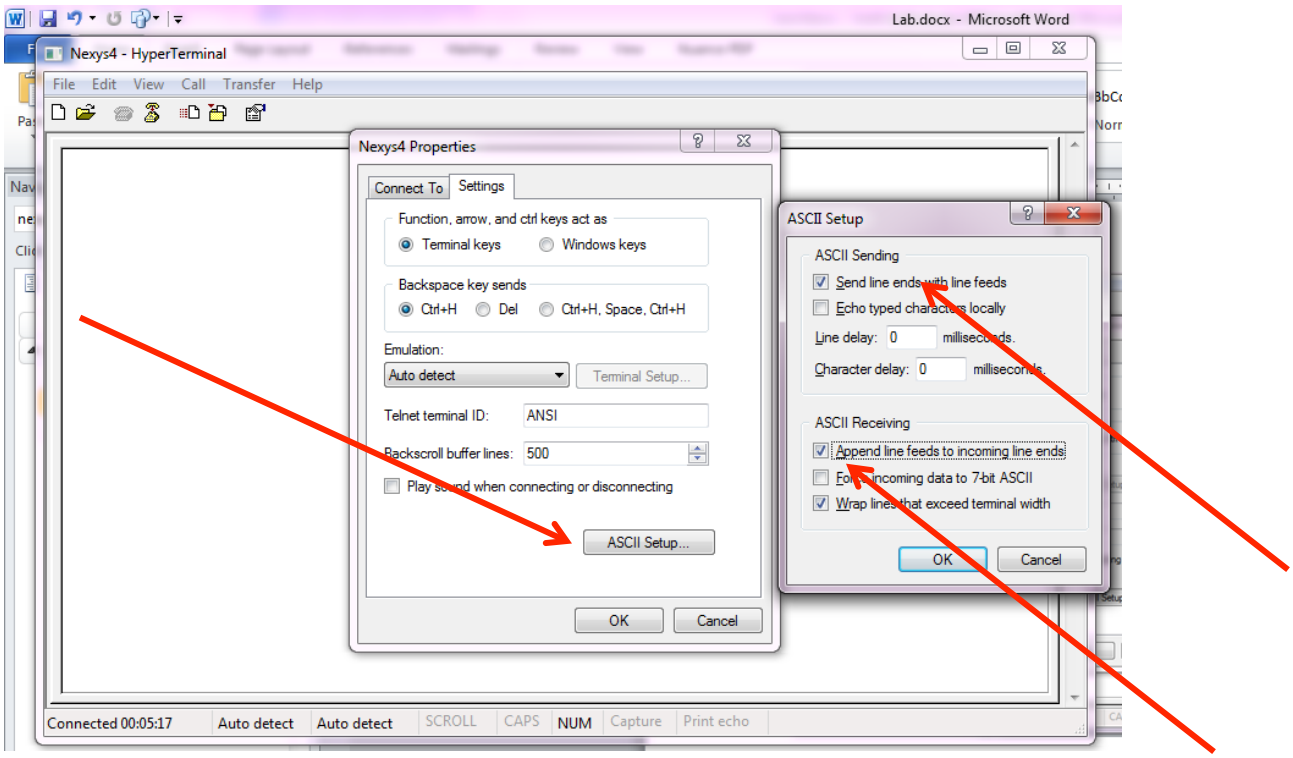
3. Check code.hex get generated inside software folder
4. The code binary is now ready to be downloaded onto the board

DOWNLOADING CODE.HEX ONTO ONBOARD PSRAM USING SERIAL COMMUNICATION

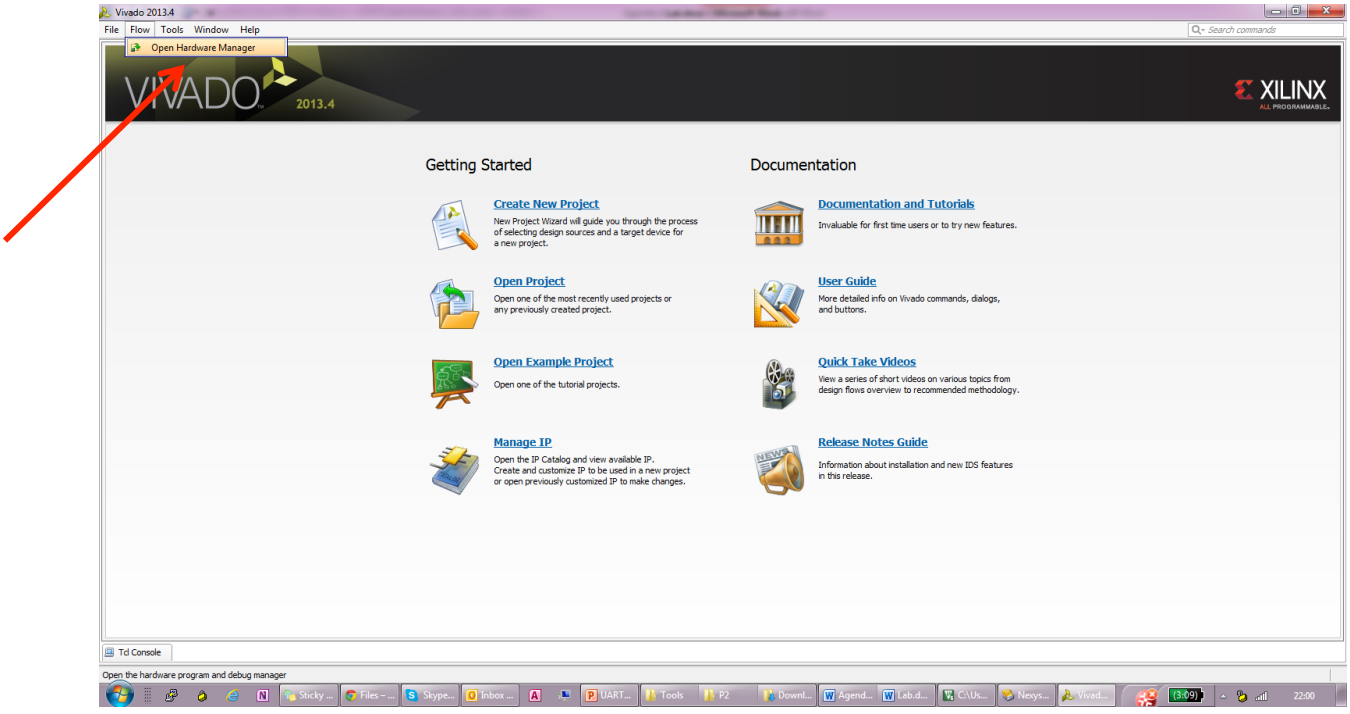
1. Go to the tools directory and open HyperTerminal.exe (or you can use any serial terminal)
2. Set the serial terminal with the following setting



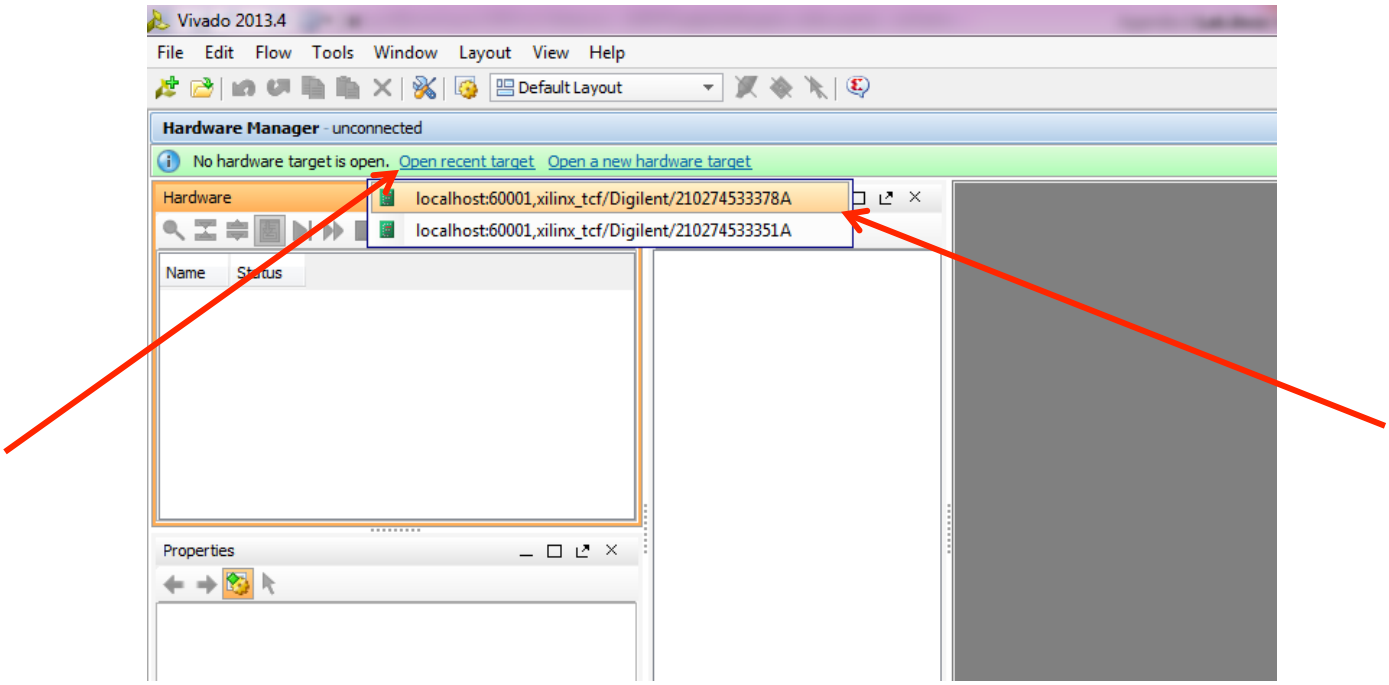
3. Now click FILE → Properties and change the ASCII setting,



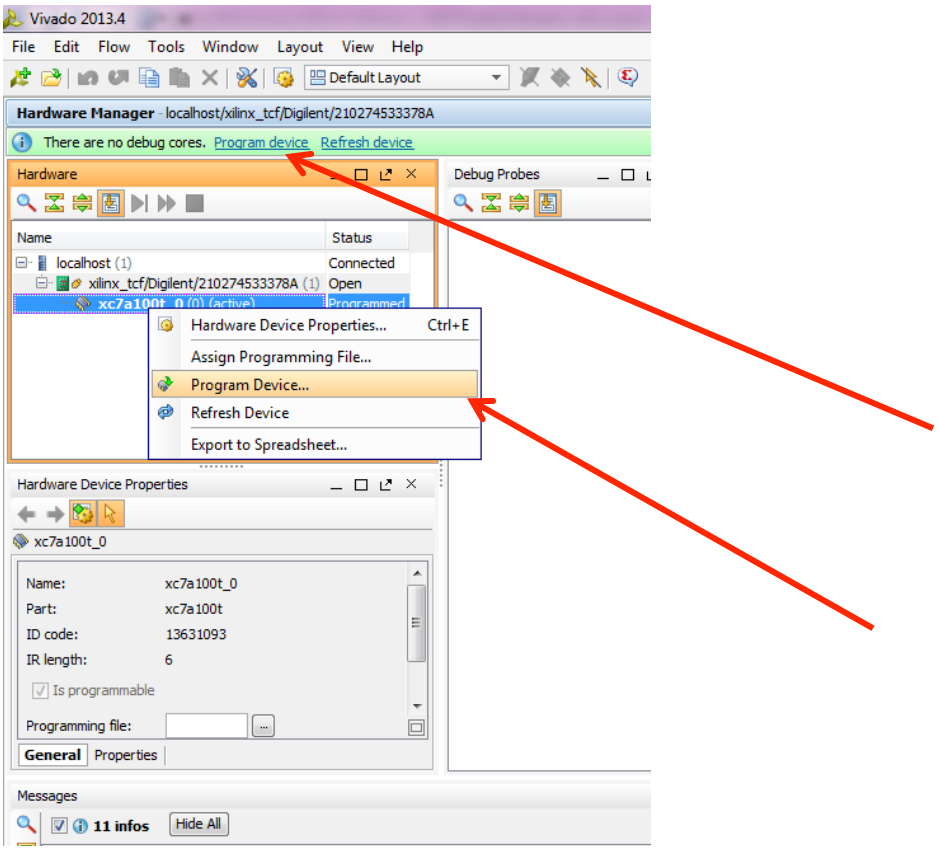
4. Now open a new Vivado window
5. Open Flow → Hardware Manager as show below



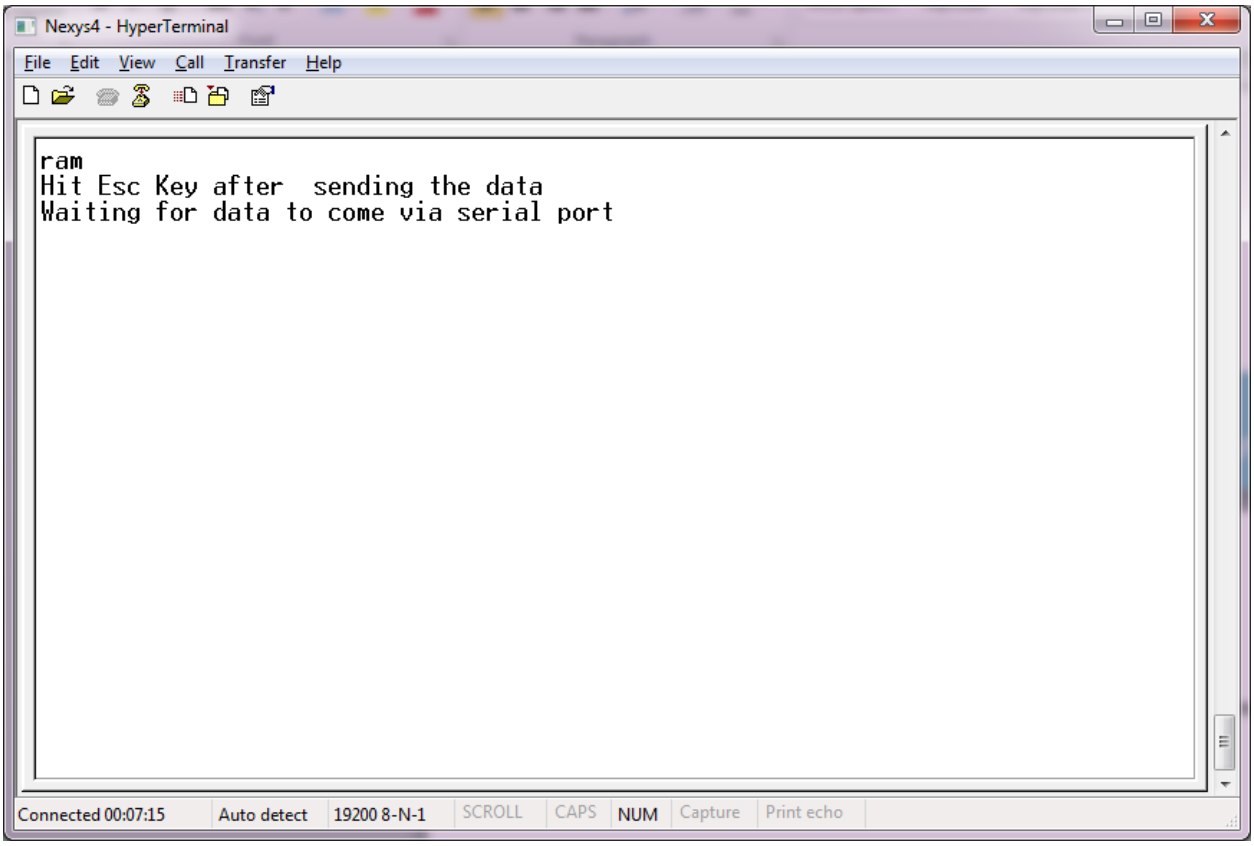
6. Click on “Open Recent Target” and choose the connection you established in the previous lab



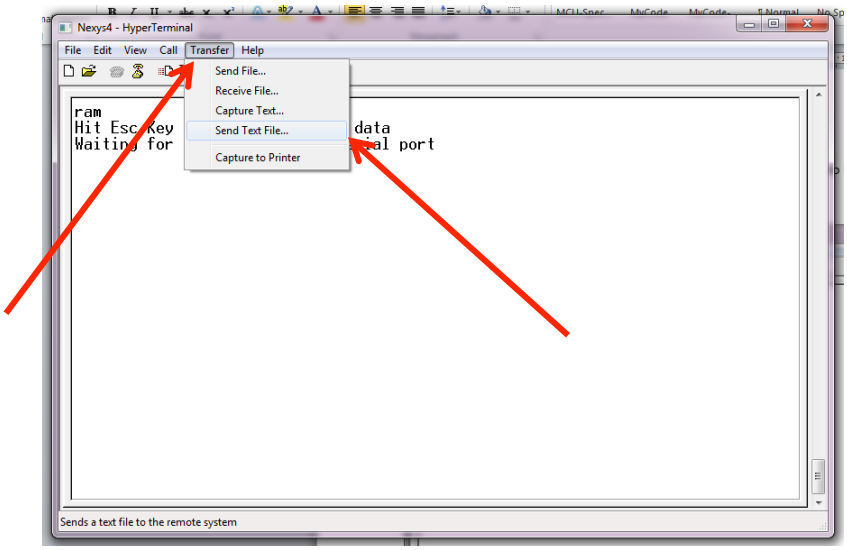
7. Right click on the device and choose “Program device”



8. Choose “download_19200.bit” present in the tools directory
9. This will load the download program which will transfer binary file into PSRAM
10. Open HyperTerminal and you should see below message,

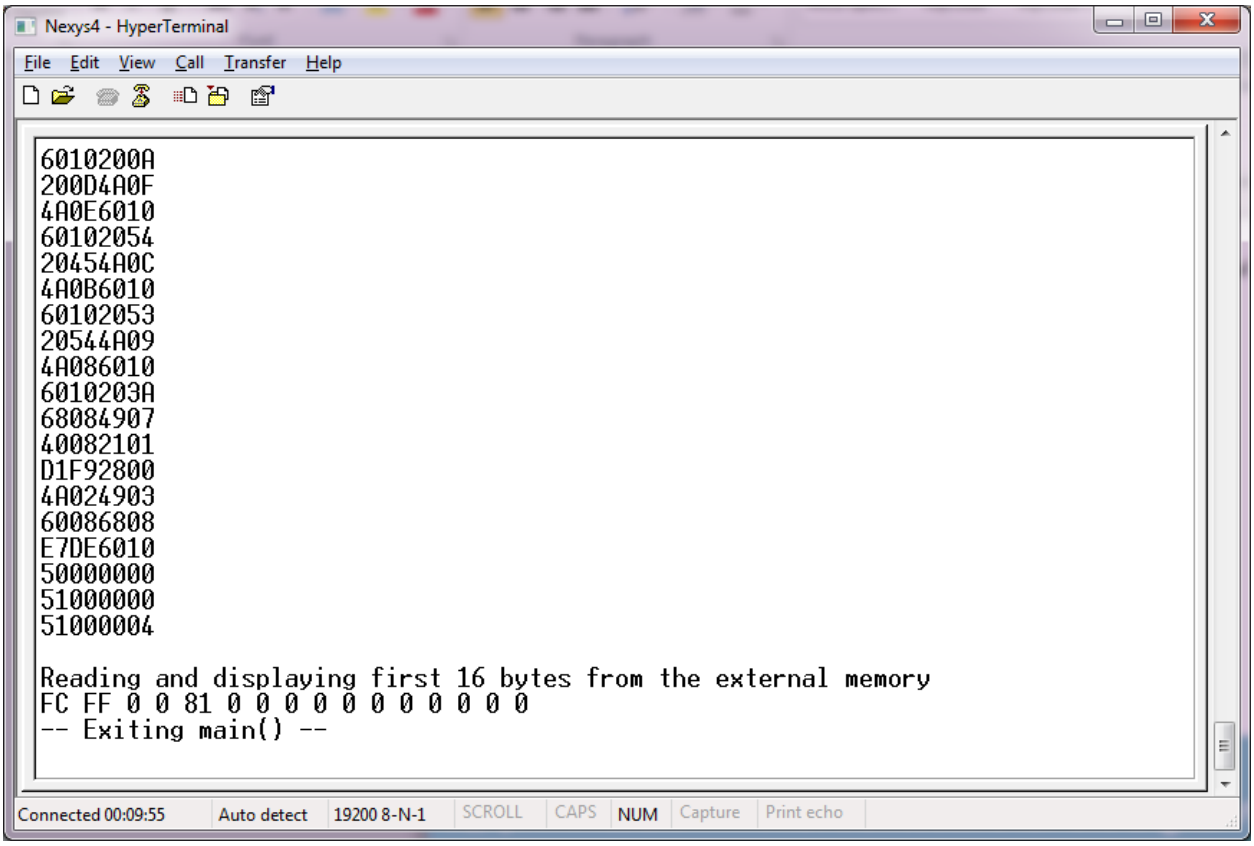


11. Send the code.hex file using “Send Text File” wizard in HyperTerminal



12. Choose code.hex file generated in lab/software directory

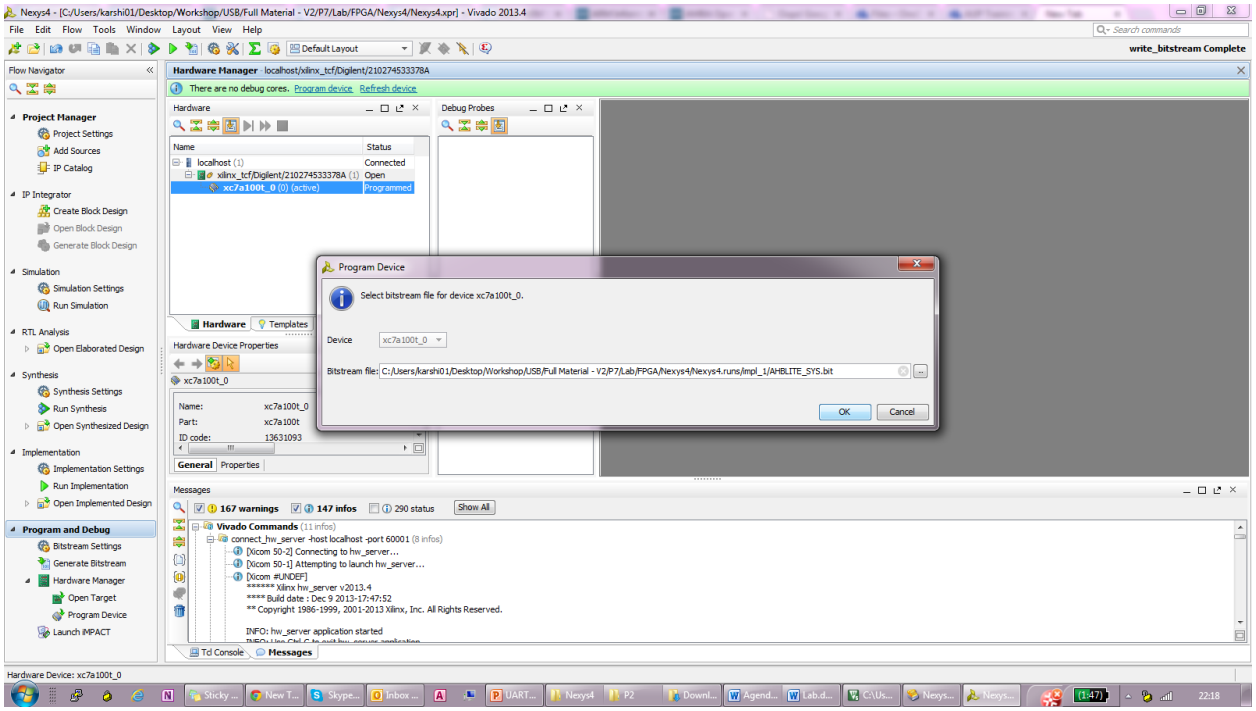
13. At the end of the transfer hit <ESC> key to complete the transfer. You should see the below message



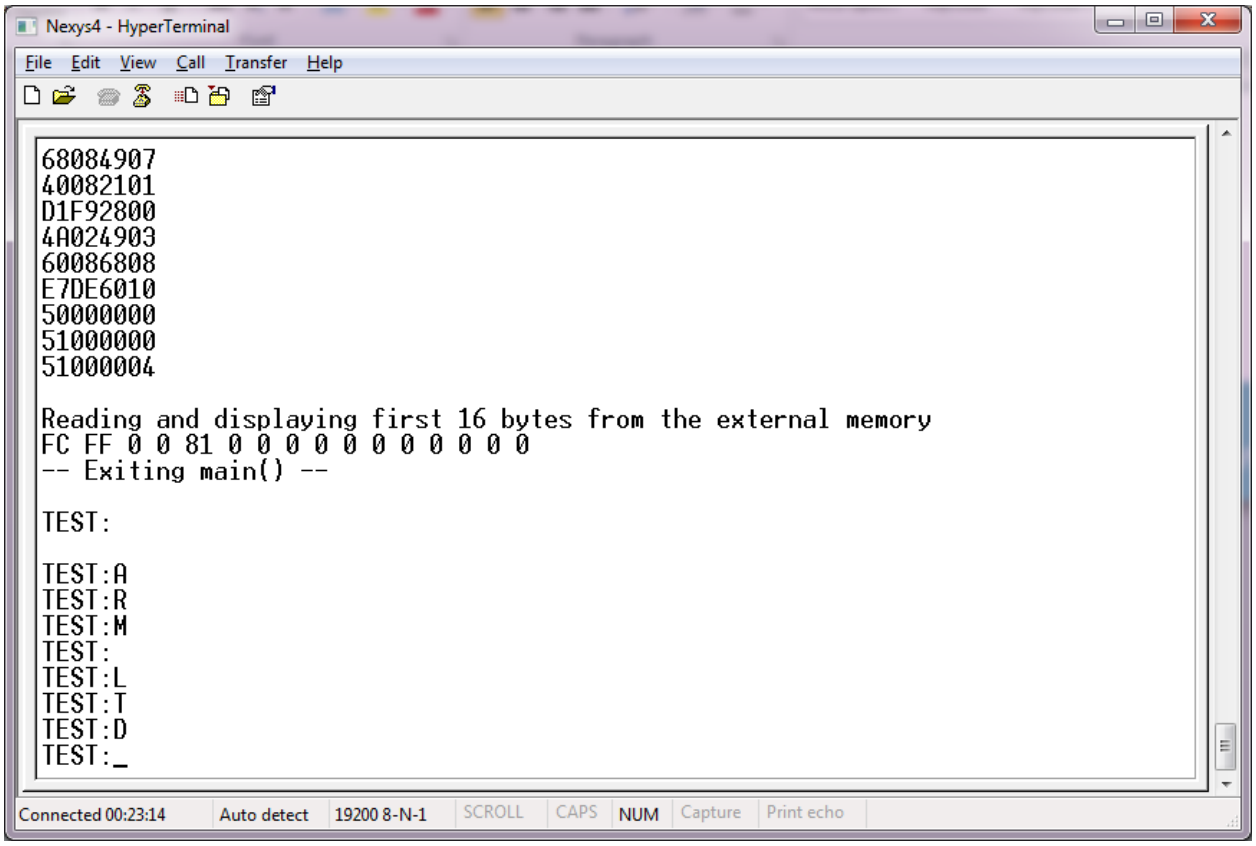
14. This complete the binary transfer and loads the PSRAM with code.hex binary data

SYNTHESIZE THE IMPLEMENT THE HARDWARE DESIGN

1. Open the Vivado project given in lab/FPGA/Nexys4/Nexys4.xpr
2. Analyze the top level of the design AHBLITE_SYS.v
3. Implement the design and generate bit stream
4. Once the bit stream is generated follow the steps from the previous lab to download the bit stream using hardware manager



5. Once the hardware is loaded onto FPGA, the CM0 in the design starts to execute the program loaded onto PSRAM
6. Check the HyperTerminal for the “TEST” message. If the message doesn’t appear, try sending a character by pressing “Enter”
7. If everything is working fine you should see something like below,



8. Note, when you send a character, the same character is reflected on the board LEDs. This will help in debugging if you have any issues with your HyperTerminal.