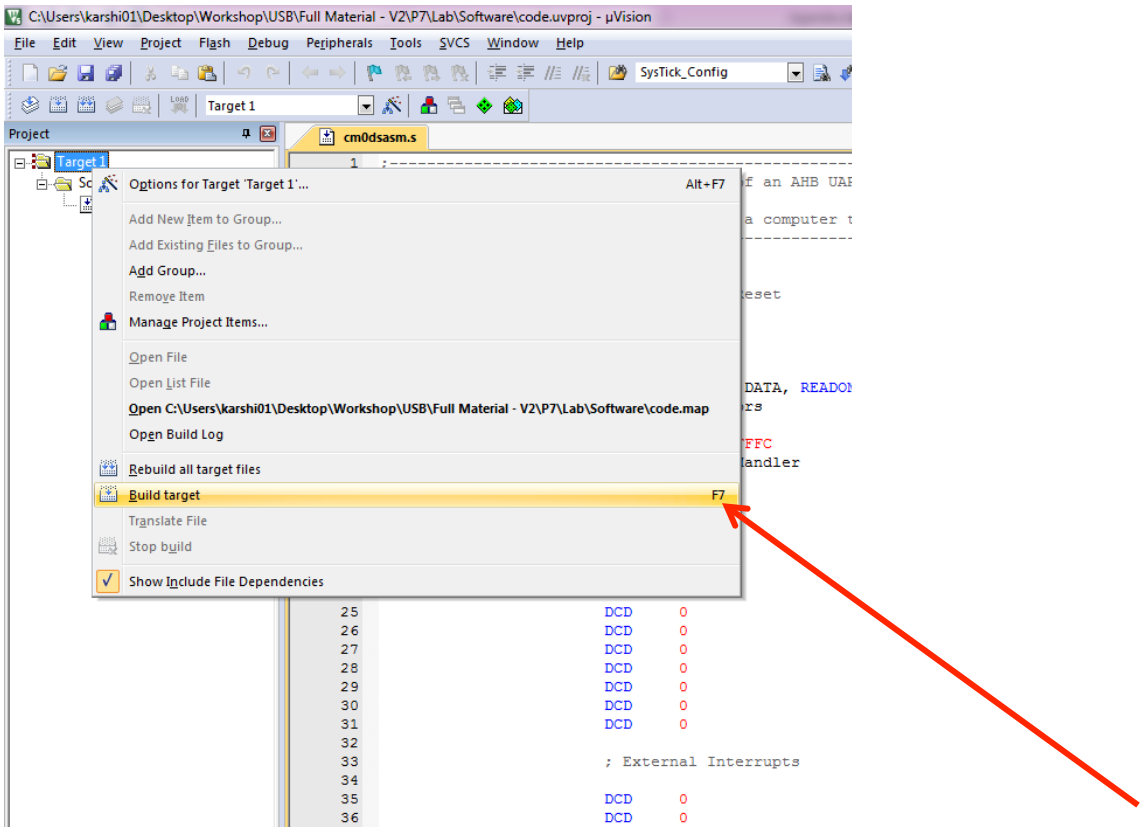
UART and BRAM Integration

SUMMARY

1. Compile the Software using KEIL MDK ARM and generate code.hex file
2. Open FPGA project under Vivado and implement the design
3. Use Vivado hardware manager to download the .bit file
4. Communicate with the board using HyperTerminal (or any other serial terminal)

SOFTWARE COMPILATION

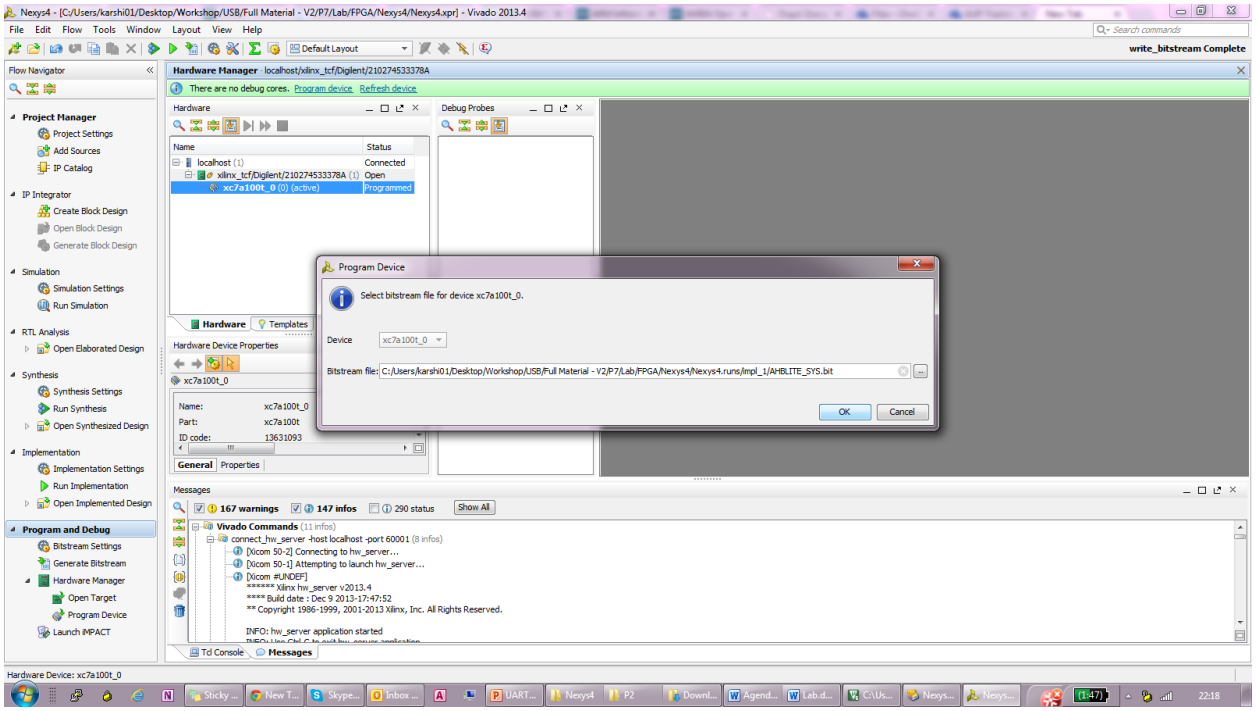
1. Open the software project lab/software/code.uvproj
2. Right click on Target and press “Build Target”



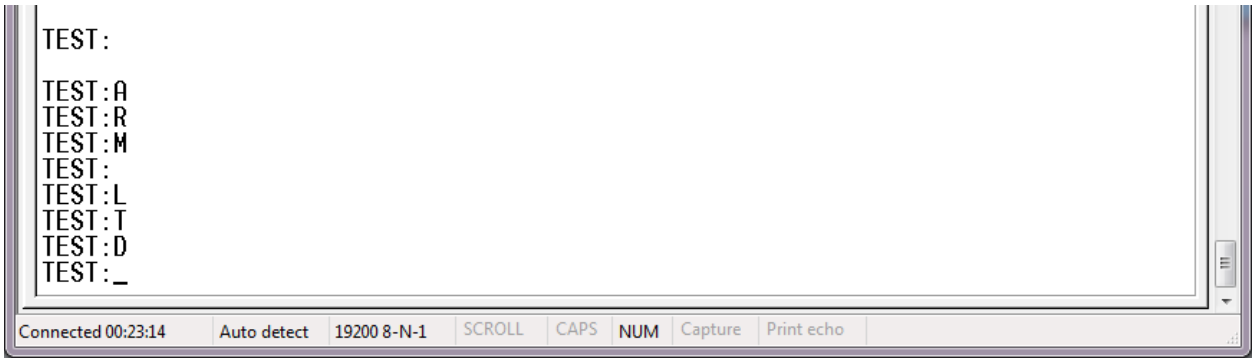
3. Check code.hex get generated inside software folder

SYNTHESIZE AND IMPLEMENT THE HARDWARE DESIGN

1. Open the Vivado project given in lab-BRAM/FPGA/Nexys4/Nexys4.xpr
2. Analyze the top level of the design AHBLITE_SYS.v
3. Implement the design and generate bit stream
4. Once the bit stream is generated follow the steps from the previous lab to download the bit stream using hardware manager



5. Once the hardware is loaded onto FPGA, the CM0 in the design starts to execute the program loaded in the internal memory
6. Check the HyperTerminal for the “TEST” message. If the message doesn’t appear, try sending a character by pressing “Enter”. (Refer to next step for setting hyperterminal)
7. If everything is working fine you should see something like below,



8. Note, when you send a character, the same character is reflected on the board LEDs. This will help in debugging if you have any issues with your HyperTerminal.

SETTING HYPERTERMINAL

1. Go to the tools directory and open HyperTerminal.exe (or you can use any serial terminal)
2. Set the serial terminal with the following setting