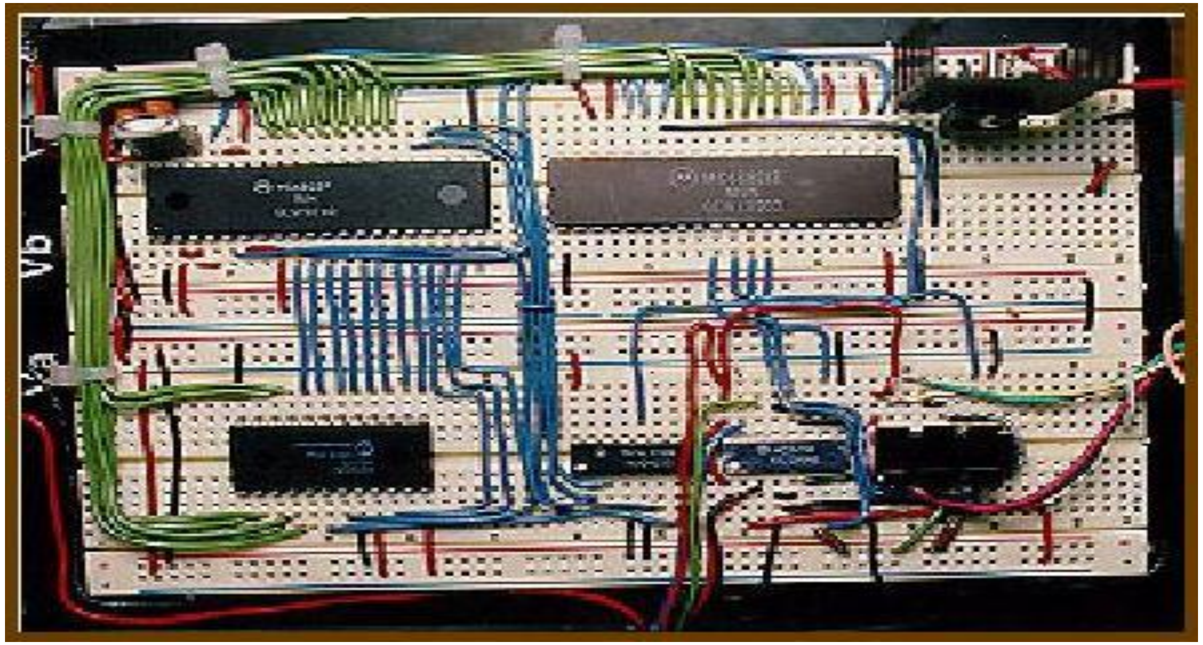
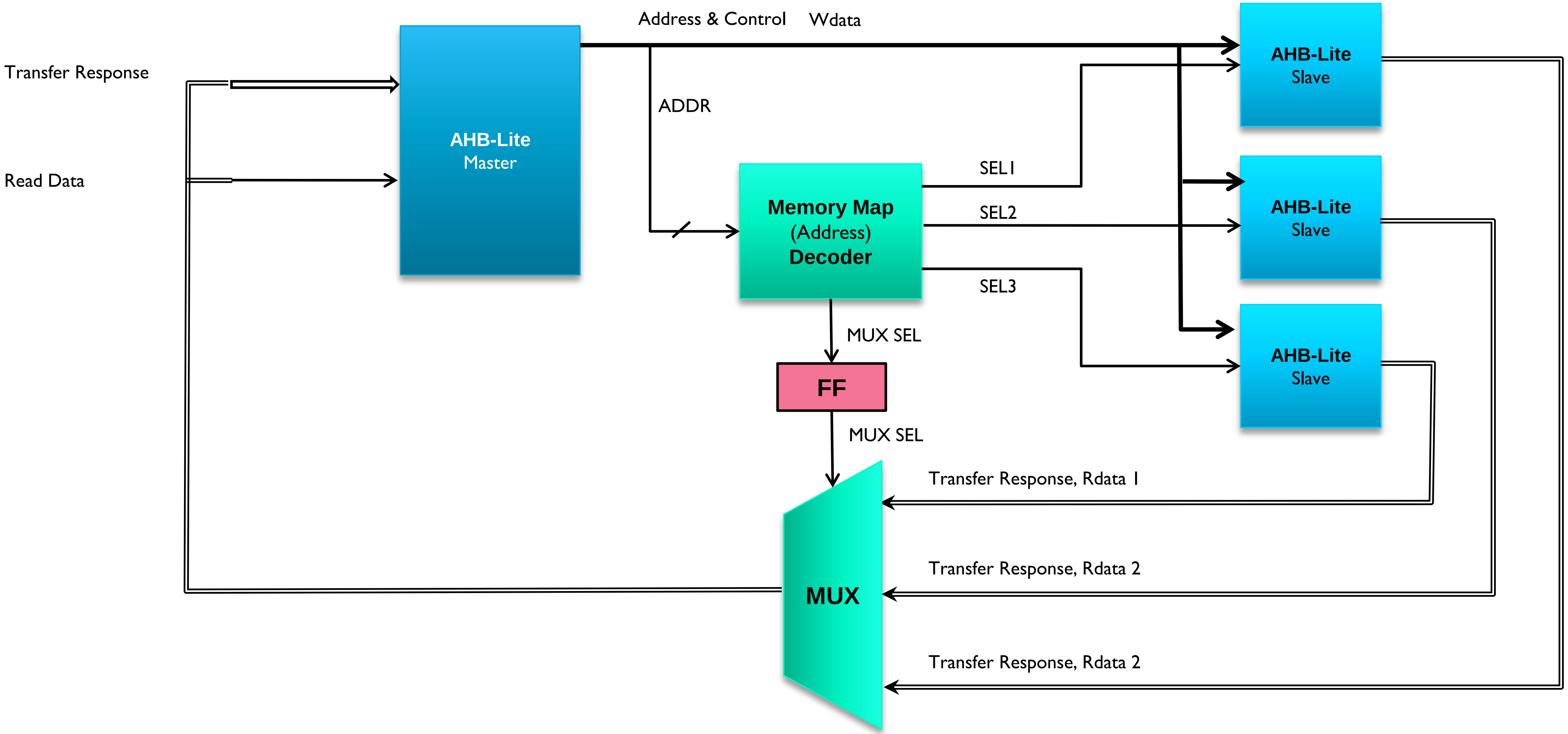
AHB-Lite System Integration



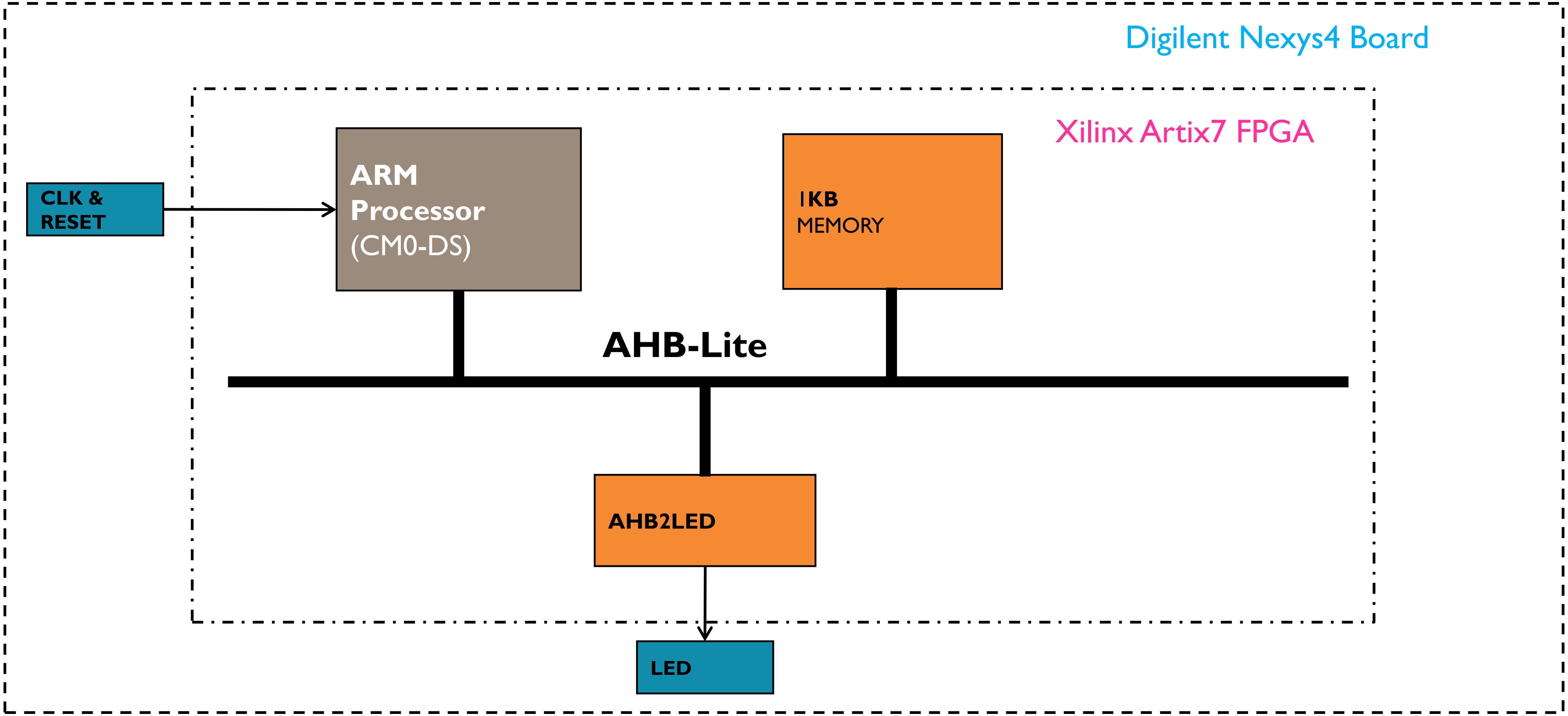
The Architecture for the Digital World®

ARM

AHB-Lite System (Recap)



Basic SoC

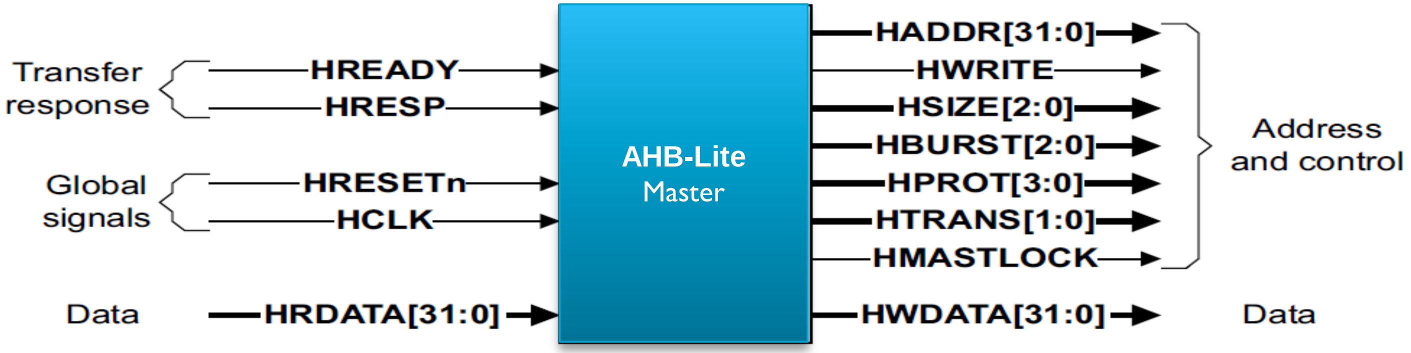

Digilent Nexys4 Board
Xilinx Artix7 FPGA
CLK &
RESET
ARM
Processor
(CM0-DS)
1KB
MEMORY
AHB-Lite
AHB2LED
LED

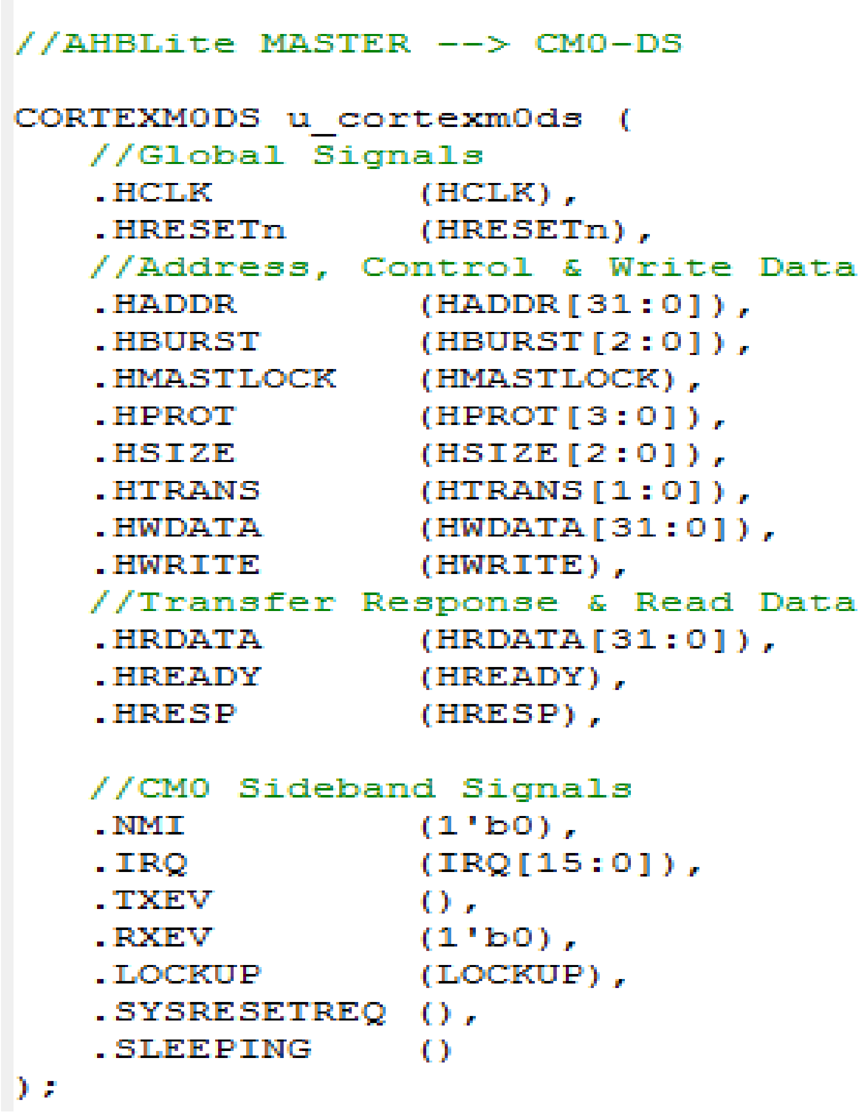
Memory Map

	START ADDRESS	END ADDRESS	SIZE
MEM	0x0000_0000	0x00FF_FFFF	1KB (256 Words)
LED	0x5000_0000	0x50FF_FFFF	16MB

AHB-Lite Master

- **CM0-DS in our case**

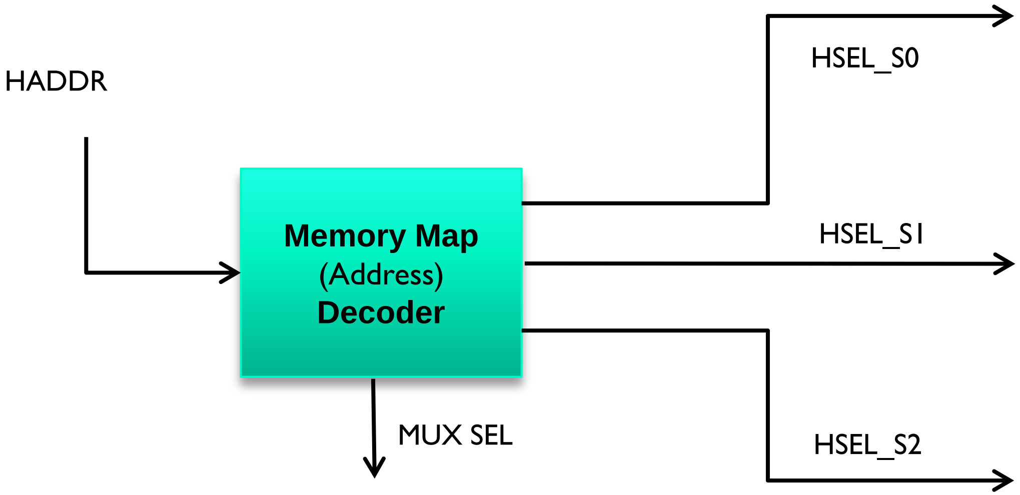


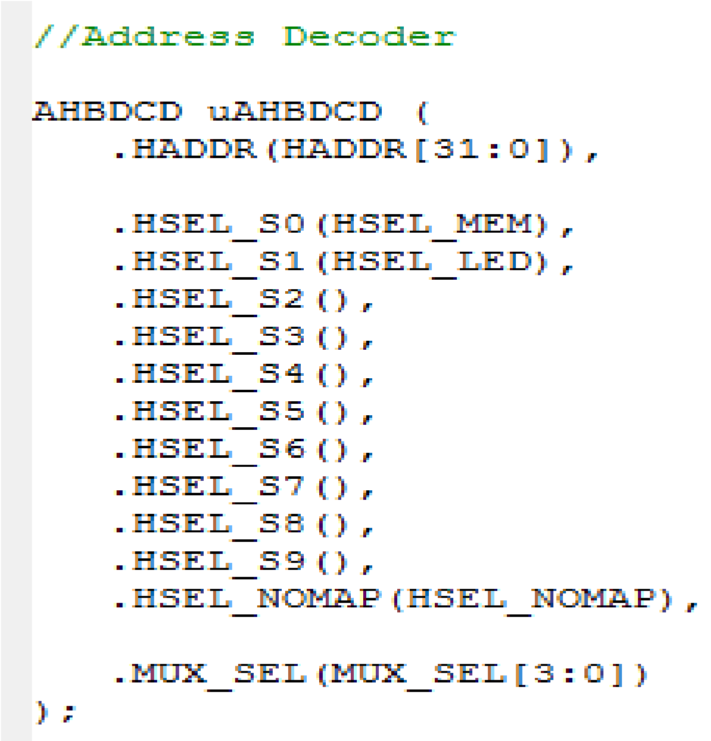


```
//AHBLite MASTER --> CM0-DS

CORTEXM0DS u_cortexm0ds (
   //Global Signals
   .HCLK         (HCLK),
   .HRESETn      (HRESETn),
   //Address, Control & Write Data
   .HADDR        (HADDR[31:0]),
   .HBURST       (HBURST[2:0]),
   .HMASTLOCK    (HMASTLOCK),
   .HPROT        (HPROT[3:0]),
   .HSIZE        (HSIZE[2:0]),
   .HTRANS       (HTRANS[1:0]),
   .HWDATA       (HWDATA[31:0]),
   .HWRITE       (HWRITE),
   //Transfer Response & Read Data
   .HRDATA       (HRDATA[31:0]),
   .HREADY       (HREADY),
   .HRESP        (HRESP),

   //CM0 Sideband Signals
   .NMI          (1'b0),
   .IRQ          (IRQ[15:0]),
   .TXEV         (),
   .RXEV         (1'b0),
   .LOCKUP       (LOCKUP),
   .SYSRESETREQ  (),
   .SLEEPING     ()
);
```

Address Decoder

- **Combination Block**
- **Decodes the address of each transfer and provides a select signal for slave**
- **Provides control signal to Multiplexer**

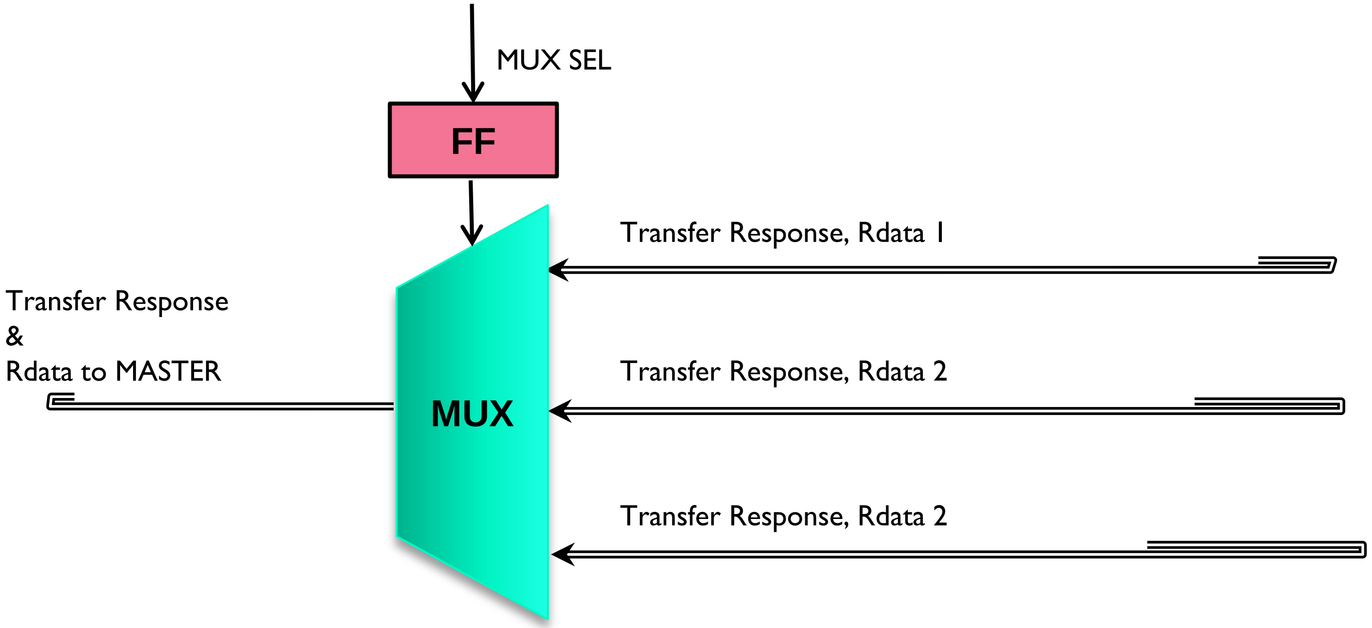


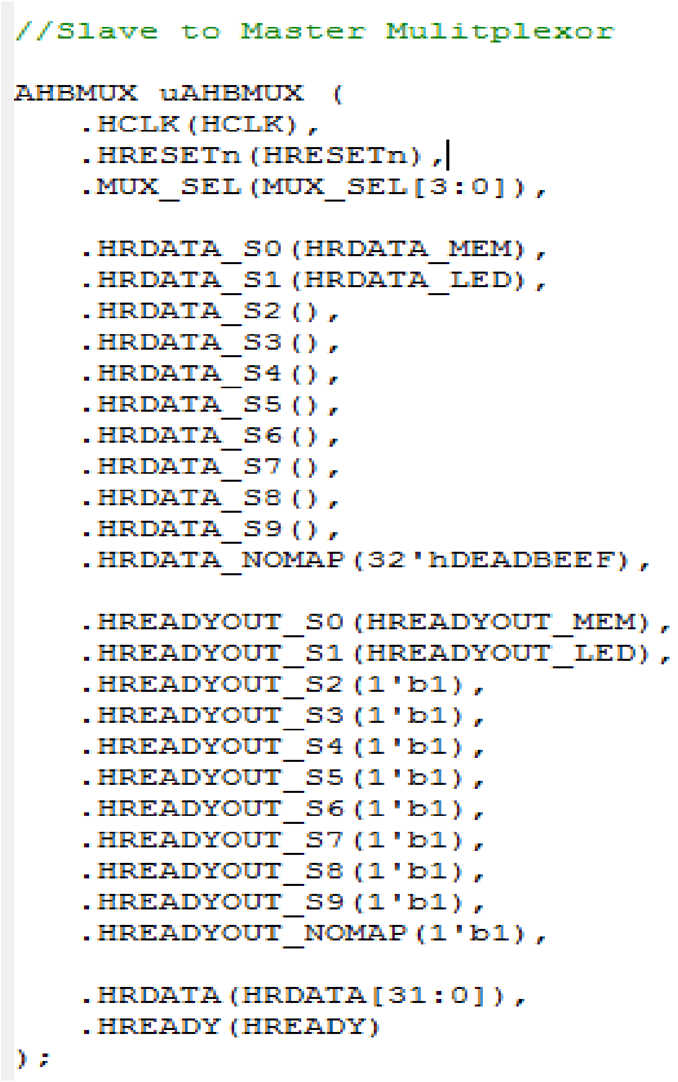


```
//Address Decoder

AHBDCD uAHBDCD (
     .HADDR(HADDR[31:0]),

     .HSEL_S0(HSEL_MEM),
     .HSEL_S1(HSEL_LED),
     .HSEL_S2(),
     .HSEL_S3(),
     .HSEL_S4(),
     .HSEL_S5(),
     .HSEL_S6(),
     .HSEL_S7(),
     .HSEL_S8(),
     .HSEL_S9(),
     .HSEL_NOMAP(HSEL_NOMAP),

     .MUX_SEL(MUX_SEL[3:0])
);
```

Slave-to-Master Multiplexer

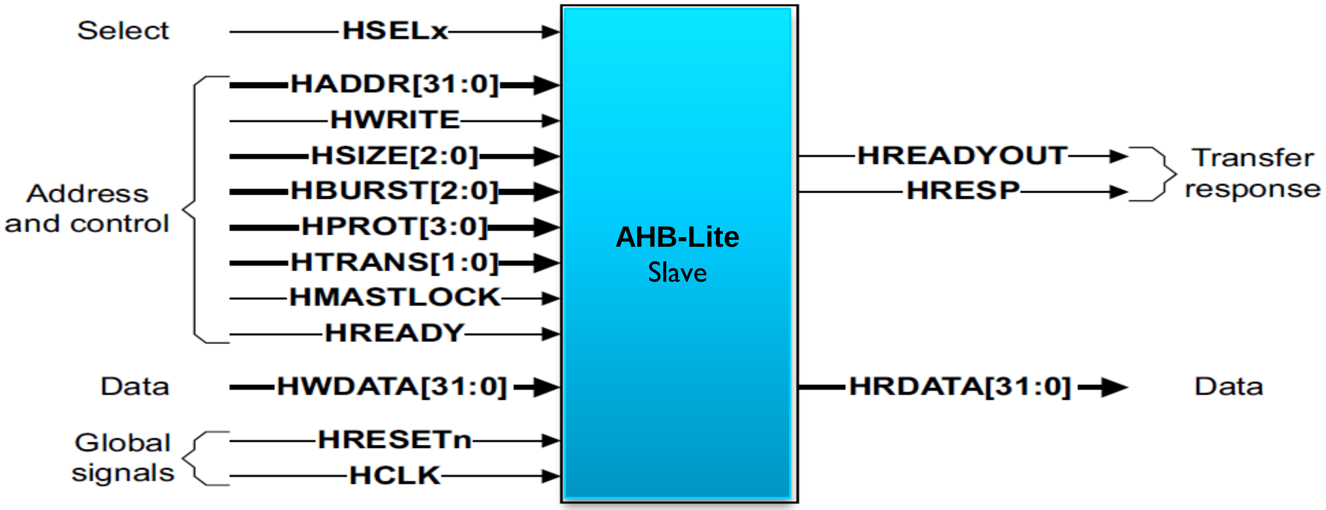
- **Multiplex the read data bus and response signals**
- **Decoder provides control (MUX_SEL)**
- **Remember Pipelined Operation**

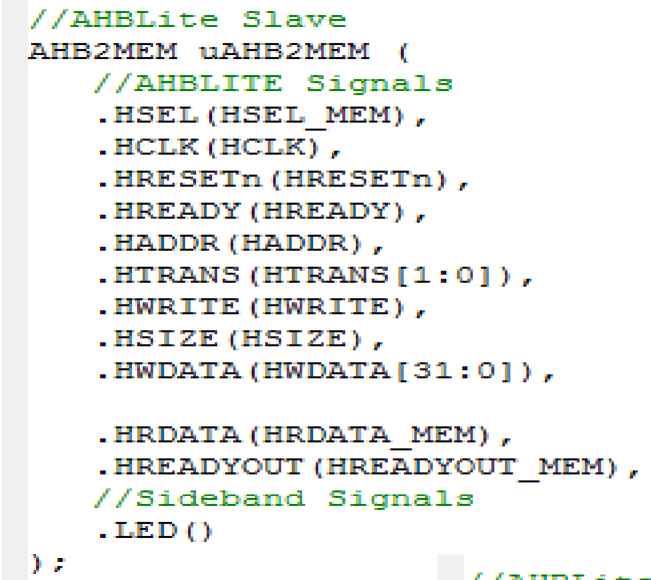

MUX SEL
FF
MUX
Transfer Response, Rdata 1
Transfer Response, Rdata 2
Transfer Response, Rdata 2
Transfer Response
&
Rdata to MASTER



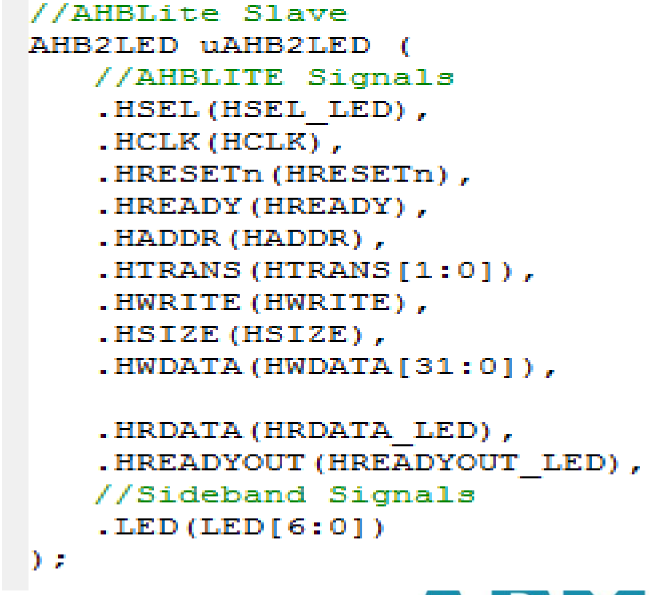
```
//Slave to Master Mulitplexor

AHBMUX uAHBMUX (
    .HCLK(HCLK),
    .HRESETn(HRESETn),
    .MUX_SEL(MUX_SEL[3:0]),

    .HRDATA_S0(HRDATA_MEM),
    .HRDATA_S1(HRDATA_LED),
    .HRDATA_S2(),
    .HRDATA_S3(),
    .HRDATA_S4(),
    .HRDATA_S5(),
    .HRDATA_S6(),
    .HRDATA_S7(),
    .HRDATA_S8(),
    .HRDATA_S9(),
    .HRDATA_NOMAP(32'hDEADBEEF),

    .HREADYOUT_S0(HREADYOUT_MEM),
    .HREADYOUT_S1(HREADYOUT_LED),
    .HREADYOUT_S2(1'b1),
    .HREADYOUT_S3(1'b1),
    .HREADYOUT_S4(1'b1),
    .HREADYOUT_S5(1'b1),
    .HREADYOUT_S6(1'b1),
    .HREADYOUT_S7(1'b1),
    .HREADYOUT_S8(1'b1),
    .HREADYOUT_S9(1'b1),
    .HREADYOUT_NOMAP(1'b1),

    .HRDATA(HRDATA[31:0]),
    .HREADY(HREADY)
);
```

AHB Slaves





```
//AHBLite Slave
AHB2MEM uAHB2MEM (
    //AHBLITE Signals
    .HSEL(HSEL_MEM),
    .HCLK(HCLK),
    .HRESETn(HRESETn),
    .HREADY(HREADY),
    .HADDR(HADDR),
    .HTRANS(HTRANS[1:0]),
    .HWRITE(HWRITE),
    .HSIZE(HSIZE),
    .HWDATA(HWDATA[31:0]),

    .HRDATA(HRDATA_MEM),
    .HREADYOUT(HREADYOUT_MEM),
    //Sideband Signals
    .LED()
);
```

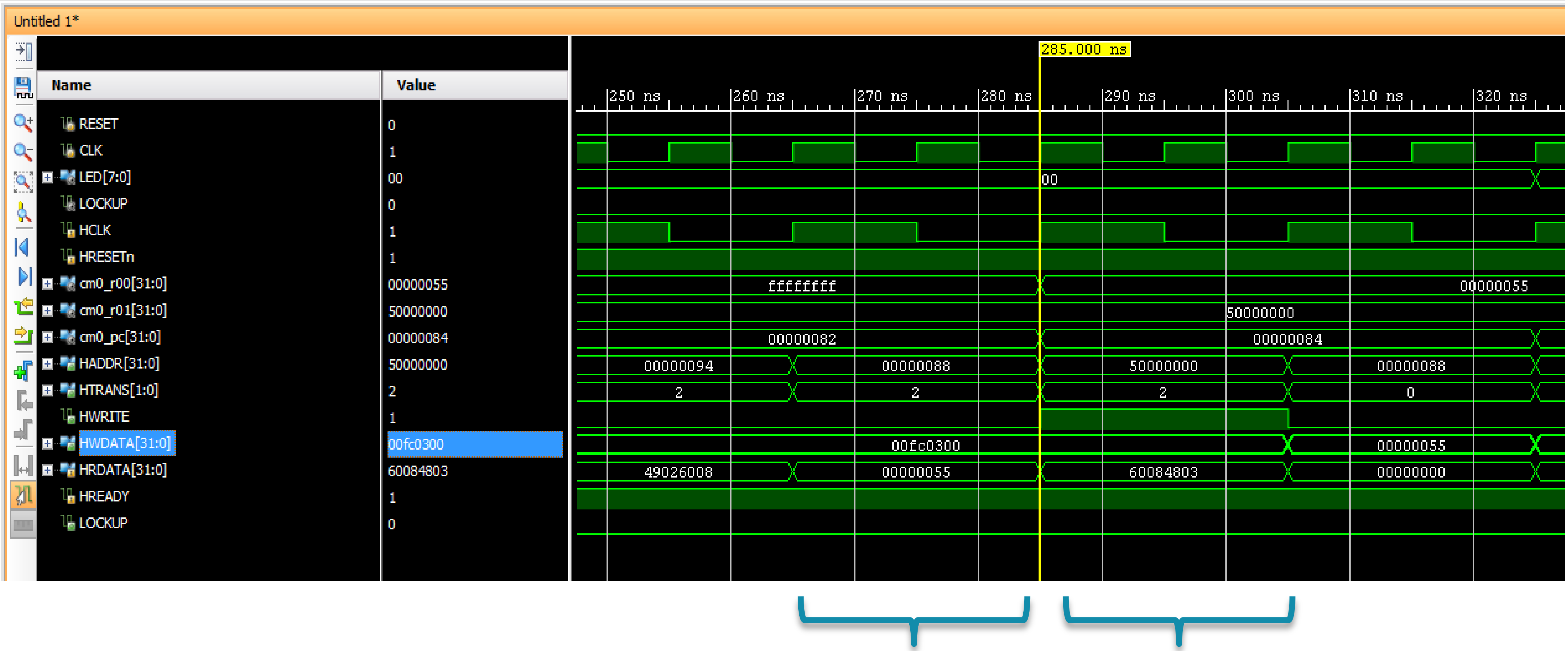


```
//AHBLite Slave
AHB2LED uAHB2LED (
    //AHBLITE Signals
    .HSEL(HSEL_LED),
    .HCLK(HCLK),
    .HRESETn(HRESETn),
    .HREADY(HREADY),
    .HADDR(HADDR),
    .HTRANS(HTRANS[1:0]),
    .HWRITE(HWRITE),
    .HSIZE(HSIZE),
    .HWDATA(HWDATA[31:0]),

    .HRDATA(HRDATA_LED),
    .HREADYOUT(HREADYOUT_LED),
    //Sideband Signals
    .LED(LED[6:0])
);
```

LAB Part 1: Simulate the design and view AHB-Lite Transactions

1. Open “CODE” KEIL project in Lab Part1/Software folder and compile the design
2. Check code.hex gets generated
3. Copy your downloaded CM0-DS design files (CORTEXM0DS.v and cortexm0ds_logic.v) to the “Lab Part1/FPGA/Source folder”
4. Follow Step 1 and Step 2 in the lab manual to simulate the design using Vivado design flow
5. Once the design starts simulation add these signals into the waveform from u_cortexm0ds design instance
    1. AHB-Lite Signals
    2. Core register signals

View AHB-Lite Transactions



Untitled 1*

Name	Value
RESET	0
CLK	1
LED[7:0]	00
LOCKUP	0
HCLK	1
HRESETn	1
cm0_r00[31:0]	00000055
cm0_r01[31:0]	50000000
cm0_pc[31:0]	00000084
HADDR[31:0]	50000000
HTRANS[1:0]	2
HWRITE	1
HWDATA[31:0]	00fc0300
HRDATA[31:0]	60084803
HREADY	1
LOCKUP	0

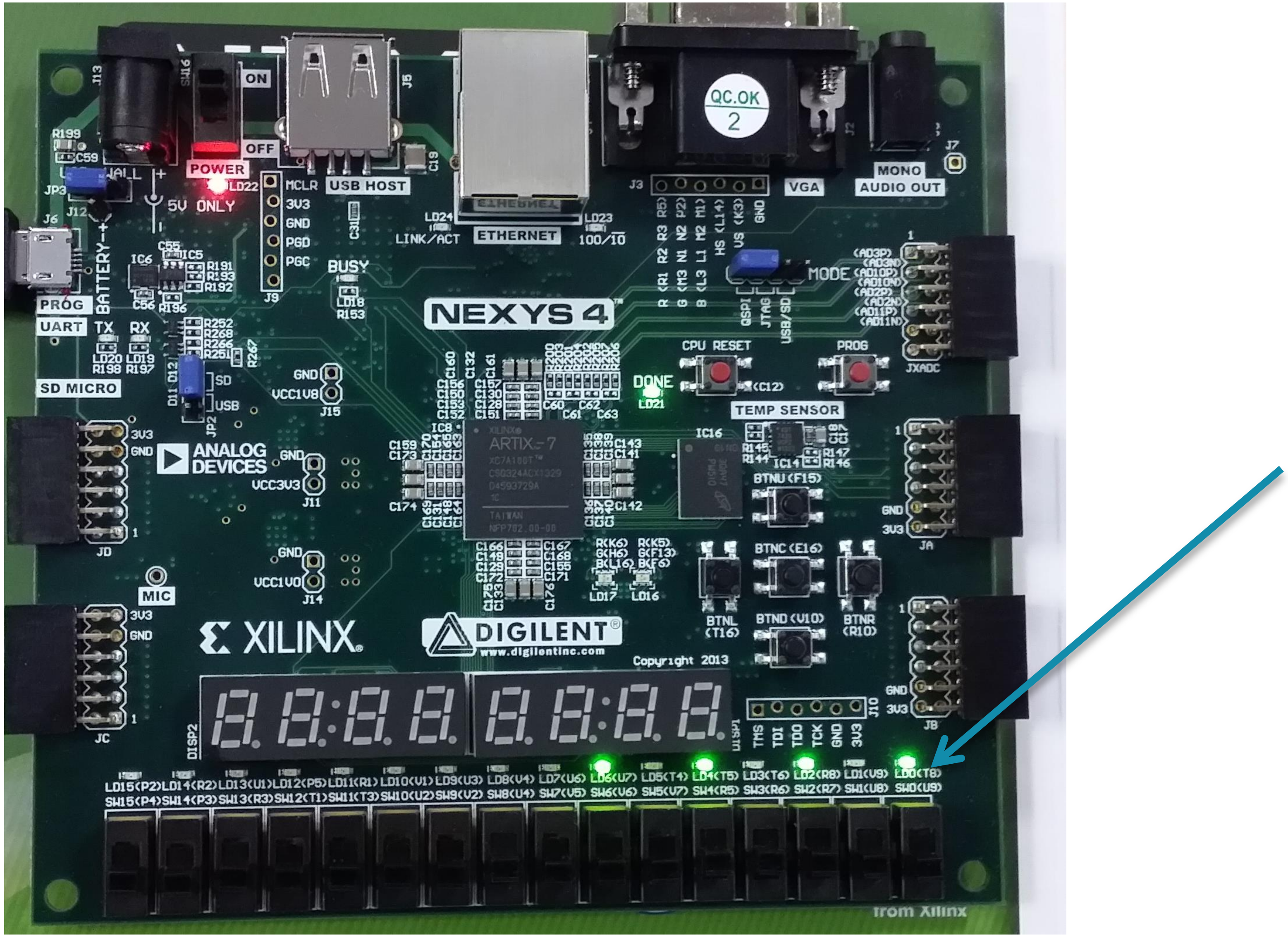
Read Transaction

Write Transaction

LAB Part 2: Make those LEDs blink on the board!

1. Open "CODE" KEIL project in Lab Part2/Software folder and compile the design
2. Check code.hex gets generated
3. Copy your downloaded CM0-DS design files (CORTEXM0DS.v and cortexm0ds_logic.v) to the "Lab Part2/FPGA/Source folder"
4. Open Vivado Project "Nexys4" inside "Lab Part2/FPGA/Nexys4 folder"
5. Follow Step 3, Step 4 and Step 5 in the lab manual to synthesize, implement and download the design on the board

Result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LD15(P2) LD14(R2) LD13(U1) LD12(P5) LD11(R1) LD10(V1) LD9(U3) LD8(V4) LD7(U6) LD6(U7) LD5(T4) LD4(T5) LD3(T6) LD2(R8) LD1(V9) LD0(T8)
SW15(P4) SW14(P3) SW13(R3) SW12(T1) SW11(T3) SW10(U2) SW9(V2) SW8(U4) SW7(V5) SW6(V6) SW5(V7) SW4(R5) SW3(R6) SW2(R7) SW1(U8) SW0(U9)