7-Series Architecture Overview

Artix-7
Vivado 2013.4 Version

Objectives

- **After completing this module, you will be able to:**
  - Describe the basic slice resources available in 7-Series FPGAs
  - List memory hierarchy and various memory resources available
  - Identify the basic I/O resources available in 7-Series FPGAs
  - List some of the dedicated hardware features of 7-Series FPGAs
  - Explain the available clocking resources and mechanism
  - Identify the MMCM, PLL, and clock routing resources included with these families

Outline

- *Introduction to 7-Series FPGA*
- Logic Resources
- I/O Resources
- Memory and DSP48 Resources
- XADC
- Clocking Resources
- Zynq SoC
- Summary

Introduction

- **All Xilinx FPGAs contain the same basic resources**
  - Logic Resources
    - Slices (grouped into configurable logic blocks (CLB))
      - Contain combinatorial logic and register resources
    - Memory
    - Multipliers
  - Interconnect Resources
    - Programmable interconnect
    - IOBs
      - Interface between the FPGA and the outside world
  - Other resources
    - Global clock buffers
    - Boundary scan logic
- **Through various generations, Xilinx added new architectural resources to target various markets and application areas**

7-Series FPGA+SoC Families

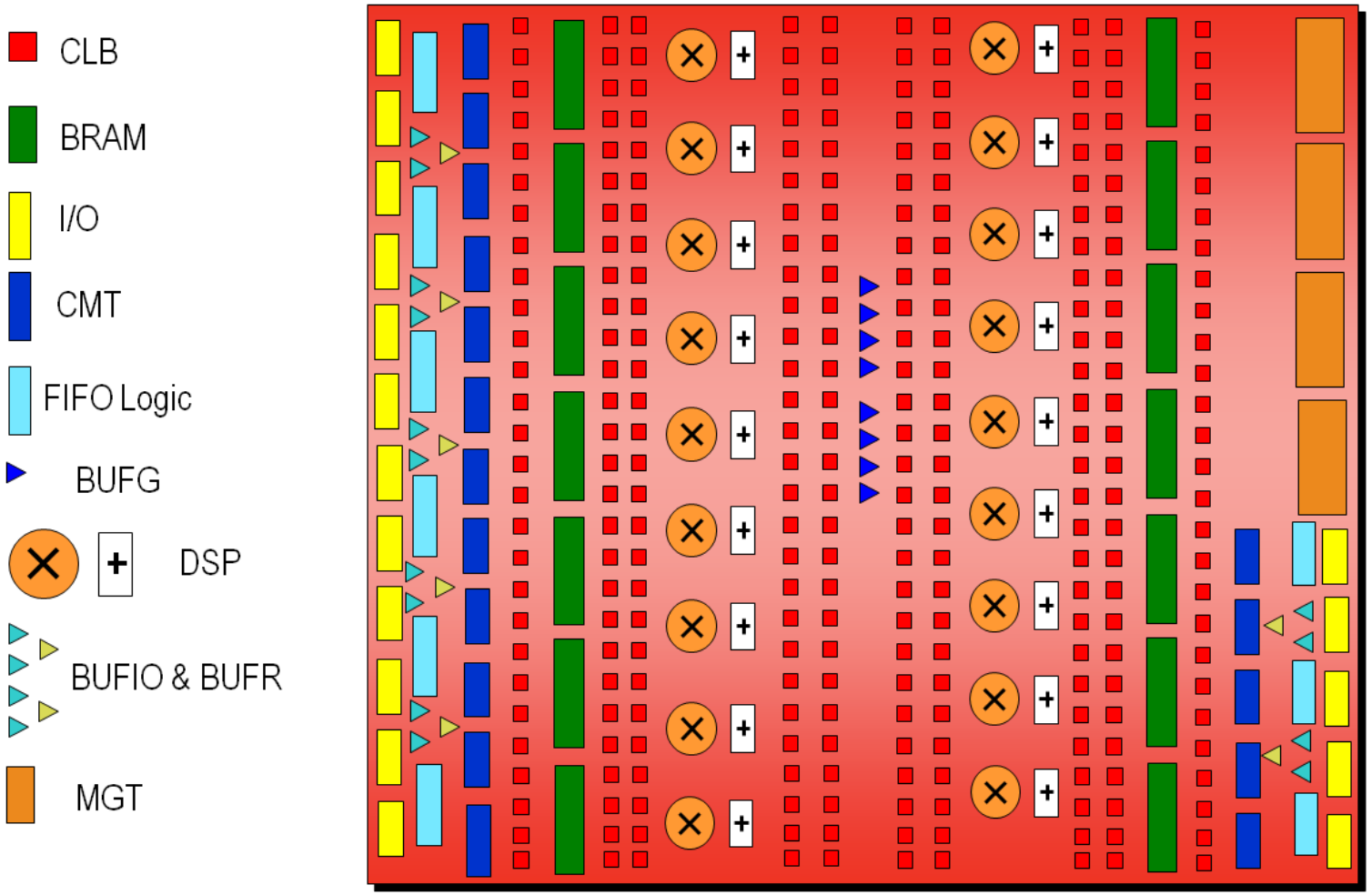
Maximum Capability	ARTIX-7 Lowest Power and Cost	KINTEX-7 Industry's Best Price/Performance	VIRTEX-7 Industry's Highest Performance	ZYNQ All Programmable SOC
Logic Cells	33K – 215K	70K – 478K	326K – 1,955K	28K – 444K
Block RAM	12 Mb	34 Mb	65 Mb	27 Mb
DSP Slices	40 – 700	240 – 1,920	700 – 3,960	80–2,020
Peak DSP Perf.	504 GMACS	2,450 GMACs	5,053 GMACS	2,662 GMACS
Transceivers	Up to 16	Up to 32	Up to 88	Up to 16
Transceiver Performance	6.6Gbps	12.5Gbps	12.5Gbps, 13.1Gbps and 28Gbps	6.6Gbps, 12.5Gbps and
Memory Performance	1066Mbps	1866Mbps	1866Mbps	1333Mbps
I/O Pins	500	500	1,200	400
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

Artix-7 Family

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTPs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18Kb	36Kb	Max (Kb)						
XC7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A75T	75,520	11,800	892	180	210	105	3,780	6	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Package[1]	CPG236		CSG324		CSG325		FTG256		SBG484		FGG484[2]		FBG484[2]		FGG676[3]		FBG676[3]		FFG1156	
Size (mm)	10 x 10		15 x 15		15 x 15		17 x 17		19 x 19		23 x 23		23 x 23		27 x 27		27 x 27		35 x 35	
Ball Pitch (mm)	0.5		0.8		0.8		1.0		0.8		1.0		1.0		1.0		1.0		1.0	
Device	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]
XC7A35T	2	106	0	210	4	150	0	170			4	250								
XC7A50T	2	106	0	210	4	150	0	170			4	250								
XC7A75T			0	210			0	170			4	285			8	300				
XC7A100T			0	210			0	170			4	285			8	300				
XC7A200T									4	285			4	285			8	400	16	500

Artix-7 FPGA Architecture Overview



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- *Logic Resources*
- I/O Resources
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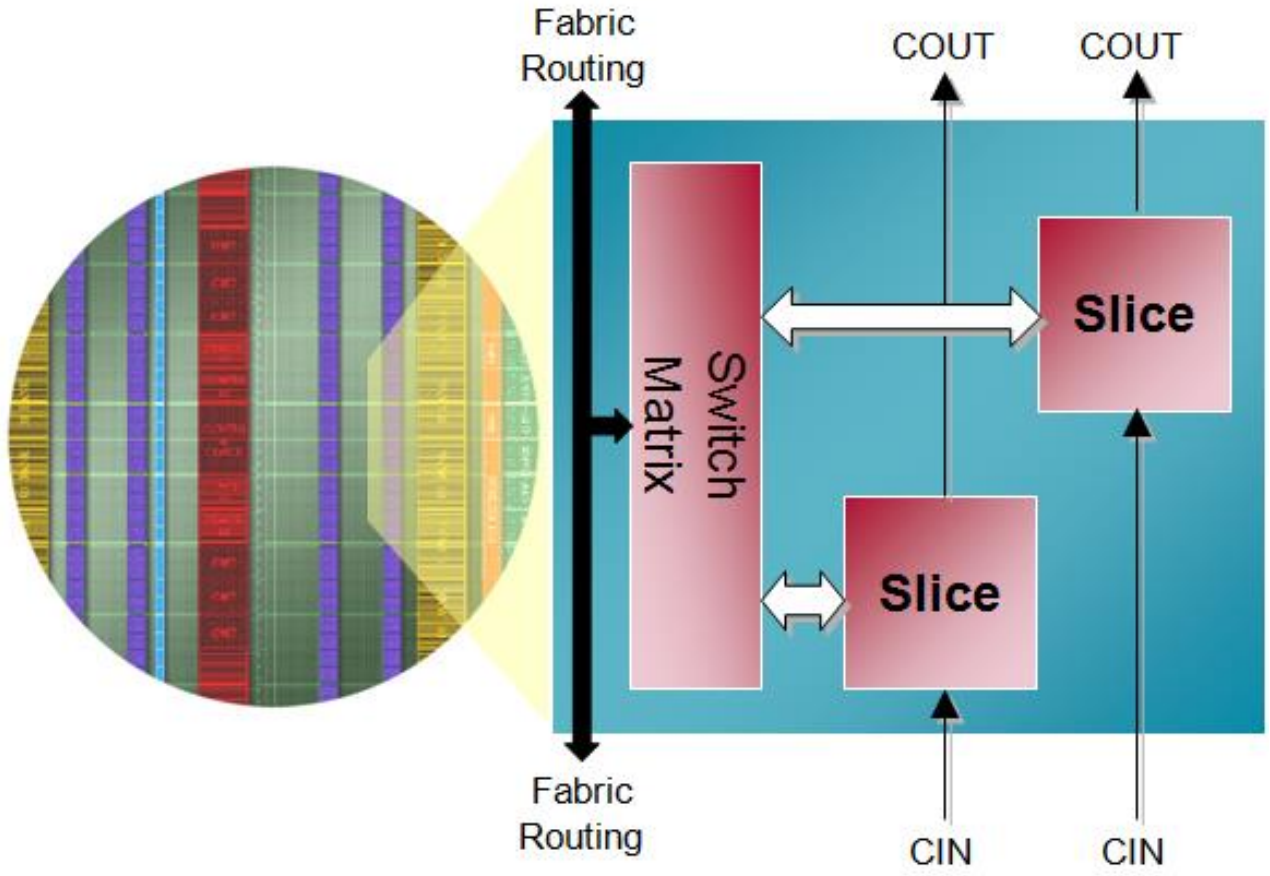
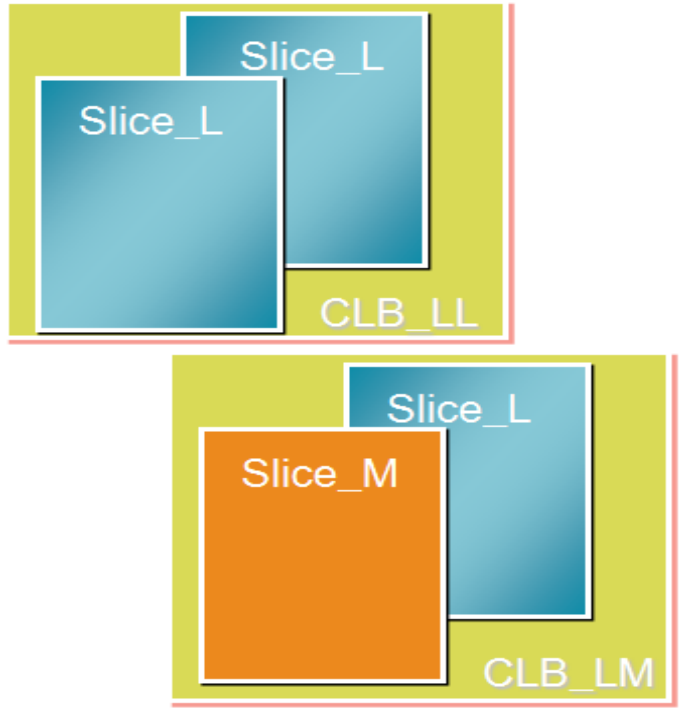
Configurable Logic Block (CLB) in 7-Series FPGAs

- **Primary resource for design**
  - Combinatorial functions
  - Flip-flops
- **CLB contains two slices**
- **Connected to switch matrix for routing to other FPGA resources**
  - Carry chain runs vertically in a column from one slice to the one above



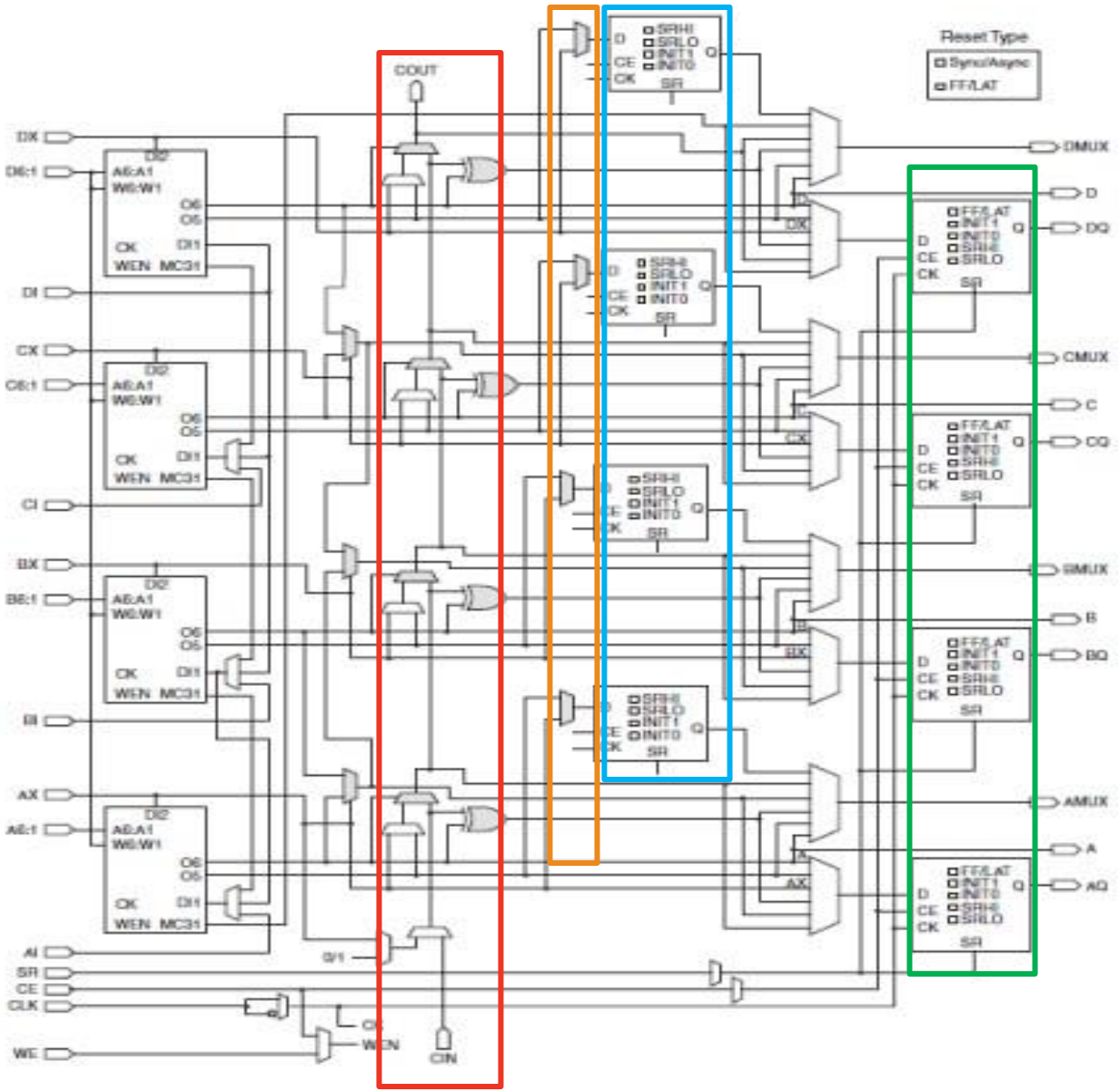
Two Types of Slices

- **Two types of slices**
  - SLICEM: Full slice
    - LUT can be used for logic and memory/SRL
    - Has wide multiplexers and carry chain
  - SLICEL: Logic and arithmetic only
    - LUT can only be used for logic (not memory)
    - Has wide multiplexers and carry chain



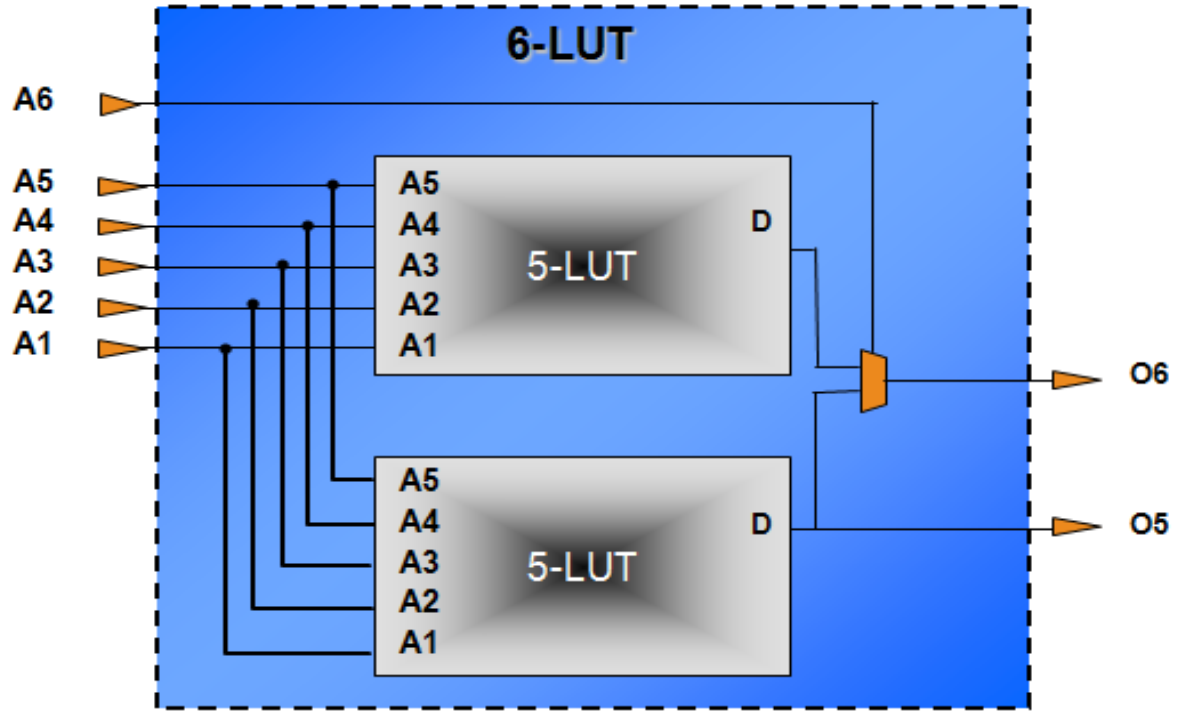
Slice Resource

- **Four six-input Look-Up Tables (LUT)**
- **Multiplexers**
- **Carry chains**
- **SRL**
  - Cascade path is not shown
- **Four flip-flops/latches**
  - Four additional flip-flops
- **The implementation tool will pack multiple slices in the same CLB if certain rules are followed**



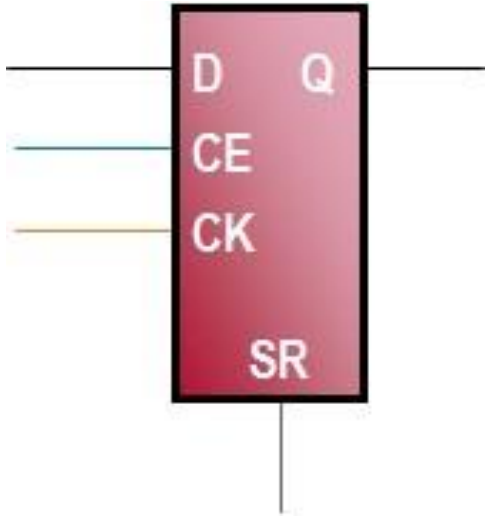
6-Input LUT with Dual Output

- **LUTs can be two 5-input LUTs with common input**
  - Minimal speed impact to a 6-input LUT
  - One or two outputs
- **Any function of six variables or two functions of five variables**



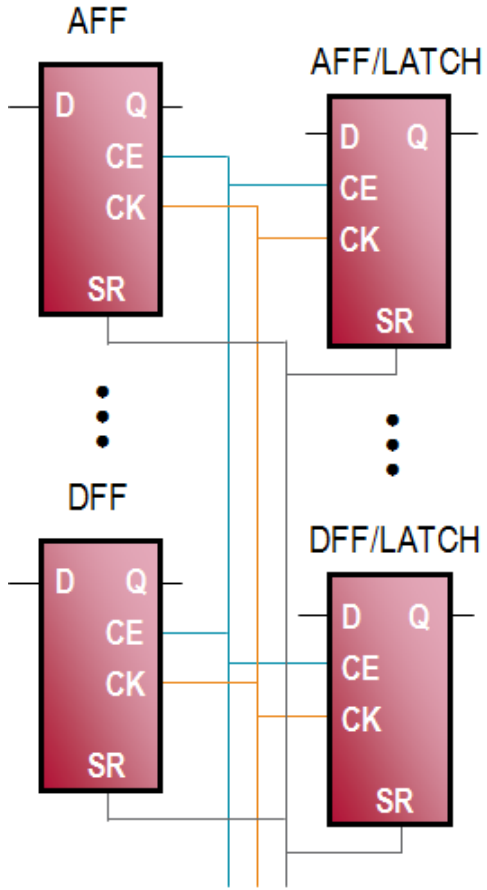
Slice Flip-Flop Capabilities

- **All flip-flops are D type**
- **All flip-flops have a single clock input (CK)**
  - Clock can be inverted at the slice boundary
- **All flip-flops have an active high chip enable (CE)**
- **All flip-flops have an active high SR input**
  - Input can be synchronous or asynchronous as determined by the corresponding configuration bit
  - Sets the flip-flop value to a pre-determined state as determined by the corresponding configuration bit



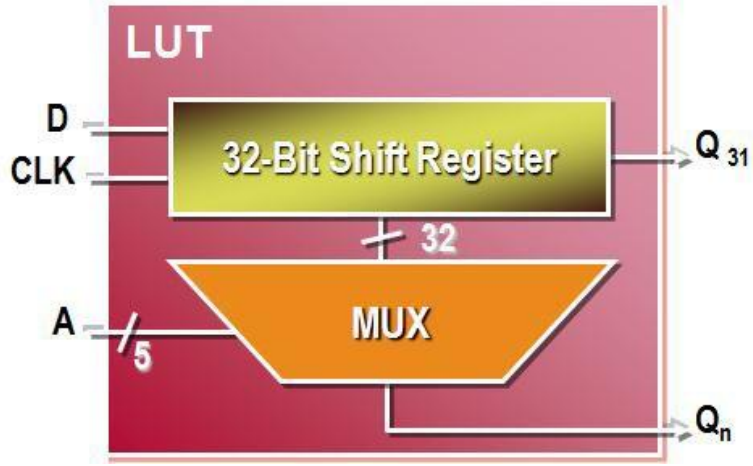
Control Sets

- **All flip-flops and flip-flop/latches share the same CK, SR, and CE signals**
  - This is referred to as the "control set" of the flip-flops
  - CE and SR are active high
  - CK can be inverted at the slice boundary
- **If any one flip-flop uses a CE, all others must use the same CE**
  - CE gates the clock at the slice boundary
  - Saves power
- **If any one flip-flop uses the SR, all others must use the same SR**
  - The reset value used for each flip-flop is individually set by the SRVAL attribute



SLICEM Used as 32-bit Shift Register

- **Versatile SRL-type shift registers**
  - Variable-length shift register
  - Synchronous FIFOs
  - Content-Addressable Memory (CAM)
  - Pattern generator
  - Compensate for delay / latency
- **Shift register length is determined by the address**
  - Constant value giving fixed delay line
  - Dynamic addressing for elastic buffer
- **Cascadable up to 128x1 shift register in one slice**



SRL Configurations in One Slice (4 LUTs)
16x1, 16x2, 16x4, 16x6, 16x8
32x1, 32x2, 32x3, 32x4
64x1, 64x2
96x1
128x1

SLICEM Used as a Distributed SelectRAM Memory

- **Uses the same storage that is used for the look-up table function**
- **Synchronous write, asynchronous read**
  - Can be converted to synchronous read using the flip-flops available in the slice
- **Various configurations**
  - Single port
    - One LUT6 = 64x1 or 32x2 RAM
    - Cascadable up to 256x1 RAM
  - Dual port (D)
    - 1 read / write port + 1 read-only port
  - Simple dual port (SDP)
    - 1 write-only port + 1 read-only port
  - Quad-port (Q)
    - 1 read / write port + 3 read-only ports

Single Port	Dual Port	Simple Dual Port	Quad Port
32x2	32x2**D**	32x6**SDP**	32x2**Q**
32x4	32x4**D**	64x3**SDP**	64x1**Q**
32x6	64x1**D**		
32x8	64x2**D**		
64x1	128x1**D**		
64x2			
64x3			
64x4			
128x1			
128x2			
256x1			

Each Port Has Independent Address Inputs

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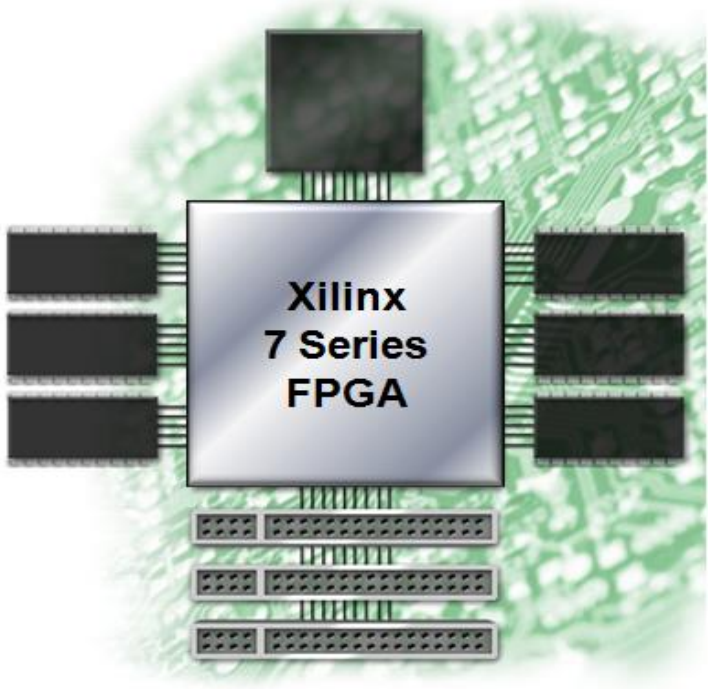
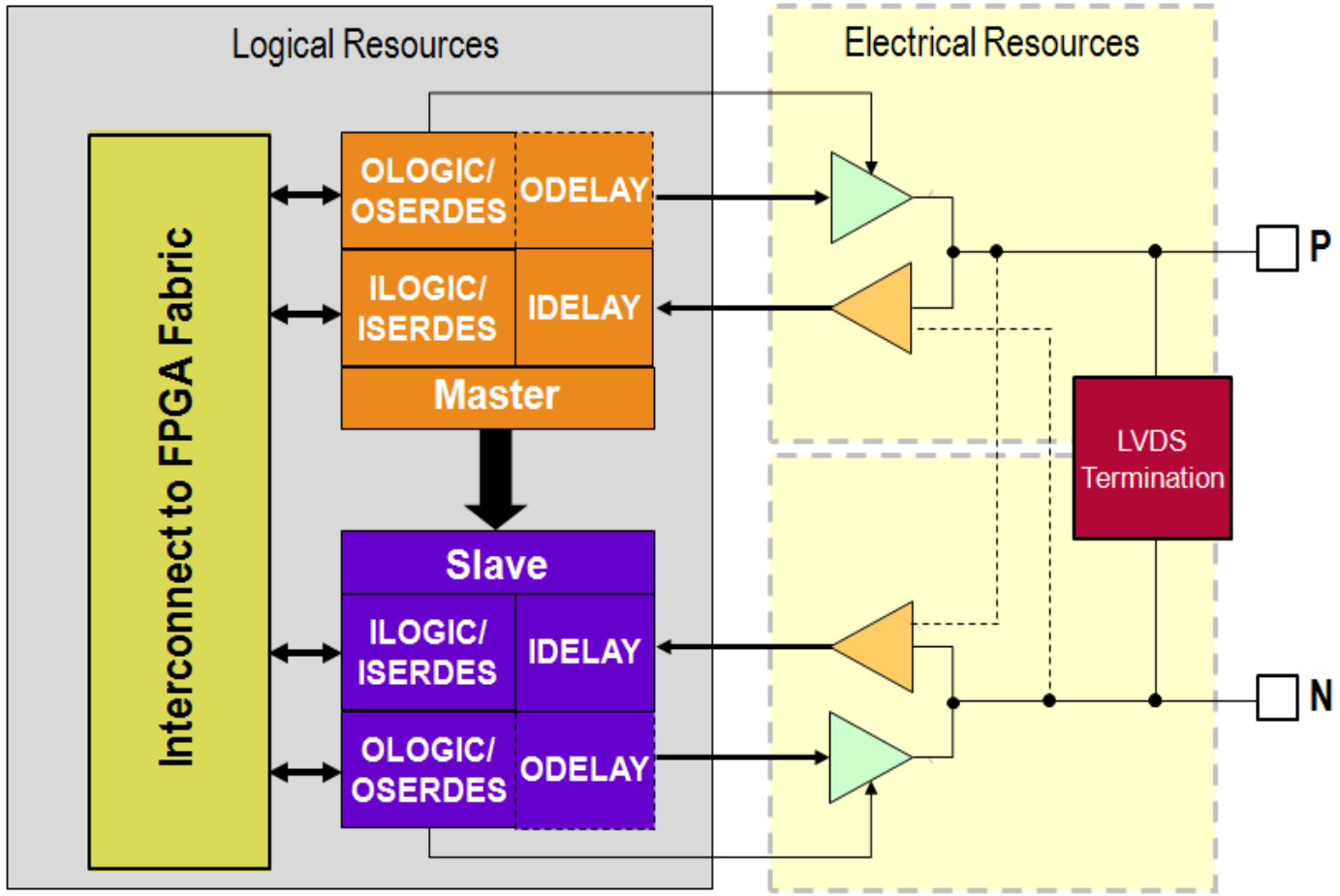
7-Series FPGA I/O

- **Wide range of voltages**
  - 1.2V to 3.3V operation
- **Many different I/O standards**
  - Single ended and differential
  - Referenced inputs
  - 3-state support
- **Very high performance**
  - Up to 1600 Mbps LVDS
  - Up to 1866 Mbps single-ended for DDR3
- **Easy interfacing to standard memories**
  - Hardware support for QDRII+ and DDR3
- **Digitally controlled impedance**
- **Low power**
  - Features to reduce power

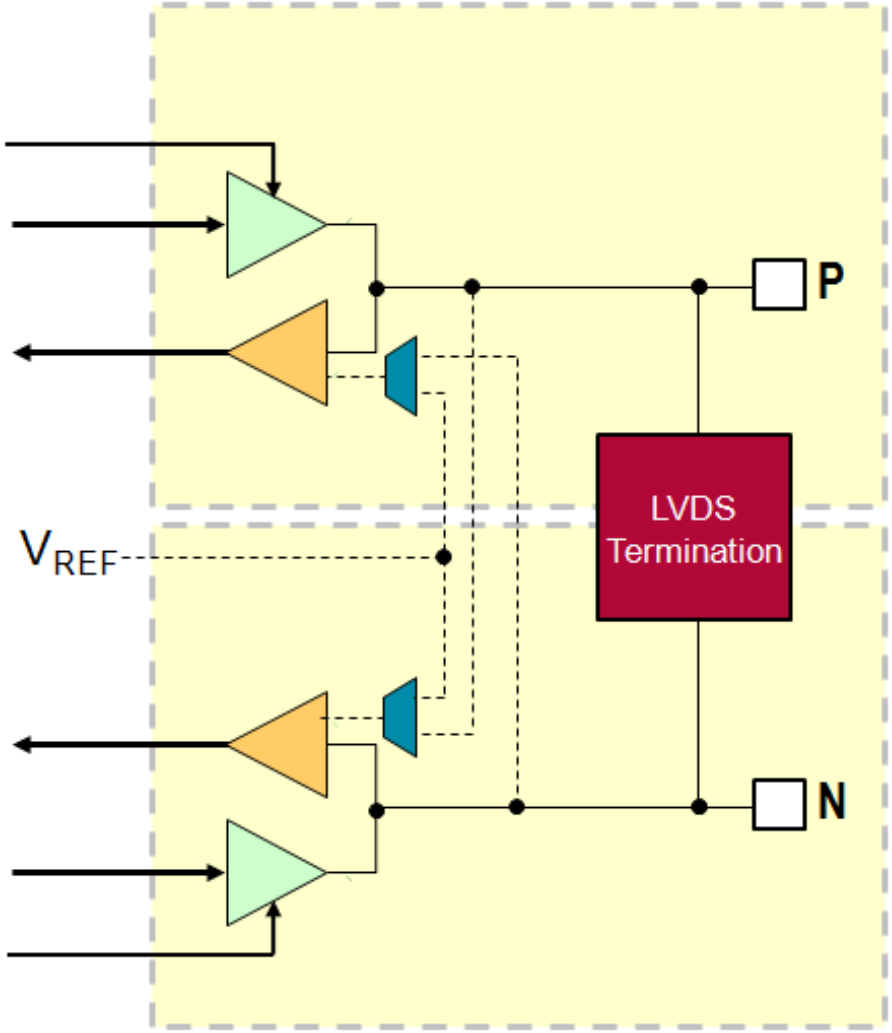


I/O Block Diagram



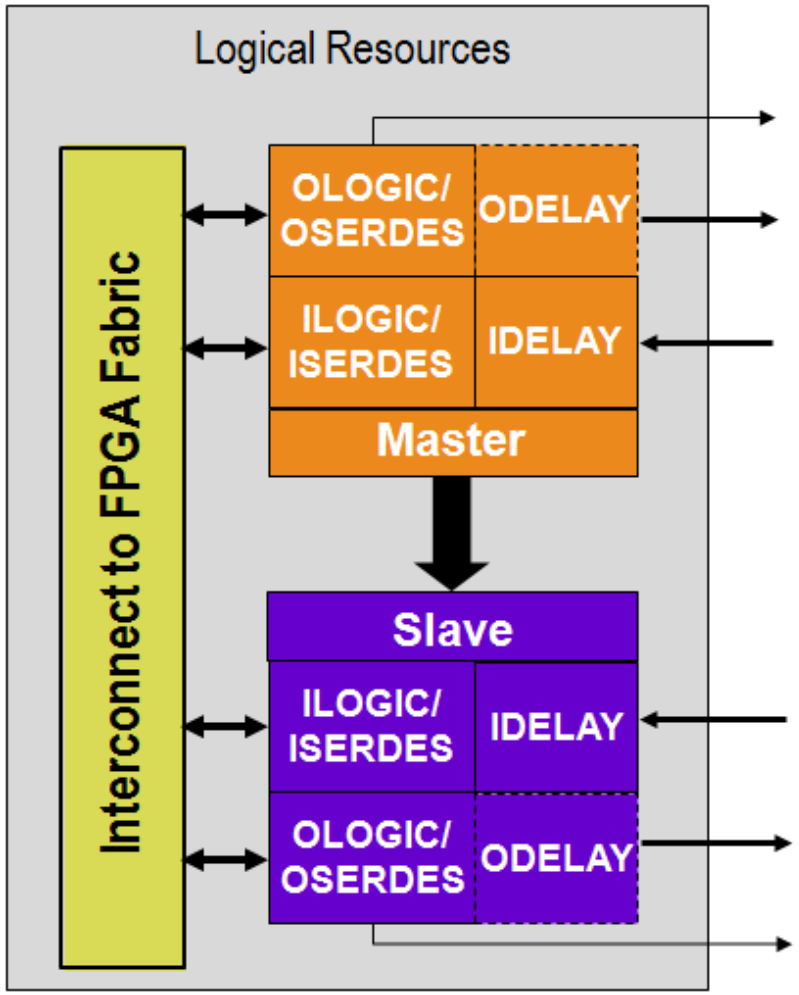
I/O Electrical Resources

- **P and N pins can be configured as**
  - Individual single-ended signals or
  - Differential pair
- **Receiver can be standard CMOS or voltage comparator**
  - When standard CMOS
    - Logic 0 when "near" ground
    - Logic 1 when "near" V_{CCO}
  - Referenced to V_{REF}
    - Logic 0 when below V_{REF}
    - Logic 1 when above V_{REF}
  - Differential
    - Logic 0 when $V_P < V_N$
    - Logic 1 when $V_P > V_N$



I/O Logical Resources

- **Two blocks of logic per I/O pair**
  - Master and slave
  - Can operate independently or concatenated
- **Each block contains**
  - ILOGIC/ISERDES
    - SDR, DDR, or high-speed serial input logic
  - OLOGIC/OSERDES
    - SDR, DDR, or high-speed serial output logic
  - IDELAY
    - Selectable fine-grained input delay
  - ODELAY
    - Selectable fine-grained output delay
    - Only available on High Performance I/O



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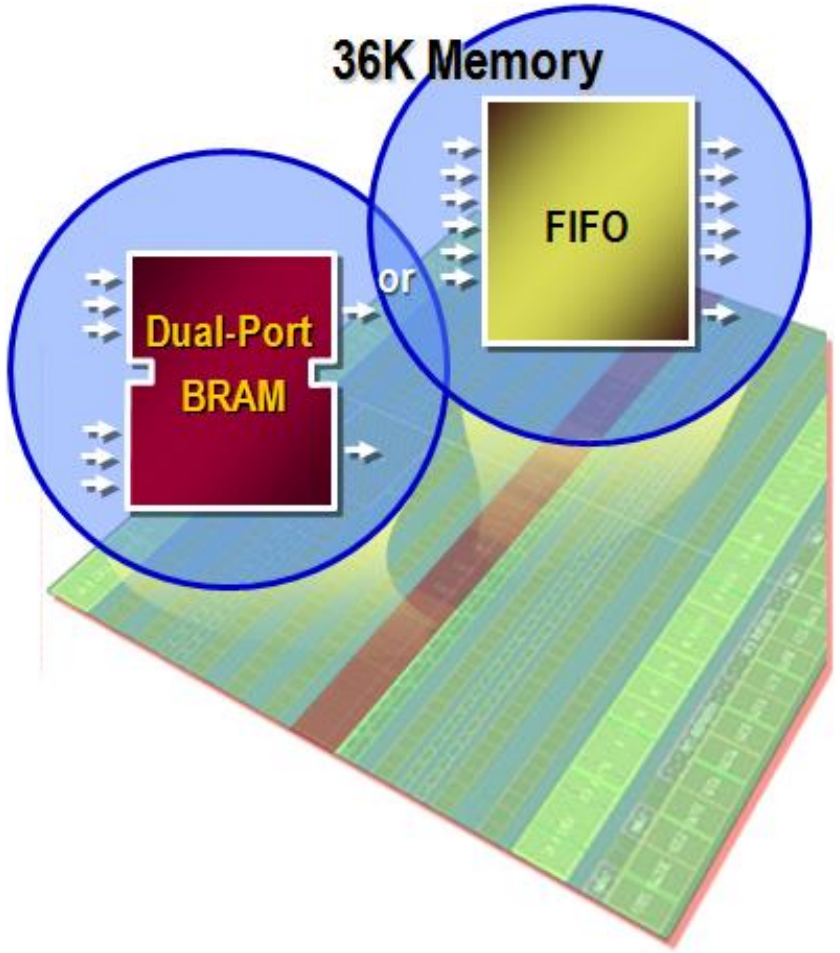
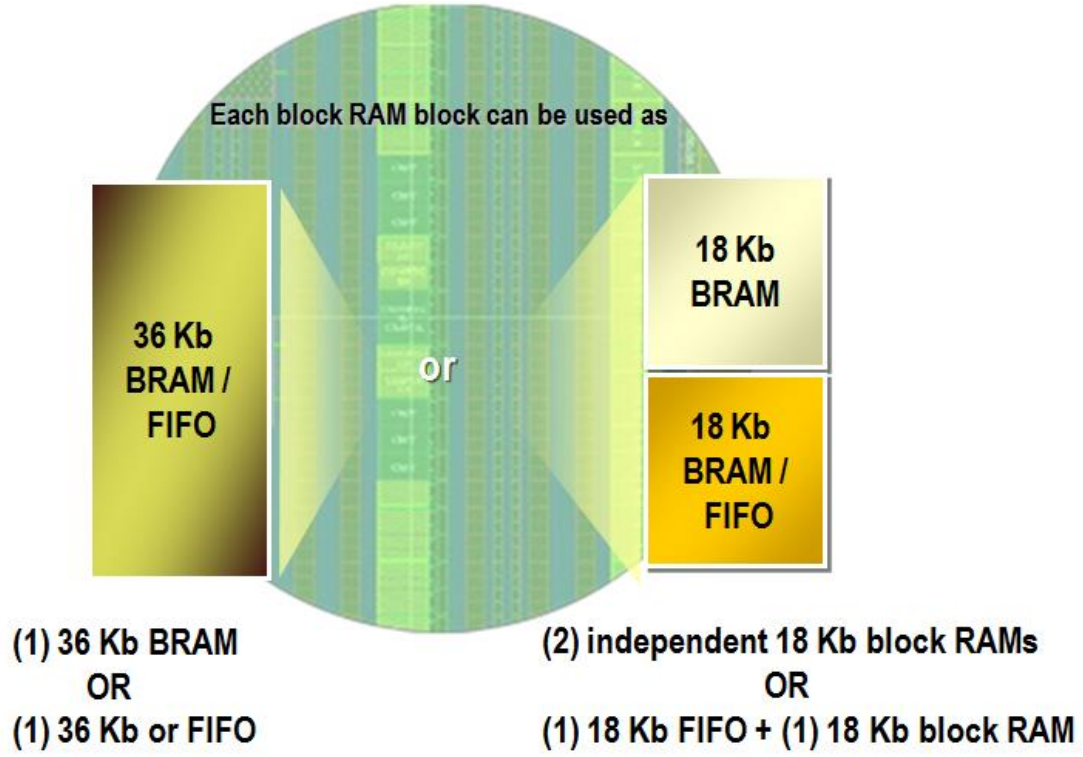
7-Series Block RAM and FIFO

- **All members of the 7-series families have the same Block RAM/FIFO**
- **Fully synchronous operation**
  - All operations are synchronous; all outputs are latched
- **Optional internal pipeline register for higher frequency operation**
- **Two independent ports access common data**
  - Individual address, clock, write enable, clock enable
  - Independent data widths for each port

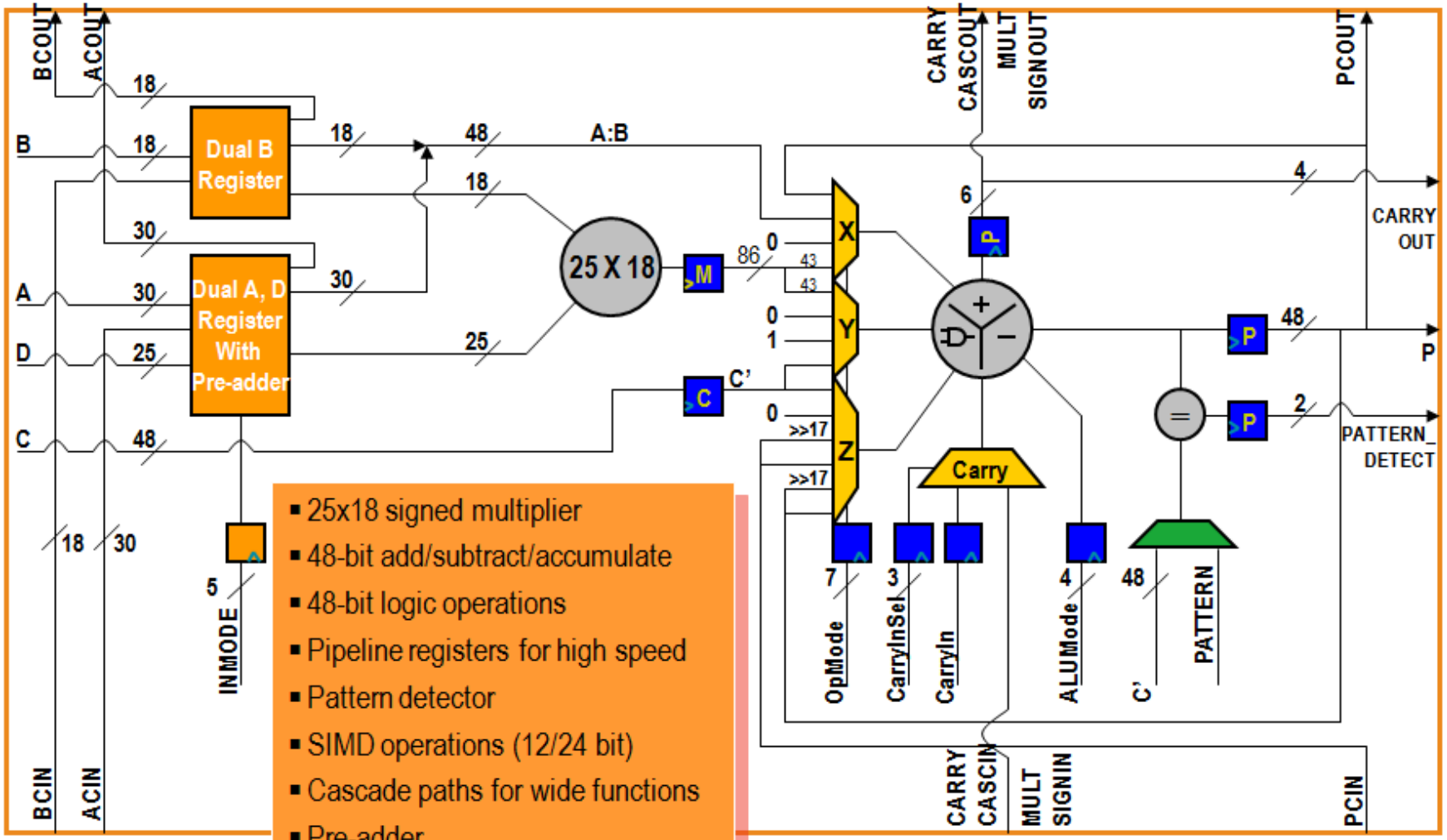


7-Series Block RAM and FIFO

- **Multiple configuration options**
  - True dual-port, simple dual-port, single-port
- **Integrated cascade logic**
- **Byte-write enable in wider configurations**
- **Integrated control for fast and efficient FIFOs**
- **Integrated 64 / 72-bit Hamming error correction**
- **Separate Vbram supply to ensure block memory functionality in -1L**



7-Series DSP48E1 Slice



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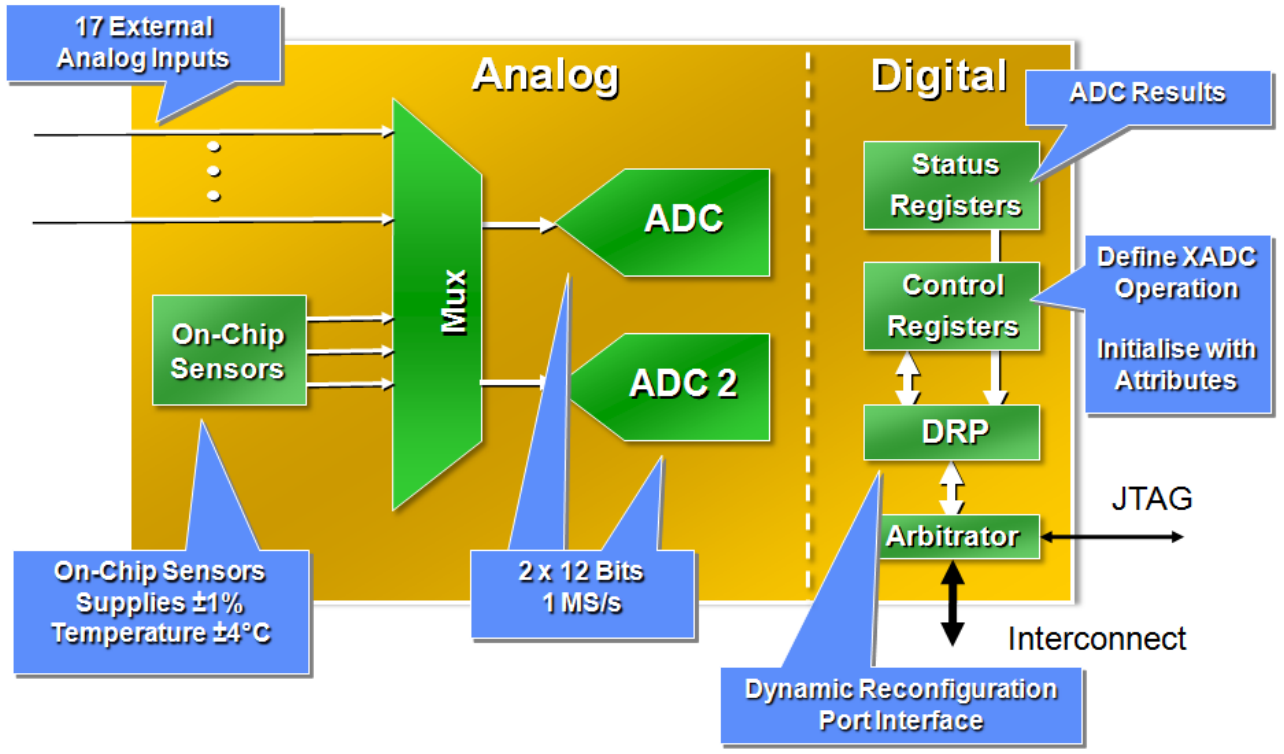
XADC and AMS

- **XADC is a high quality and flexible analog interface new to the 7-series**
  - Dual 12-bit 1Msps ADCs, on-chip sensors, 17 flexible analog inputs, and track & holds with programmable signal conditioning
  - 1V input range
  - 16-bit resolution conversion
  - Built in digital gain and offset calibration
- **Analog Mixed Signal (AMS)**
  - Using the FPGA programmable logic to customize the XADC and replace other external analog functions; for example, linearization, calibration, filtering, and DC balancing to improve data conversion resolution

XADC Block Diagram

- **Fast sampling**
  - Conversion time of 1 us with support for simultaneous sampling
  - Flexible timing modes (self and externally triggered sampling modes)
  - Separate track/hold amplifier for each ADC ensures maximum throughput using multiplexed analog input channels
- **Flexible analog inputs**
  - Differential analog inputs with high common mode noise rejection
  - Support for unipolar, bipolar, and true differential input signal types



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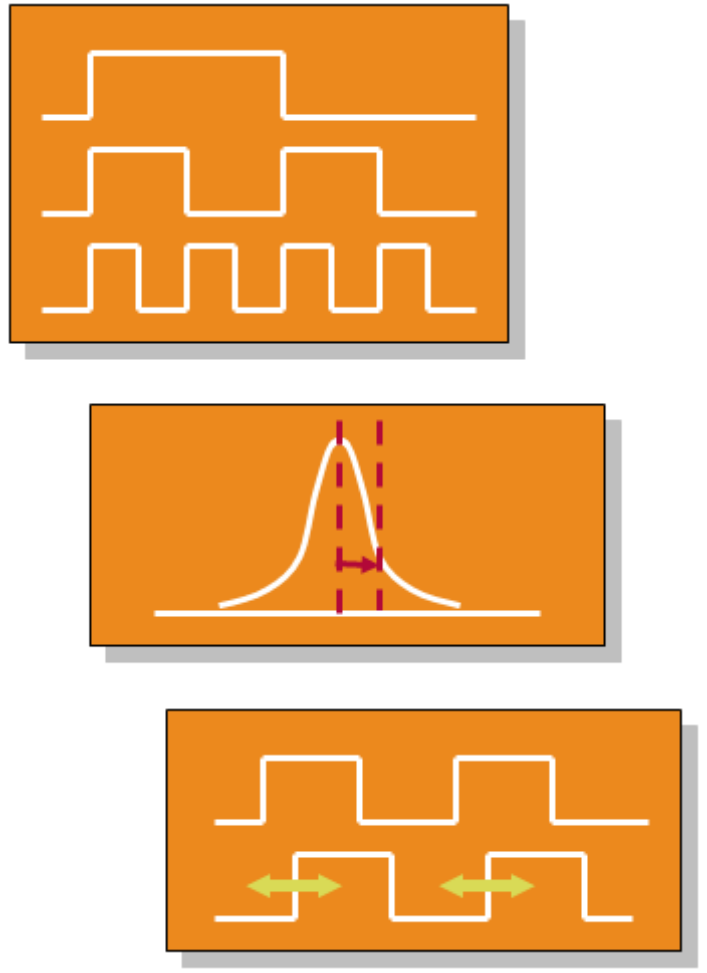
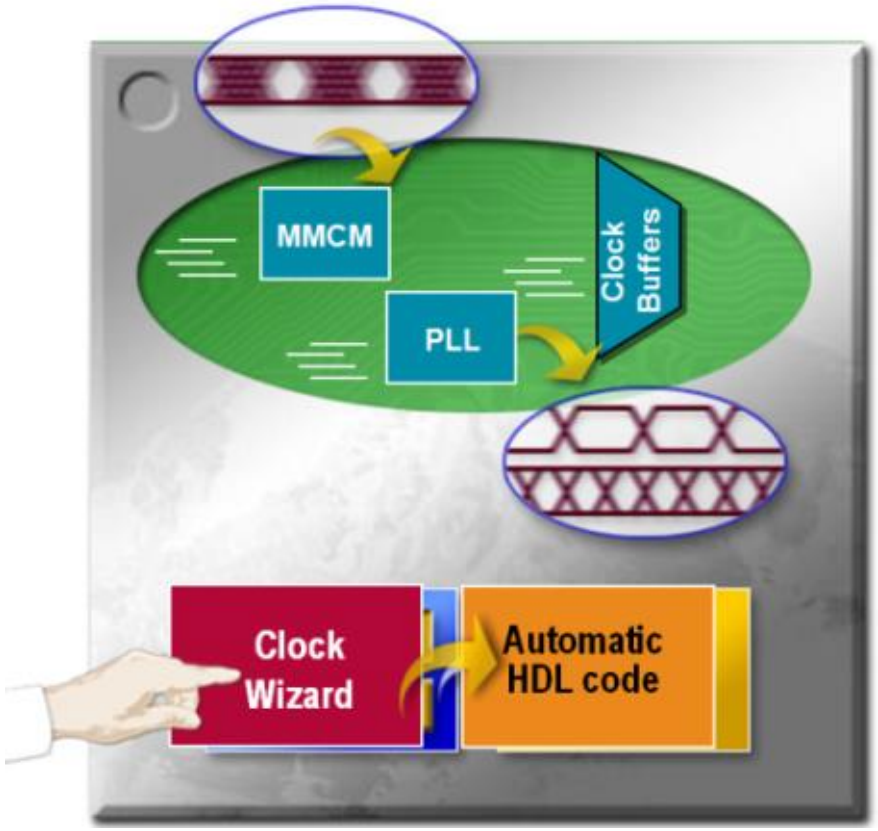
High-Performance Clocking

- **Modern applications have complex clocking requirements**
  - Extremely high-performance clock signals
  - Support for multiple frequency domains across a wide frequency range
  - De-skewing of clocks relative to one another
  - Low jitter and precise duty cycle to maintain the widest possible data valid window
  - Lowest possible system power
- **Xilinx FPGAs have a rich mixture of clocking resources to accommodate these requirements**
  - The perfect balance of resources at the right cost



7-Series FPGAs Clock Management

- **Global clock buffers**
  - High fanout clock distribution buffer
- **Low-skew clock distribution**
  - Regional clock routing
- **Clock regions**
  - Each clock region is 50 CLBs high and spans half the device
- **Clock management tile (CMT)**
  - One Mixed-Mode Clock Managers (MMCMs) and one Phase Locked Loop (PLL) in each CMT
  - Performs frequency synthesis, clock de-skew, and jitter-filtering
  - High input frequency range
- **Simple design creation through the Clocking Wizard**



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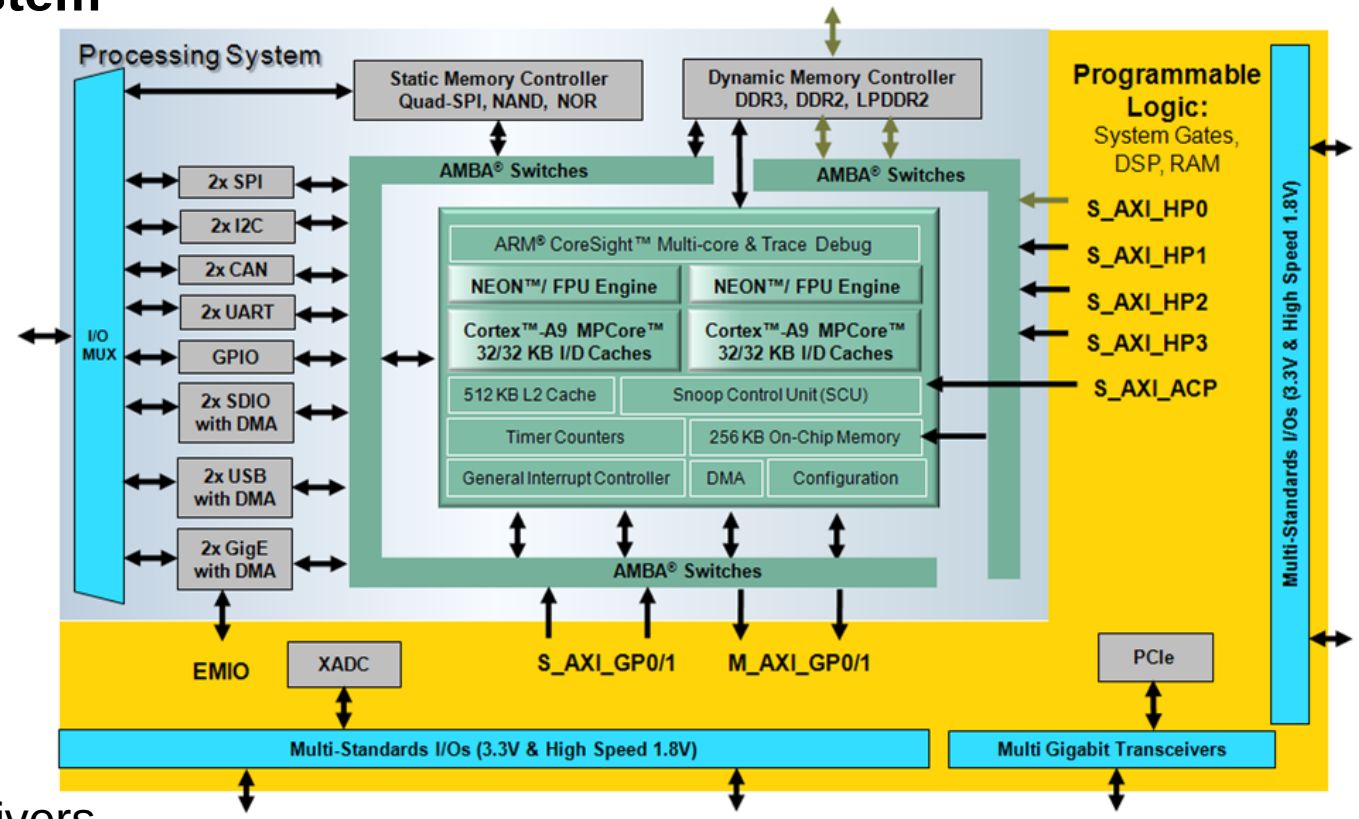
Zynq-7000 Family Highlights

- **Complete ARM®-based processing system**
  - Application Processor Unit (APU)
    - Dual ARM Cortex™-A9 processors
    - Caches and support blocks
  - Fully integrated memory controllers
  - I/O peripherals
- **Tightly integrated programmable logic**
  - Used to extend the processing system
  - Scalable density and performance
- **Flexible array of I/O**
  - Wide range of external multi-standard I/O
  - High-performance integrated serial transceivers
  - Analog-to-digital converter inputs



The PS and the PL

- **The Zynq-7000 AP SoC architecture consists of two major sections**
  - PS: Processing system
    - Dual ARM Cortex-A9 processor based
    - Multiple peripherals
    - Hard silicon core
  - PL: Programmable logic
    - Shares the same 7-series programmable logic as
      - Artix™-based devices: Z-7010, Z-7015, and Z-7020 (high-range I/O banks only)
      - Kintex™-based devices: Z-7030, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)

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Summary

- **The 7-series FPGA slices contain four 6-input LUTs, eight registers, and carry logic**
  - LUTs can perform any combinatorial function of up to six inputs
  - LUTs are connected with dedicated multiplexers and carry logic
  - Some LUTs can be configured as shift registers or memories
  - Slices also contain carry logic and the MUXF7 and MUXF8 multiplexers
  - The MUXF7 multiplexers combine LUT outputs to create 7-input functions or 8-input multiplexers
  - The MUXF8 multiplexers combine the MUXF7 outputs to create 8-input functions or 16-input multiplexers
  - The carry logic can be used to implement fast addition, subtraction, and comparison operations
- **The 7-series FPGA IOBs contain DDR registers as well as SERDES resources**
- **The SelectIO™ interfaces enable direct connection to multiple I/O standards**

Summary

- The 7-series FPGA includes dedicated block RAM and DSP slice resources
- The 7-series FPGAs includes dedicated MMCMs, PLLs, and routing resources to improve your system clock performance and generation capability
- The 7-series FPGAs include other dedicated hardware such as XADC
- The Zynq-7000 processing platform is a system on a chip (SoC) processor with embedded programmable logic fabric of either Artix or Kintex 7-series FPGA